

PE International 2023

Plasma Dicing of GaN on Si Wafers

18th – 19th April 2023, Brussels, Belgium

Panasonic Connect Co., Ltd., Japan*¹

Panasonic Connect Europe GmbH, Germany*²

Atsushi Harikai*¹, James Weber*²



Agenda

1. Introduction

- Panasonic Connect introduction
- Process Automation Business Division introduction

2. Plasma dicing for GaN on Si

- Background
- Total solution for GaN on Silicon device

3. Equipment lineup for Dry Etching and Plasma Dicing

- Dry etching equipment
- Plasma dicing equipment
- Introduction of Plasma Dicing Demo Center

Agenda

1. Introduction

- Panasonic Connect introduction
- Process Automation Business Division introduction

2. Plasma dicing for GaN on Si

- Background
- Total solution for GaN on Silicon device

3. Equipment lineup for Dry Etching and Plasma Dicing

- Dry etching equipment
- Plasma dicing equipment
- Introduction of Plasma Dicing Demo Center

Panasonic Group Structure

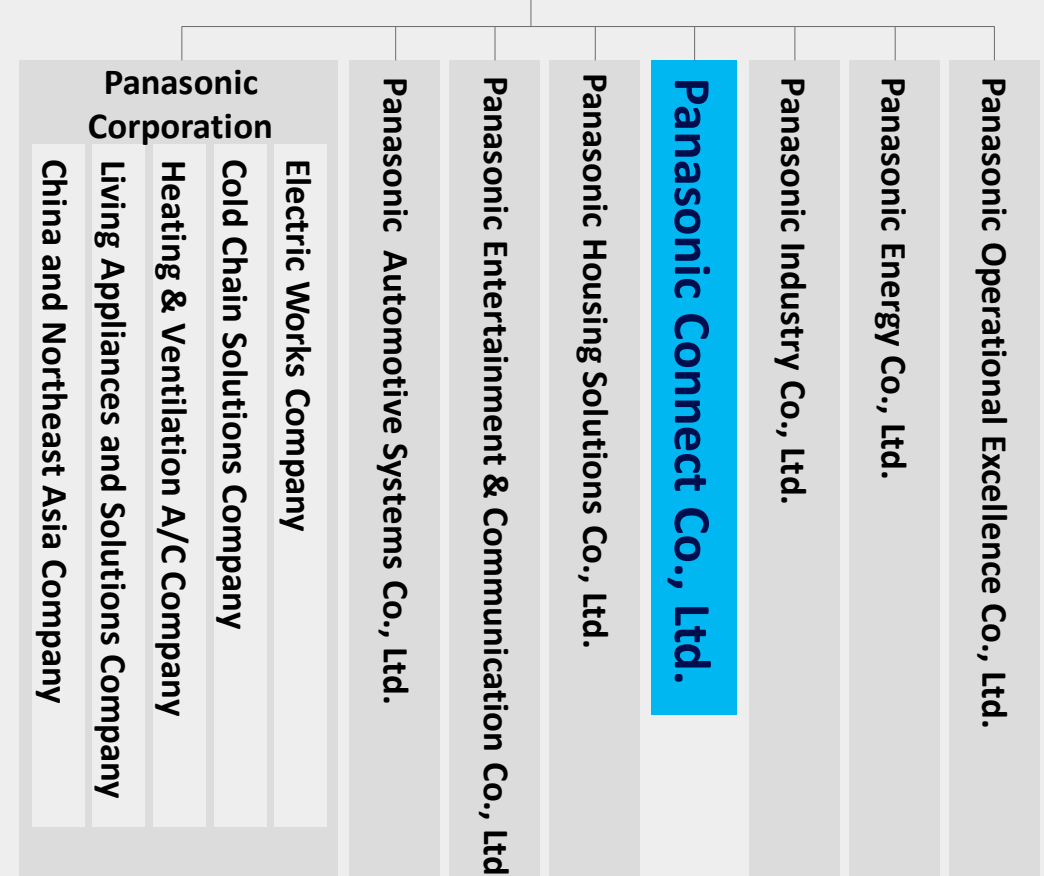
Up to March 2022

From April 2022

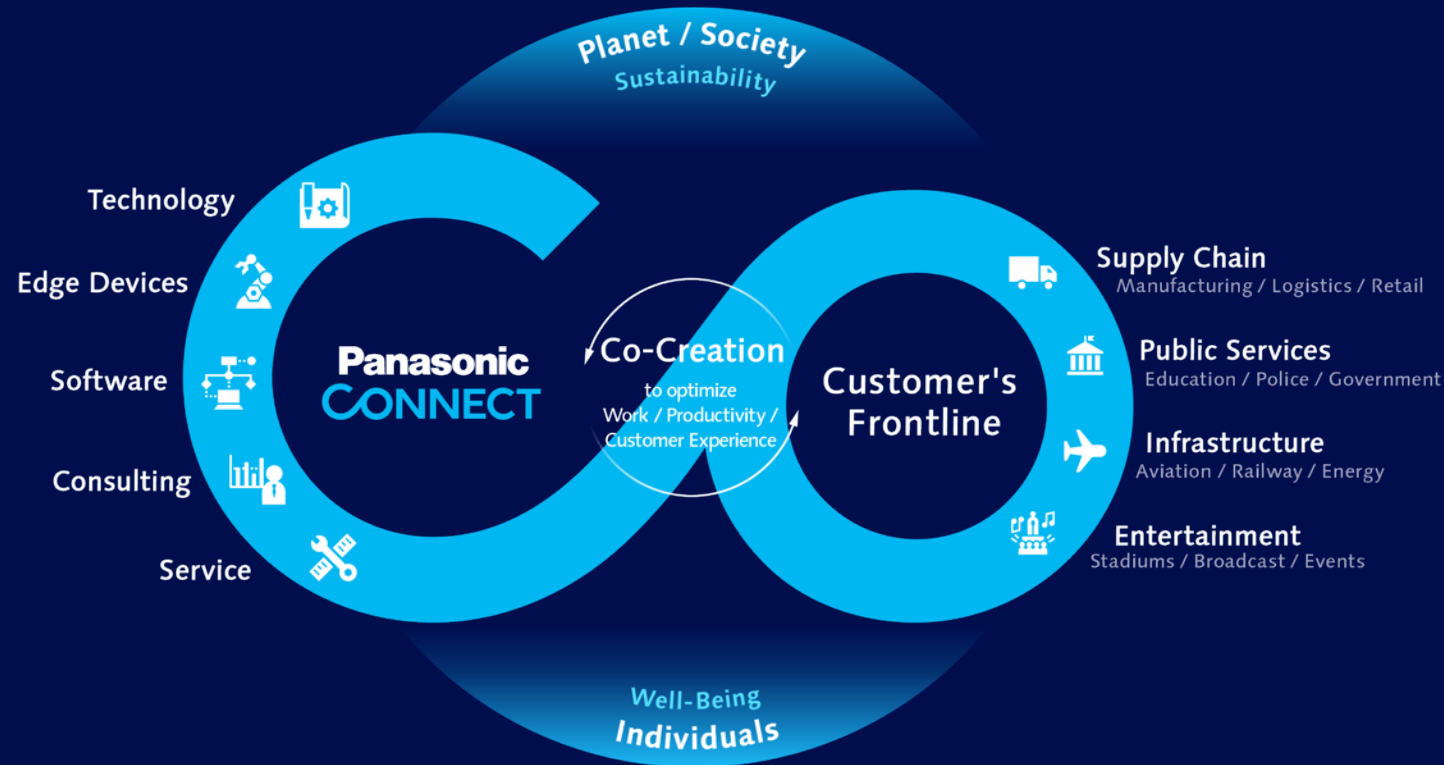
Panasonic Corporation

- Corporate Strategy & Technology Sector
- Lifestyle Updates Business Division
- Automotive Company
- Entertainment & Communication Business Division
- Housing Systems Business Division
- **Connected Solutions Company**
- Industry Company
- Energy Company
- Operational Excellence Company

Panasonic Holdings Corporation



Change Work, Advance Society, Connect to Tomorrow.

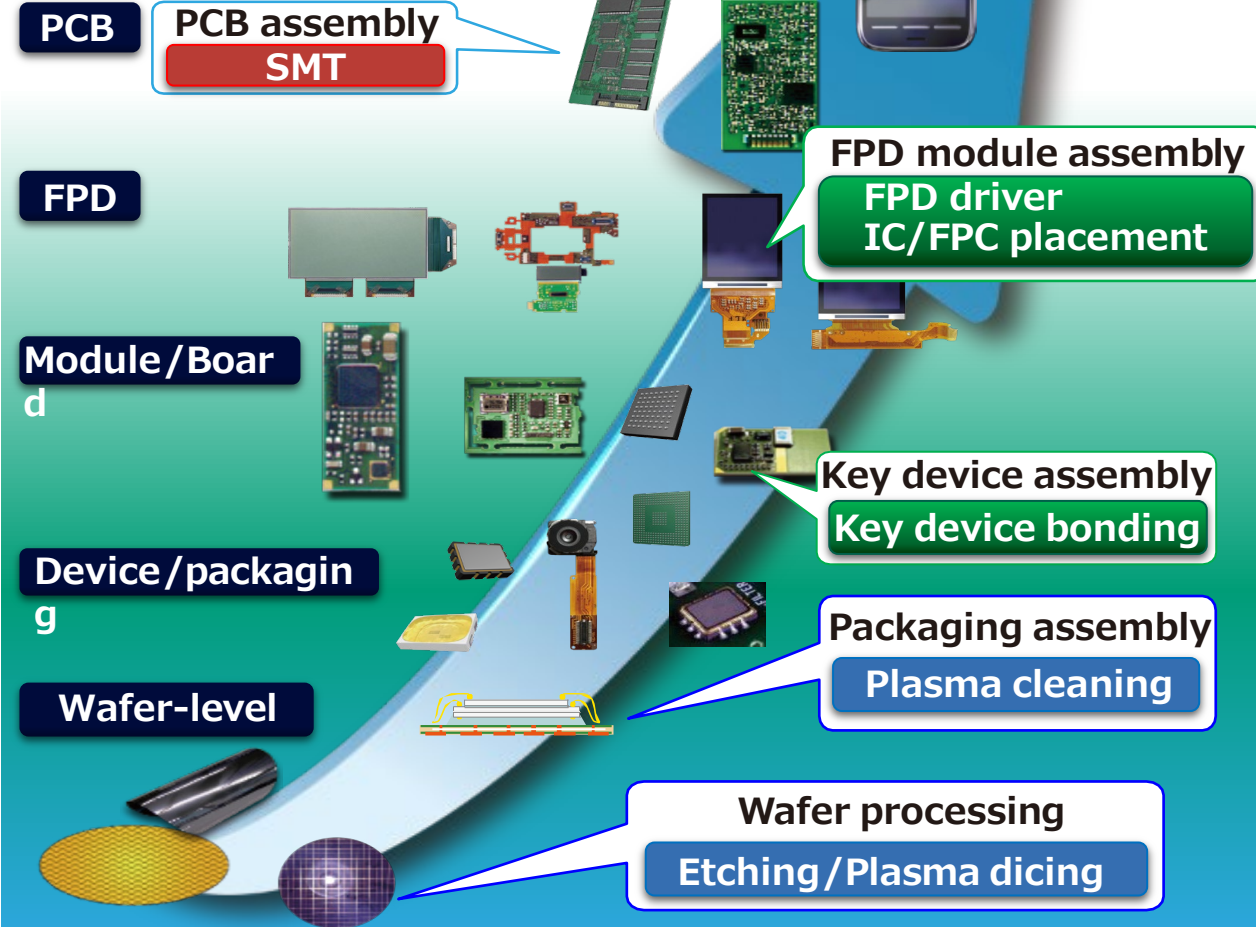


A better future through “Gemba Process Innovation”

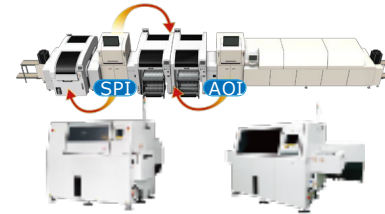
By leveraging Gemba Process Innovation to solve challenges we work alongside our customers with the ultimate goal of creating efficiency, a better society and a sustainable future.

Process Automation Business Division

Total solution for circuit formation
"Smart Manufacturing"



Surface mounting



Surface mounting for electronic circuit board

- Chip moulder
- Screen printer
- Insertion machine for lead component
- Insertion machine for odd-shape component

High-precision bonding



FPD Driver IC/FPC placement

COG bonder/FOG bonder

Key device placement

Die bonder/Flip chip bonder

High-precision processing



In this presentation

Etching and dicing

Dry etcher

Plasma dicer

Cleaning

Plasma cleaner

Agenda

1. Introduction

- Panasonic Connect introduction
- Process Automation Business Division introduction

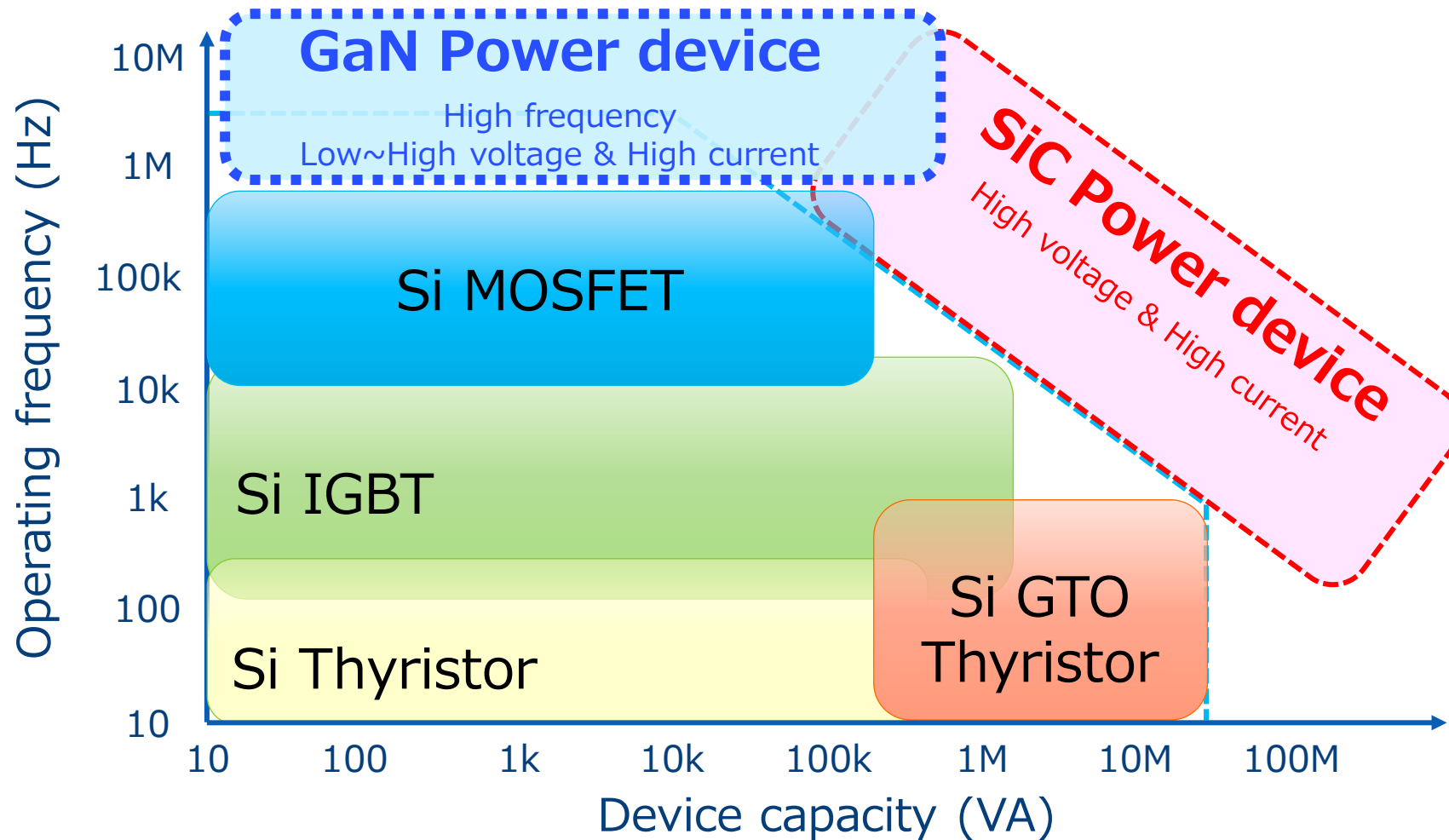
2. Plasma dicing for GaN on Si

- Background
- Total solution for GaN on Silicon device

3. Equipment lineup for Dry Etching and Plasma Dicing

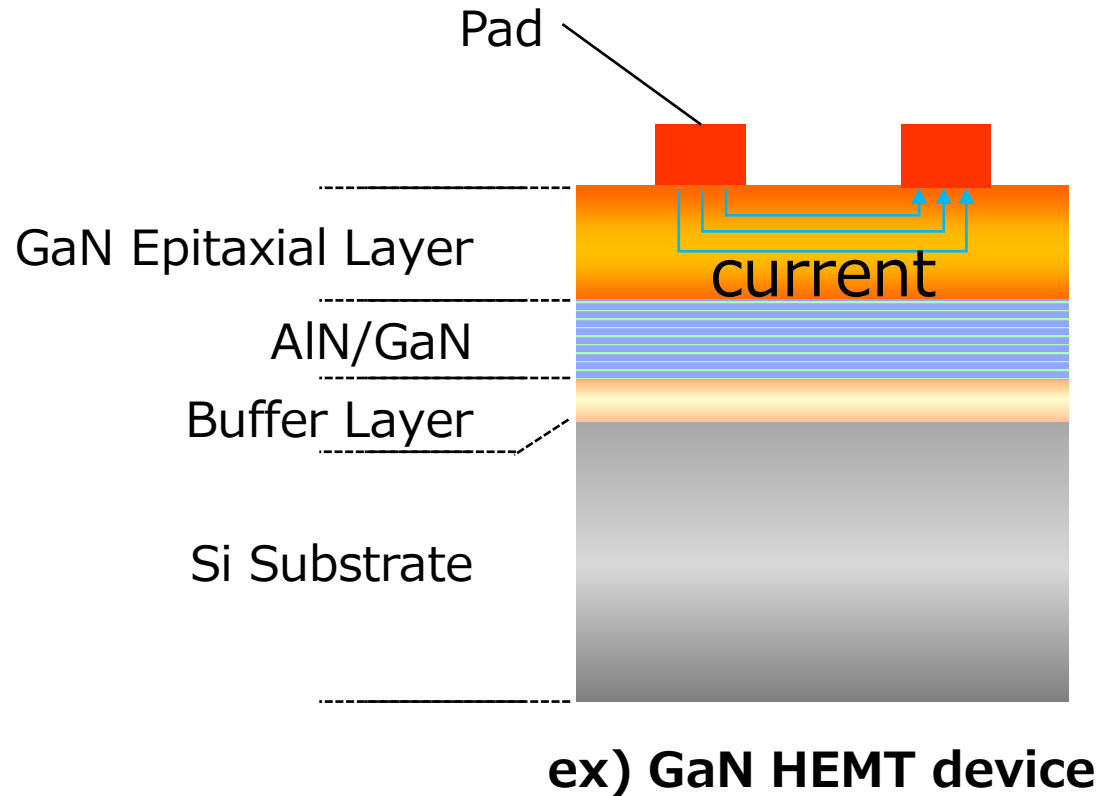
- Dry etching equipment
- Plasma dicing equipment
- Introduction of Plasma Dicing Demo Center

Applicable area of GaN power device



GaN power devices are effective for high operating frequency region

Device structure of GaN on Silicon Power Devices



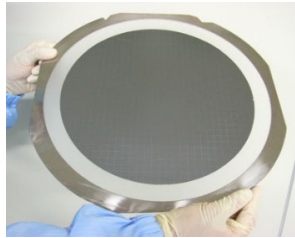
Feature of GaN on Silicon power device

- Withstand high voltage
 - Excellent switching characteristics
 - Low current loss
 - **Low production cost** compared to other compound power devices
- ➔ **Strong demand due to low production cost**

Panasonic proposes further low-cost production by using plasma dicing

Principles and Benefits of Plasma Dicing

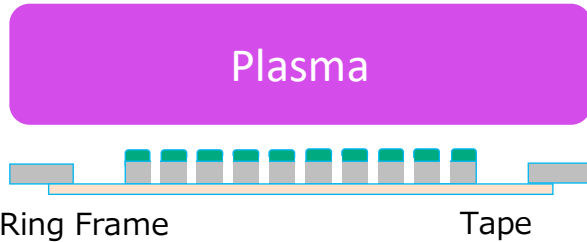
■ Outline of Plasma Dicing



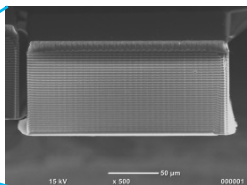
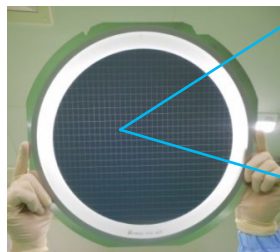
Wafer is mounted on metal ring frame and tape



Wafer is transferred into the Process Chamber



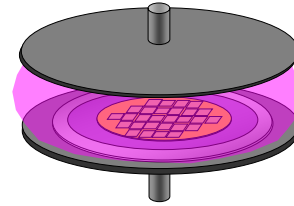
Wafer is transferred from the Process Chamber



Fully diced wafer by Plasma Dicing

Metal ring frame and tape have no damage

■ Benefits of Plasma Dicing



Plasma Dicing
by chemical reactance of gas

1. High Productivity & Low CoO

- Narrow dicing width and kerf margin by elimination cracks increases the amount of dies
- Parallel processing

2. No Damage & No Chipping

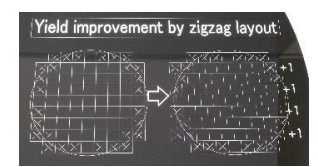
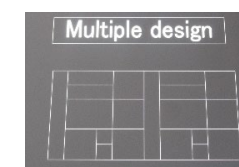
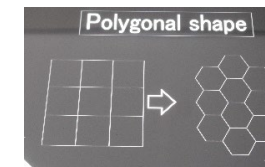
- Dicing of thin & fragile wafers w/o damage
- Possible to reduce the kerf margin
- Possible to dice with low device damage

3. No Dust & No Particle

- Clean chemical etching process
- No mechanical dust, debris, vibrations etc.
- Potential to reduce inspections

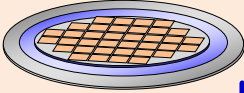
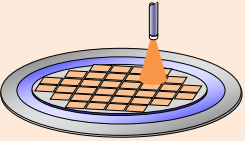
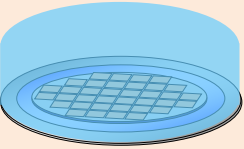
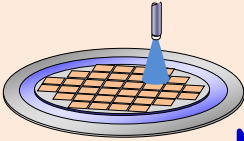
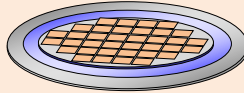
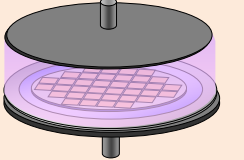
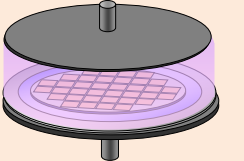
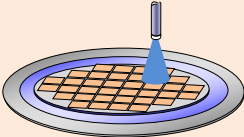
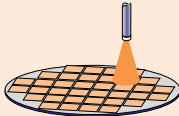
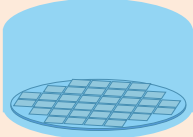
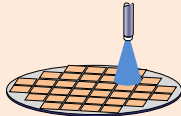
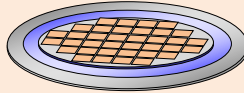
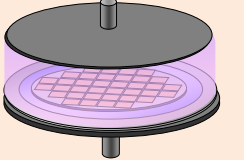
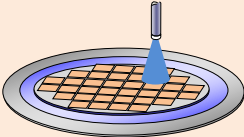



4. Variant Chip Shape & Layout

- Flexible die shapes and non-orthogonal layouts

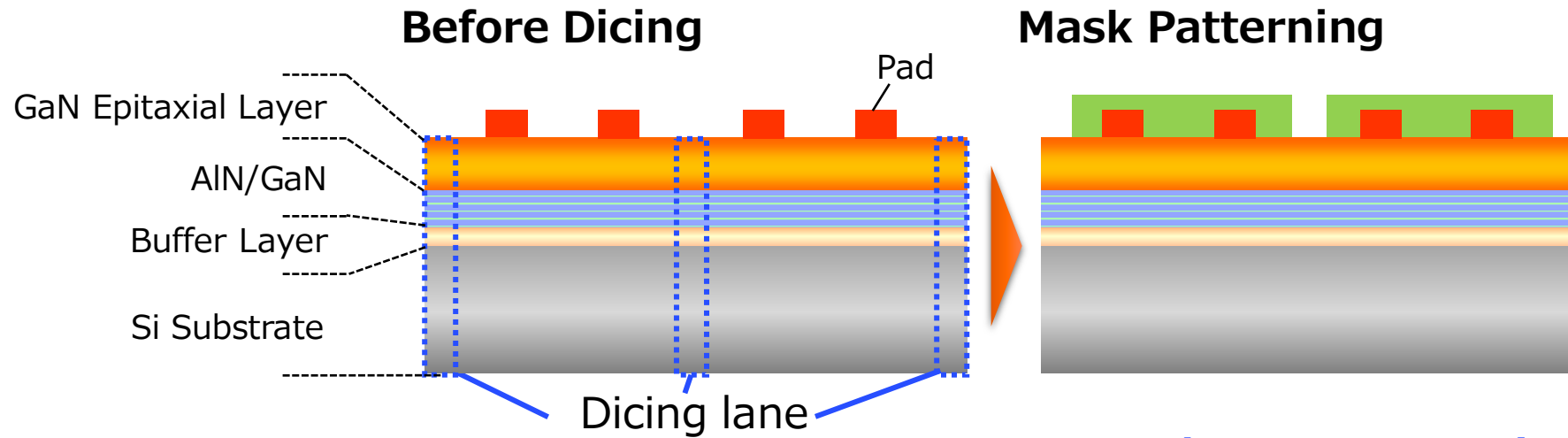


Panasonic proposes further low-cost production by using plasma dicing

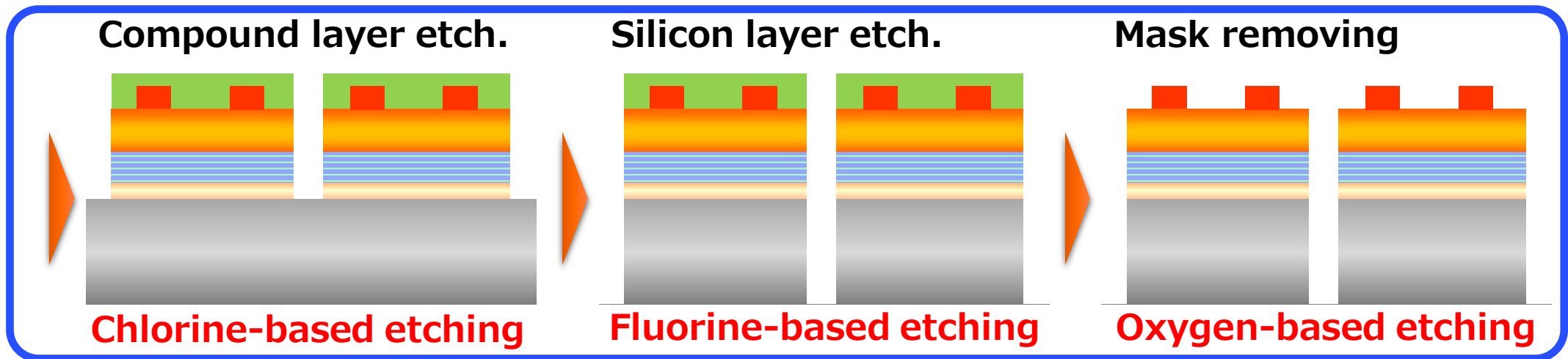
Plasma Dicing Process Flow for GaN on Si Devices

Wafer thickness	Process						
	Tape mounting	Mask Patterning			Tape mounting	Plasma Dicing	Mask Stripping
< 200µm		Coat 	Exposure 	Development 			Ashing  or Chemical Cleaning 
≥ 200µm	-						
Equipment	Tape mounter	EVG101 series 			Tape mounter	APX300-DM 	APX300-DM or wet station 

Plasma Dicing for GaN on Silicon Wafers



Plasma process in the same chamber



Various materials must be processed in the same chamber

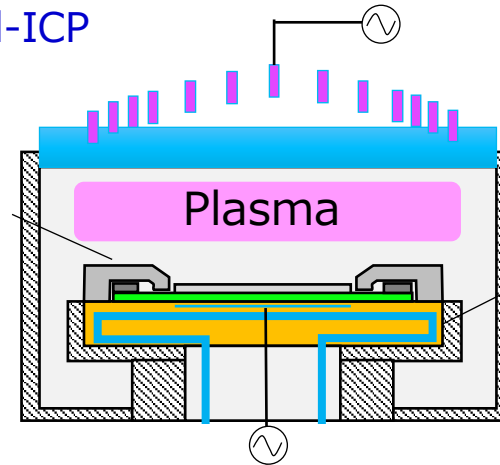
Feature of APX300-DM for GaN on Silicon Wafers

■ Equipment Information



Patented Enhanced-ICP

Patented
Dicing Ring Cover



Patented

Panasonic Original
ESC Electrode

•APX300-DM has optimized elemental technologies for Plasma Dicing

Configuration of APX300-DM Process Chamber

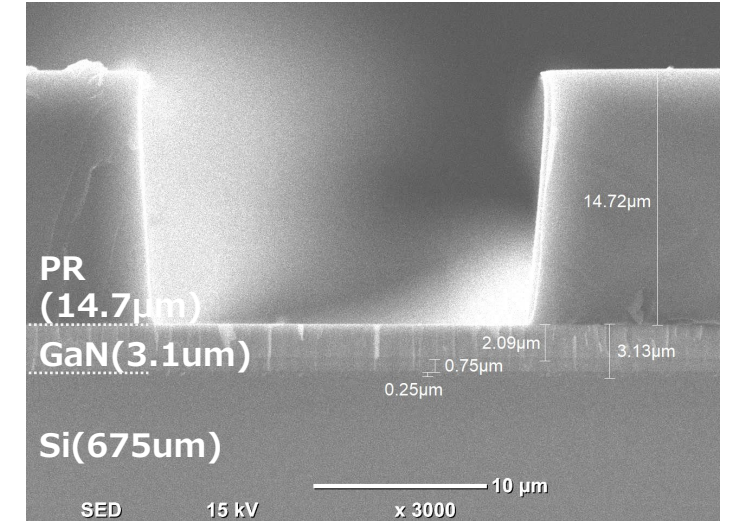
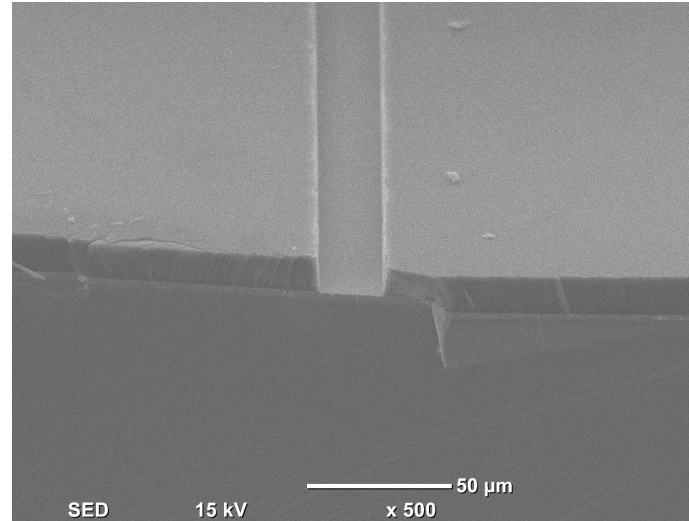
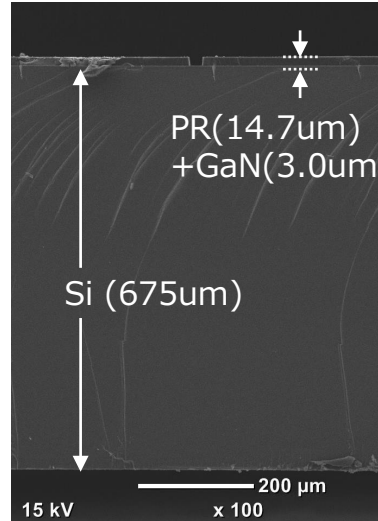
1. Enhanced ICP Plasma Source : High density and uniform plasma
2. Plasma Dicing ESC Electrode & Dicing Ring Cover
 - Patented Panasonic design enables the Plasma Dicing process to be performed on wafers mounted on ring frame with tape
 - Strong chucking force and cooling enables almost all dicing (DC) tape to be used.
 - Eliminates exposure of the tape and frame to plasma
3. Etching performance
 - Process chamber that can use both Fluorine-based and Chlorine-based etching gasses. Compound Semiconductor etching is possible
 - Multi layer dicing (GaN, AlGaN, SiO₂, SiN, DAF & Si) is possible

APX300-DM can use various gas types for each layer, and integrate this with high productivity dicing of GaN on Silicon wafers.

Evaluation of Plasma Dicing with GaN on Silicon Wafers

■ Sample Information

- Si wafer size: 6inch
- Thickness : 675um * non BG
- GaN layer structure :
GaN(2000nm)/AlNGaN(800nm)/AlN(200nm)
- Chip pitch : 1.38x1.67mm
- PR material : Novolak Photo Resist (PR)
positive type
- PR thickness : 14.7μm
- Dicing line width : 5, 10, 15, 20μm

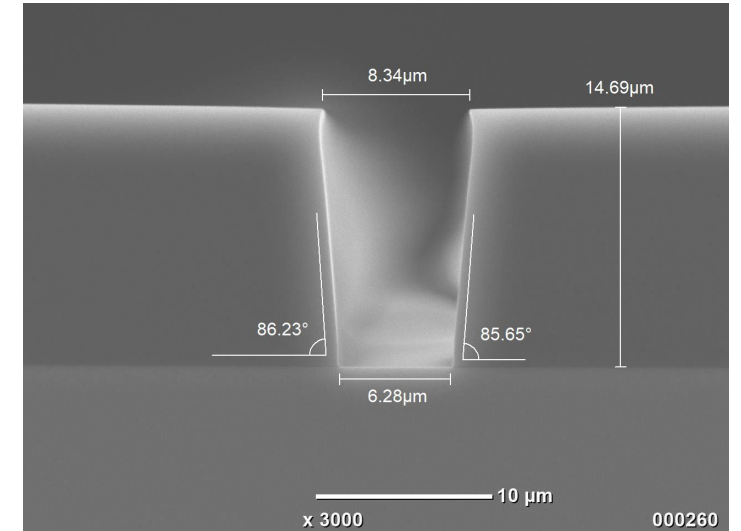
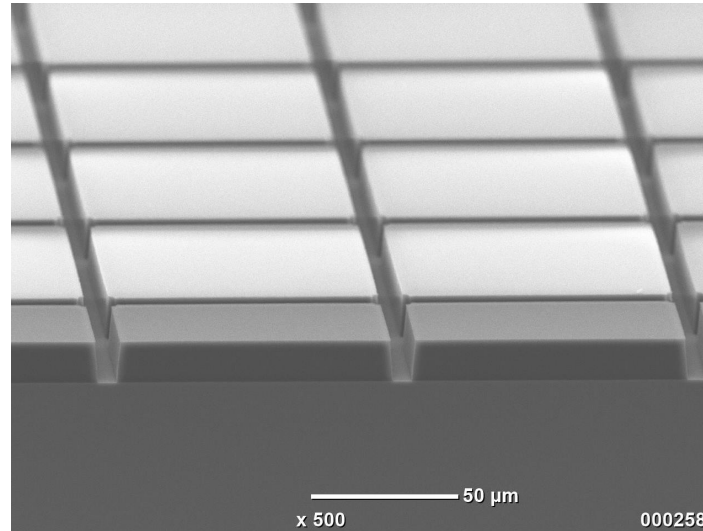
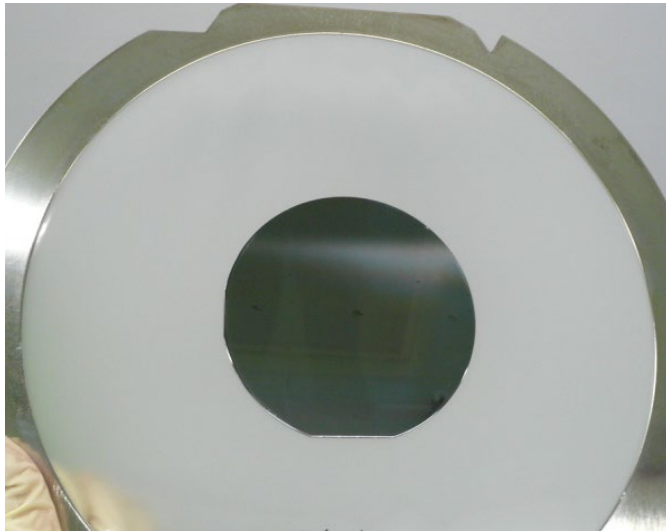


Structure of GaN on Silicon wafer after mask patterning @ 20um line

Example of Photo-lithography on FFC with thick PR

■ High Aspect Ratio PR for GaAs wafer

- Equipment : EVG101
- Resist : Novolak Photo Resist (PR)
- Wafer : GaAs wafer (150 μ mt) - 4inch



PR thickness : 14.6 μ m
Dicing width : 6.3 μ m
Chip pitch : 100x100 μ m
A/R = 2.3

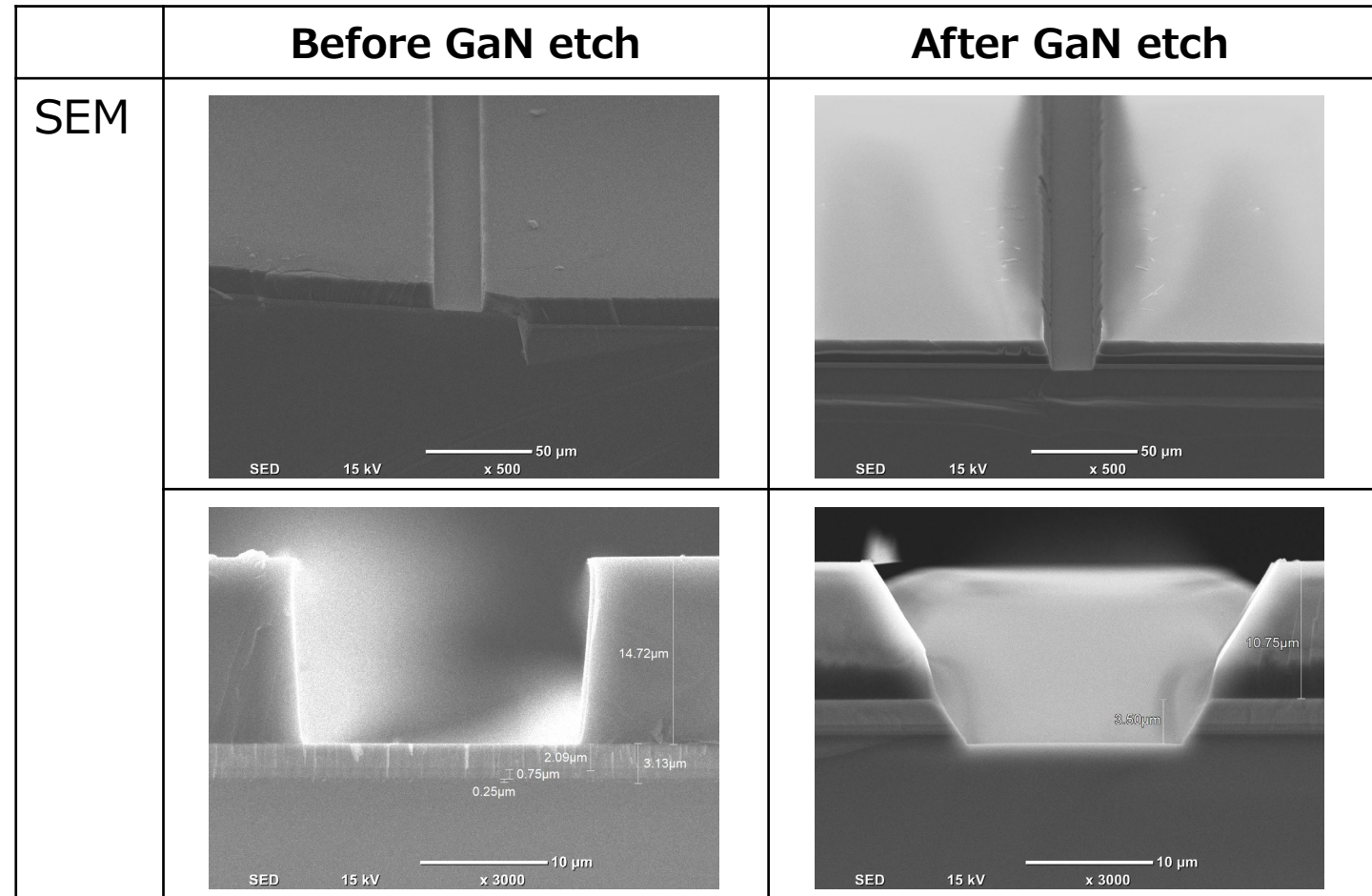
GaN Layer Etching : Basic Specification

■ Etching Condition

- Equipment : APX300-DM
- Etching gas : chlorine gas base
- Etching time : 4 min.

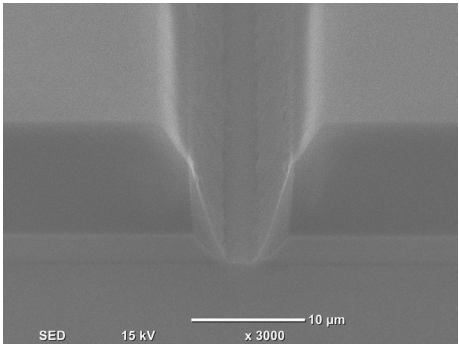
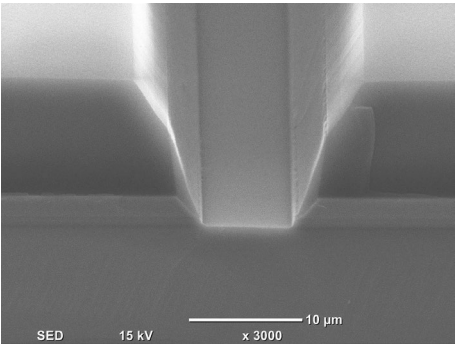
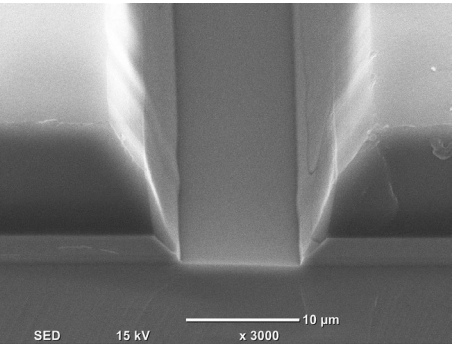
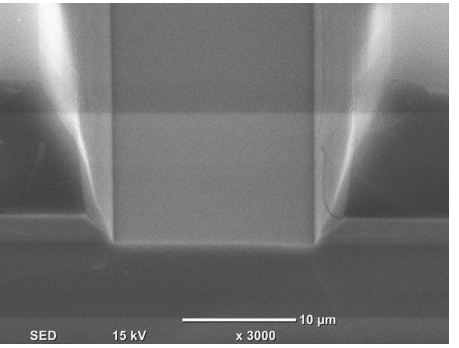
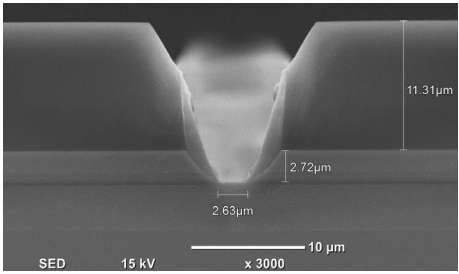
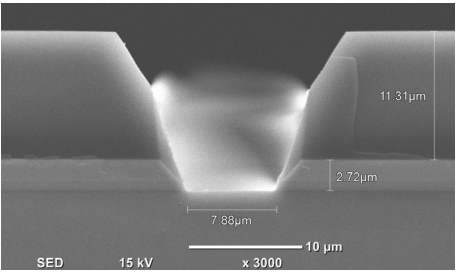
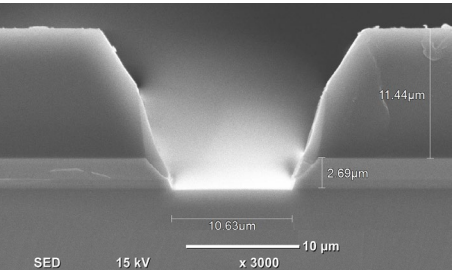
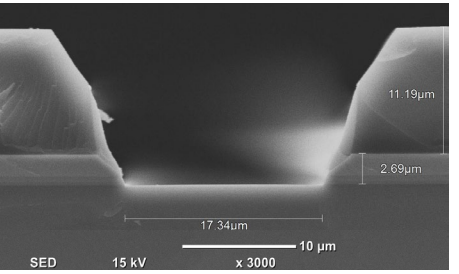
■ Etching Specification

- GaN Etching rate : 0.94 μ m/min.
- Selectivity(GaN+AlGaN+AlN / PR) : 0.89



GaN multi layer can be etched

GaN Layer Etching : Etching rate dependency on dicing width

	Dicing width [μm]			
	5 μm	10 μm	15 μm	20 μm
SEM				
Etching time 3 min.				
GaN rate [$\mu\text{m}/\text{min.}$]	0.91	0.91	0.90	0.90
PR sel.	0.94	0.94	0.97	0.89

GaN etching rate is similar, regardless of dicing line width

GaN Layer Etching : Etching rate uniformity on the wafer

	Wafer position				
	Center	Top	Bottom	Left	Right
<p>SEM</p> <p>Center 5µm Top 10µm Right 15µm Bottom 15µm Left 20µm</p> <p>Etching time : 3 min.</p>	<p>SED 15 kV x 3000 10 µm</p>	<p>SED 15 kV x 3000 10 µm</p>	<p>SED 15 kV x 3000 10 µm</p>	<p>SED 15 kV x 3000 10 µm</p>	<p>SED 15 kV x 3000 10 µm</p>
	<p>11.06µm 2.72µm</p> <p>SED 15 kV x 3000 10 µm</p>	<p>11.06µm 2.72µm</p> <p>SED 15 kV x 3000 10 µm</p>	<p>10.94µm 2.72µm</p> <p>SED 15 kV x 3000 10 µm</p>	<p>11.16µm 2.59µm</p> <p>SED 15 kV x 3000 10 µm</p>	<p>10.94µm 2.72µm</p> <p>SED 15 kV x 3000 10 µm</p>
GaN rate [µm/min.]	0.91	0.91	0.86	0.91	0.90
	(Ave.) 0.90µm/min. (Unif.) ±2.41%				
PR sel.	0.94	0.87	0.85	0.90	0.83

Uniform processing on the entire wafer area is achieved

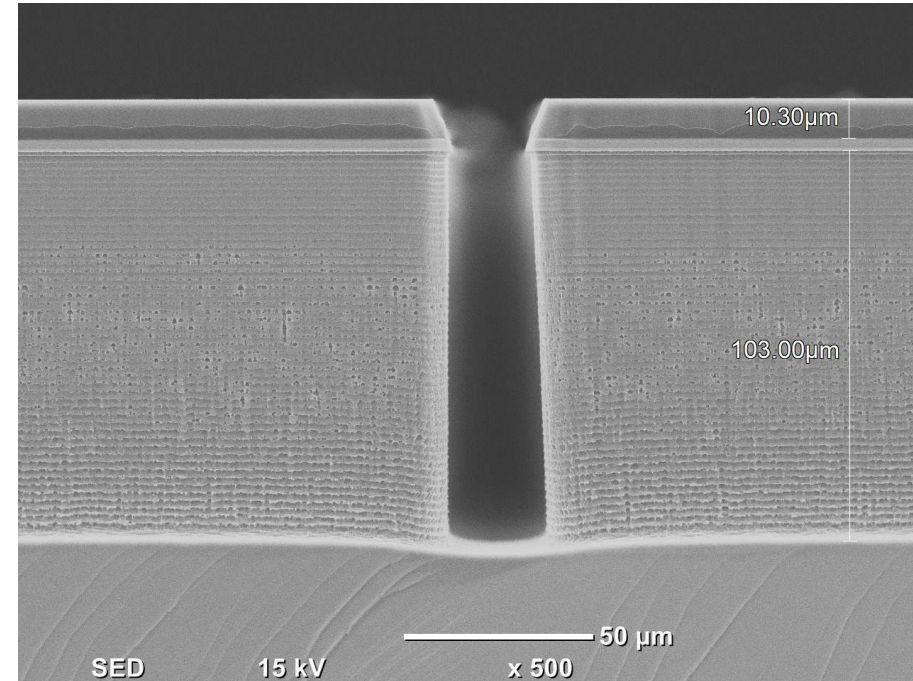
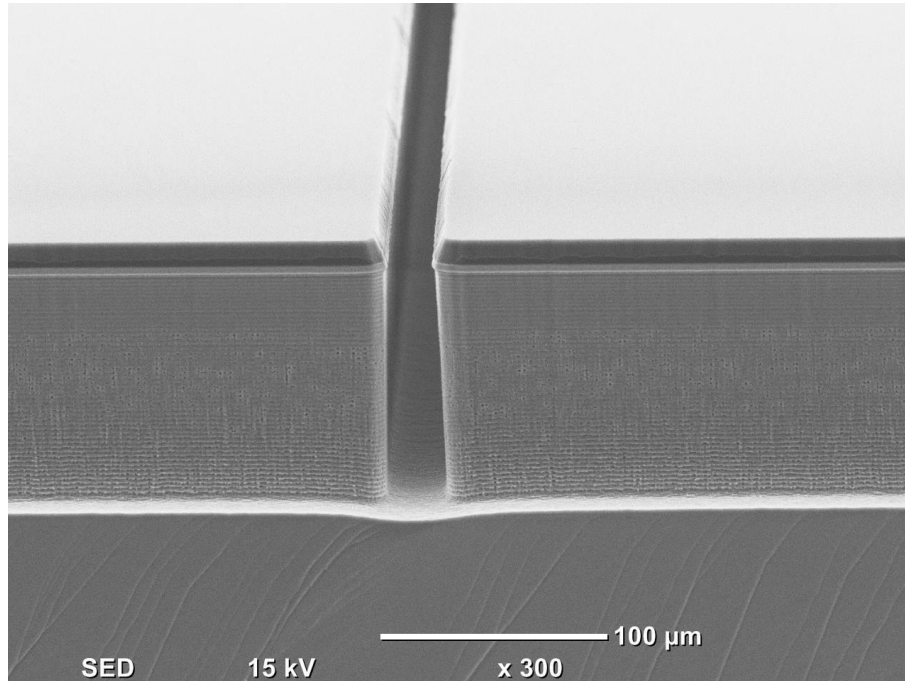
Si Layer Etching : Basic Specification

■ Etching Condition

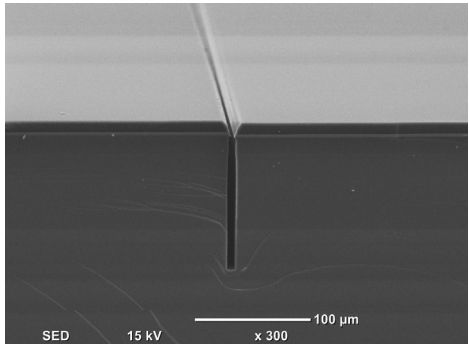
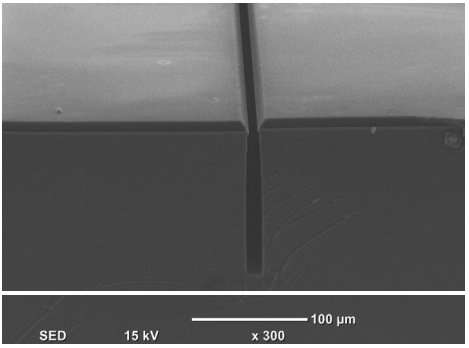
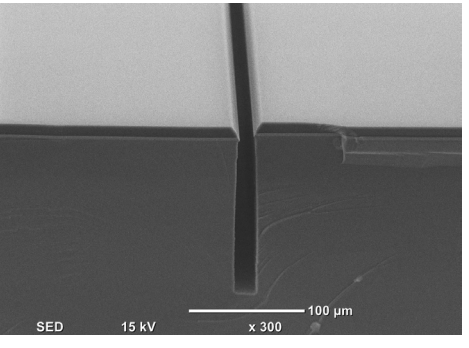
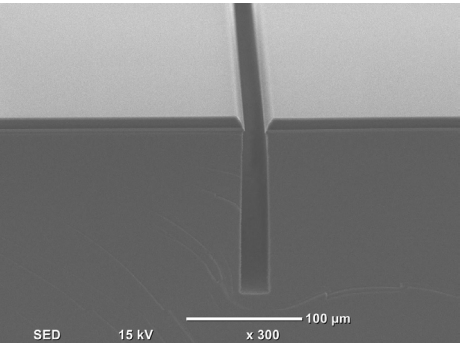
- Equipment : APX300-DM
- Etching gas : chlorine gas base -> fluorine gas base
- Etching time : 4 min. -> 8/5 min.

■ Etching Specification

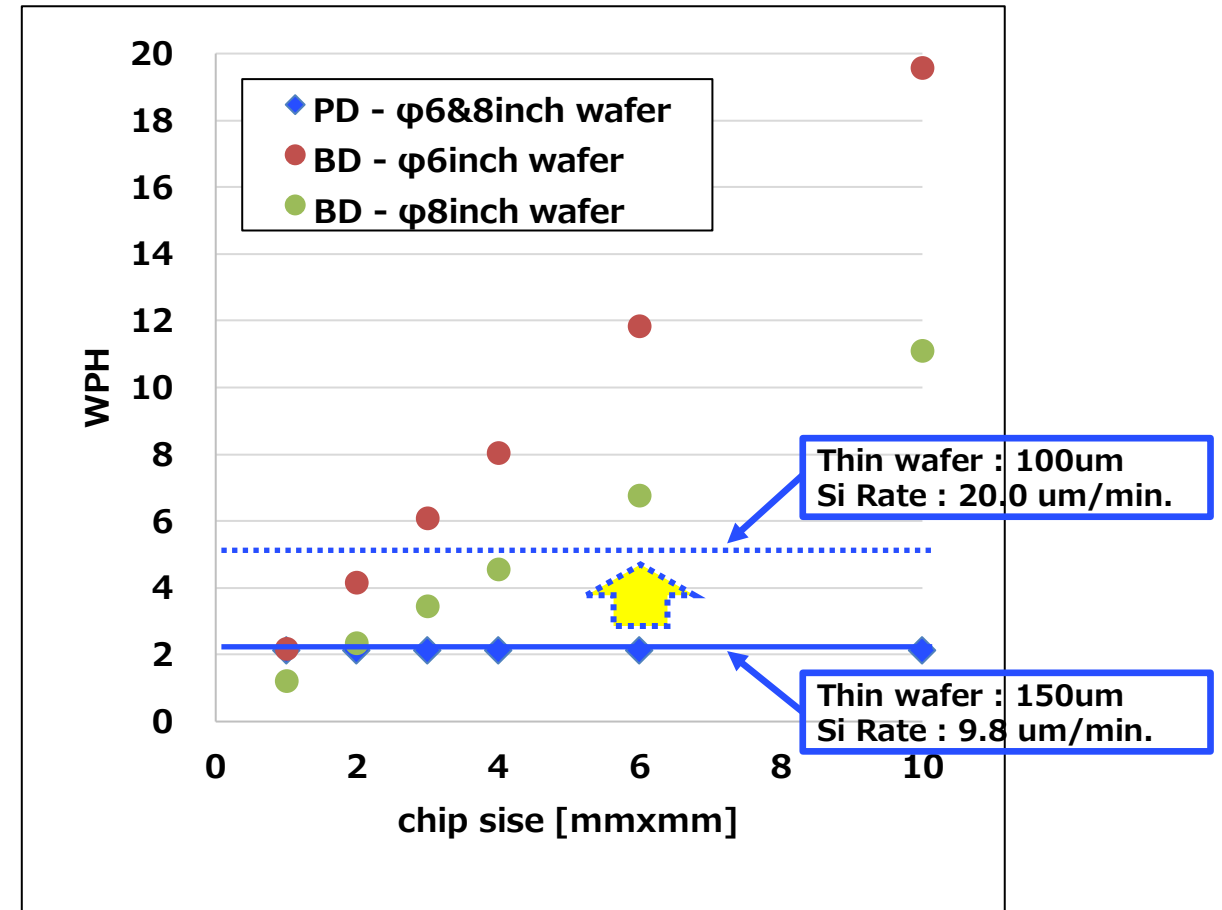
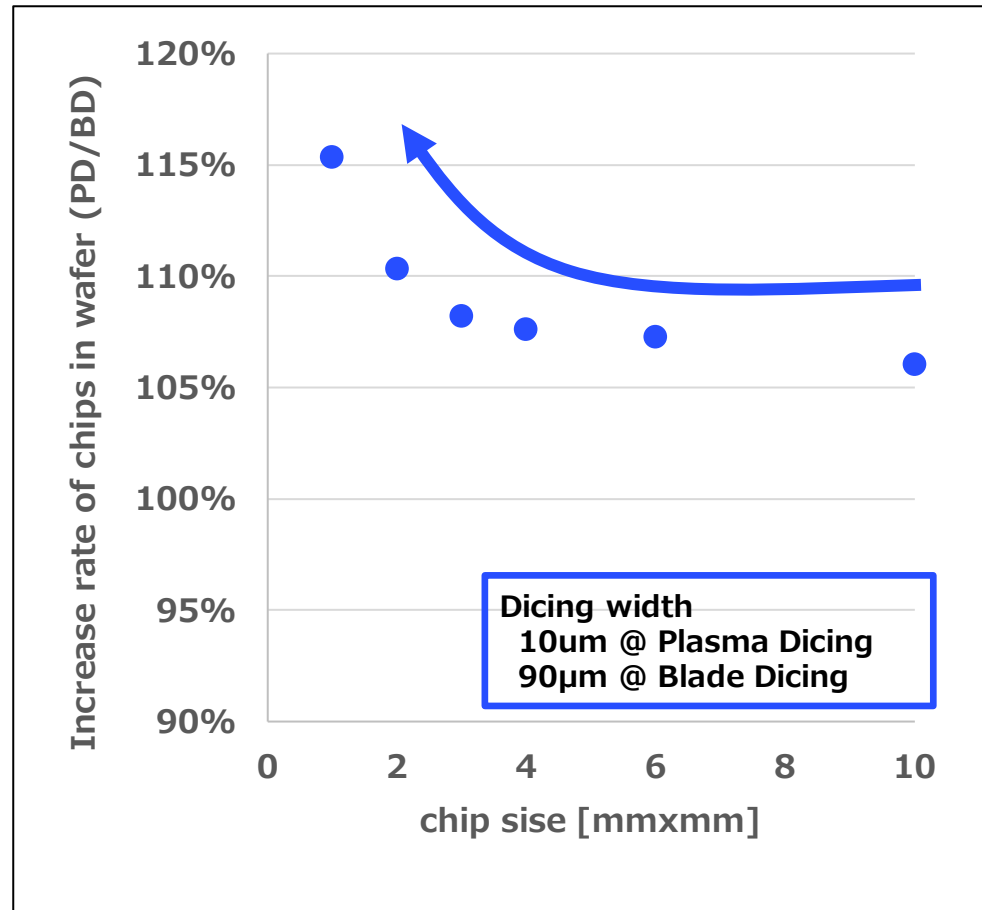
- Si Etching rate : 12.1 $\mu\text{m}/\text{min}$.
- Selectivity(Total etching depth / PR) : 82.4



Si Layer Etching : Etching rate dependency on dicing width

	Dicing width [μm]			
	5 μm	10 μm	15 μm	20 μm
SEM				
Si rate [$\mu\text{m}/\text{min.}$]	9.8	11.9	12.6	12.5
PR sel.	0.94	0.94	0.97	0.89

Increase Rate of PD/BD and WPH estimation



Dicing width reduction can increase the chip yield by about 15%

WPH should be improved by higher Si etching rate and thinner wafer thickness

Agenda

1. Introduction

- Panasonic Connect introduction
- Process Automation Business Division introduction


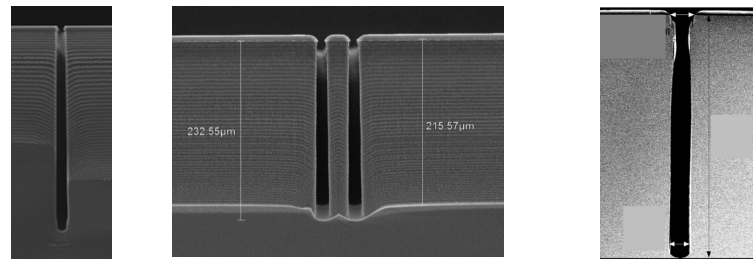

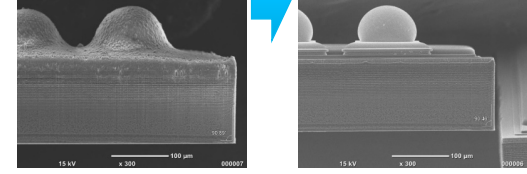
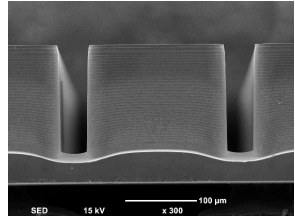
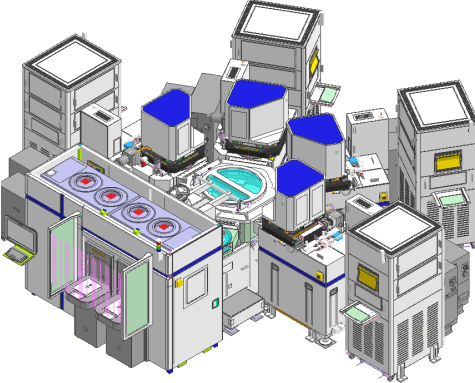
2. Plasma dicing for GaN on Si

- Background
- Total solution for GaN on Silicon device


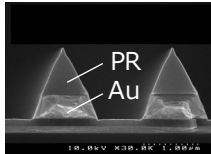
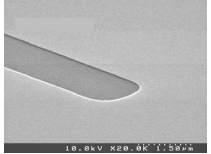
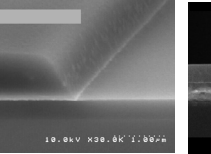
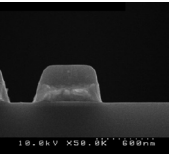

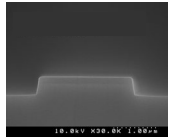
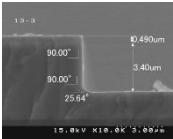
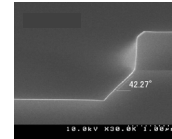
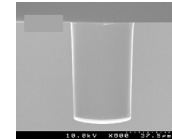
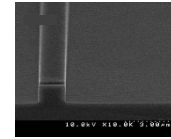
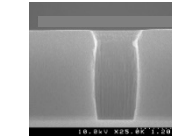

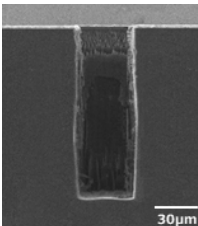
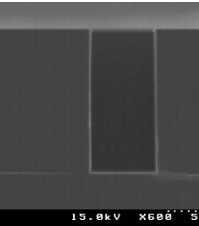
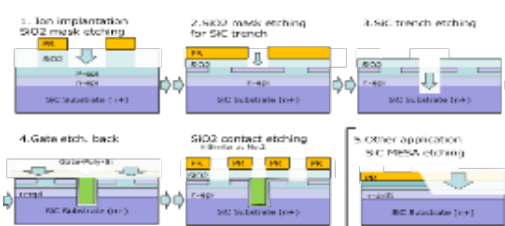
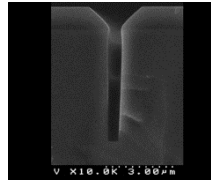

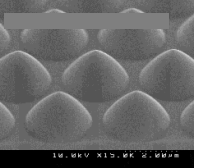
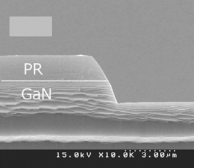
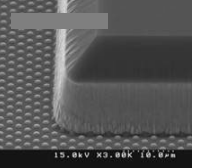
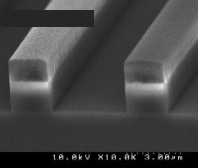
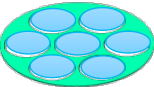
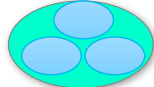
3. Equipment lineup for Dry Etching and Plasma Dicing

- Plasma dicing equipment
- Dry etching equipment
- Introduction of Plasma Dicing Demo Center

Plasma Dicing Solutions for Various Semiconductors

Machine/Specification	Applicable Device			
<p>APX300-DM</p> 	<p>Compound semiconductor, small chip, MEMS and R&D</p> <p>Material : Si / SiO2 / SiN / SiCN / GaAs / GaN etc.,</p> <p>Wafer size : φ4 ~ 8inch wafer with frame for φ8inch φ12inch wafer with frame for φ12inch</p> <p>Max. chamber : 1ch (single chamber type)</p>	<p>■ Narrow street etching</p> <p>Si dicing 5um X 175um Si double line 10um X 220um GaAs Plasma dicing 15um X 160um</p>  <p>■ Characteristic plasma etching</p> <p>Ball bump/Device-layer/Si Si with DAF</p>  <p>After Plasma dicing After Washing</p>  <p>GaAs smooth sidewall</p> 		
<p>New APX300-PD</p> 	<p>Memory (DRAM, NAND), Image sensor, Logic</p> <p>Material : Si / SiO2 / SiN / SiCN etc.,</p> <p>Wafer size : φ8~12inch wafer with frame for φ12inch</p> <p>Max. chamber : 4ch (multi chamber type)</p>			

Dry Etching Solutions for Compound Semiconductors

Machine/Specification	Applicable Device	
 <p>New APX300-S FS-ICP</p>	<p>Long MTBC*1 ICP Process for Non-volatile materials Au / PZT / Pt for Piezo MEMS Magnetic film, Metal wiring for MEMS and Magnetic sensor Capacitor for compound</p>	<p>*1 MTBC : mean-time-between-clean</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Au</p>  </div> <div style="text-align: center;"> <p>NiCo</p>  </div> <div style="text-align: center;"> <p>NiFe</p>  </div> <div style="text-align: center;"> <p>Pt</p>  </div> </div>
 <p>APX300-S MSC-ICP</p>	<p>High Precision Multi-Spiral-Coil ICP Process GaAs High Frequency / Optronics (Recess, GaAs MESA, VIA) GaN High Frequency / Optronics (Recess, MESA, Isolation) InP Optronics (MESA, VIA) SiC Power (MESA, Trench, Etch. Back) Passivation (SiO₂, SiN, BCB, PI, etc.)</p>	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>GaAs MESA</p>  </div> <div style="text-align: center;"> <p>GaN Isolation</p>  </div> <div style="text-align: center;"> <p>SiC MESA</p>  </div> <div style="text-align: center;"> <p>GaAs VIA</p>  </div> <div style="text-align: center;"> <p>InP MESA</p>  </div> <div style="text-align: center;"> <p>BCB</p>  </div> </div>
 <p>APX300-S BM-ICP</p>	<p>High Density Plasma Process Si / SiC VIA for GaN HEMT All SiC trench process (SiO₂ mask, Trench, Etch-Back)</p>	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>SiC VIA</p>  </div> <div style="text-align: center;"> <p>Si VIA</p>  </div> <div style="text-align: center;"> <p>SiC total flow</p>  </div> <div style="text-align: center;"> <p>SiC Trench</p>  </div> </div>
 <p>APX300 Batch processing</p>	<p>Batch Processing for Mass-production LED (PSS, GaN MESA, GaN Isolation, SiO₂, etc.) SiO₂ mask etching, etc.</p>	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>PSS</p>  </div> <div style="text-align: center;"> <p>GaN MESA</p>  </div> <div style="text-align: center;"> <p>GaN Isolation</p>  </div> <div style="text-align: center;"> <p>SiO₂ Mask</p>  </div> </div> <div style="display: flex; justify-content: center; margin-top: 10px;"> <div style="text-align: center; margin: 0 20px;">  <p>Φ4" x 7</p> </div> <div style="text-align: center; margin: 0 20px;">  <p>Φ6" x 3</p> </div> </div>

Demo Centers in Osaka

■ Plasma Dicing Demo Center



Location: Osaka, Japan

Floor Space: 230m²

Wafer size: Φ 200mm up to Φ 300mm

Equipment: Plasma Dicer, Plasma Cleaner, Back-grinder, Photo-lithography, Laser Patterning, Measurement tools, etc.

■ Dry Etching Demo Center



Location : Osaka, Japan

Floor Space : 275m²

Wafer: Up to Φ 200mm or 340mm tray

Equipment: Dry Etcher, Plasma Cleaner, Measurement tools, etc.

Panasonic provides and supports customers with the “Total Solutions Approach” for Plasma Dicing and Dry Etching, together with our partners.

Conclusions and Acknowledgments

Plasma dicing for GaN on silicon

Panasonic can propose Plasma Dicing technology to singulate GaN on Silicon wafers.

Panasonic developed and demonstrated suitable process flows for GaN on Silicon wafers :

1. Photo-lithography :

photo-lithography with / without metal ring and tape can be performed.

2. Plasma Dicing :

- GaN multi layer can be fully cut by using Chlorine-based gases.

- Si layer also can be etched by using Flourine-based gases in the same chamber for GaN layer.

Panasonic continue to improve Plasma Dicing technology for GaN on Silicon and intend to expand its application to other compound semiconductors such as GaN, etc.

- High etching rate,

Acknowledgments:

Thank you very much to EV Group for their cooperation, and to several other chemical manufacturers.

Contact Information

Please visit us at our booth.

For more information in Europe, please contact our sales office:

Panasonic Connect Europe GmbH

Caroline-Herschel-Strasse 100
85521 Ottobrunn
Germany

(Near Munich)

Panasonic CONNECT



James Weber

Senior Business Development Manager
Electronics Manufacturing Solutions

james.weber@eu.panasonic.com



Visit our website

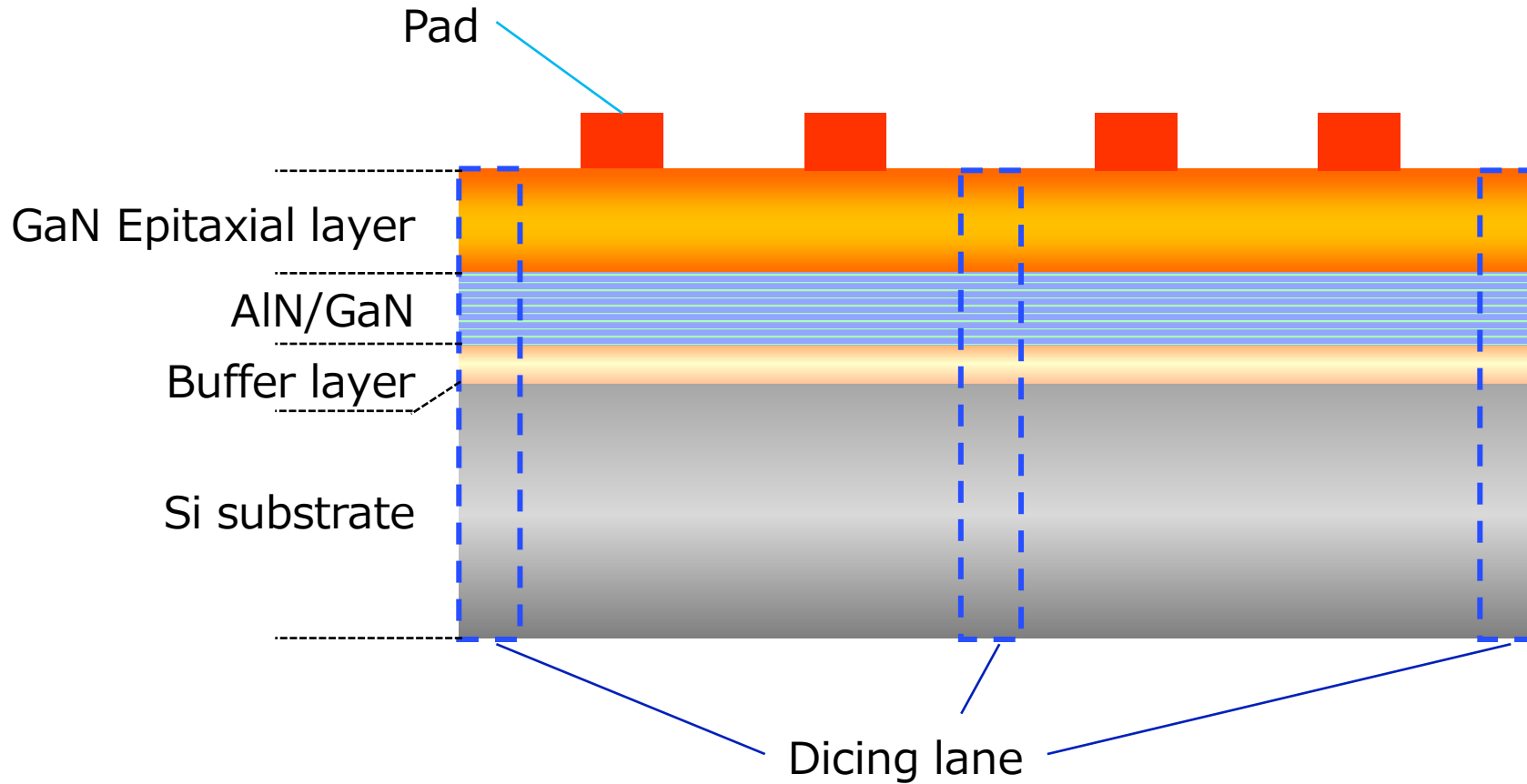
[Panasonic Microelectronics](https://www.panasonic.com/europe/microelectronics)



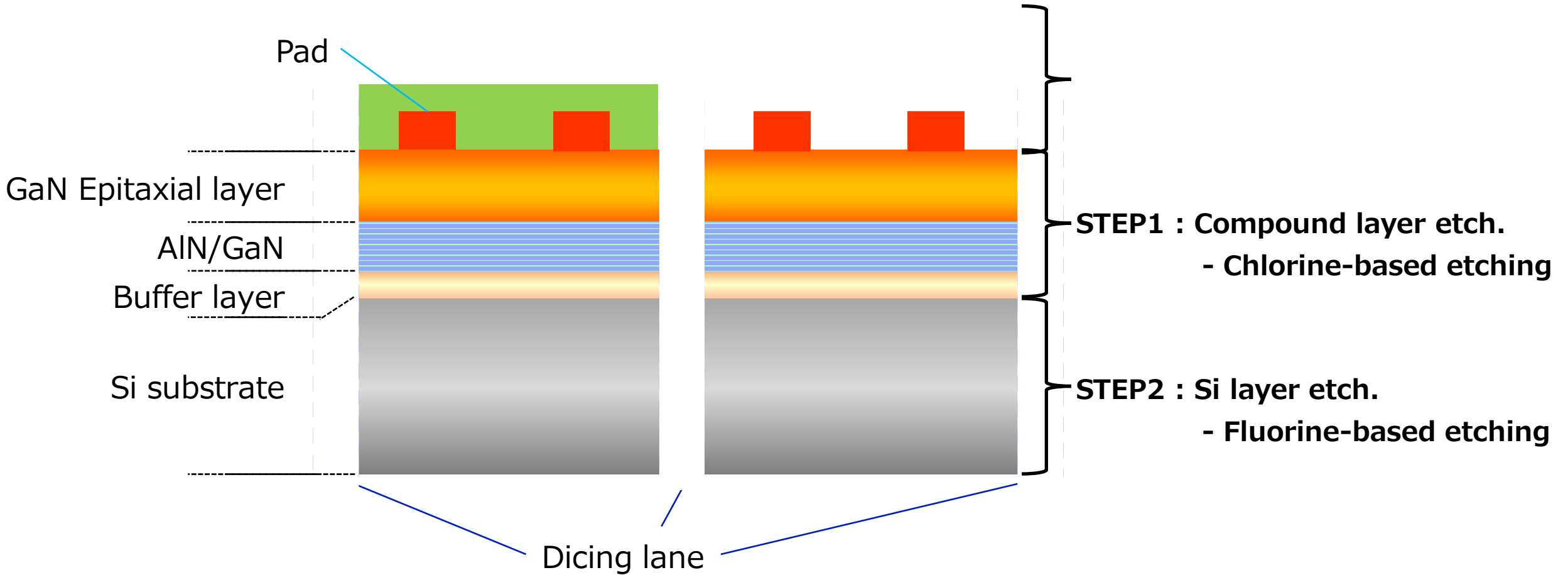
Panasonic
CONNECT

Plasma dicing for GaN on Silicon

Initial condition



Plasma dicing for GaN on Silicon



Plasma dicing for GaN on Silicon

