Clas-SiC WAFER FAB

Strengthening Supply Chains

Clas-SiC: The UK's only Commercial Power SiC Wafer Fab

David Clark, Technology Manager

From concept to prototype to manufacture

PE INTERNATIONAL CONFERENCE ANGELTECH

Introduction to Clas-SiC

- Clas-SiC Wafer Fab is the world's first dedicated, open, 150mm, pure-play foundry to manufacture Silicon Carbide power devices
- Clas-SiC combines the best & most experienced talent in the industry, with state of the art Silicon Carbide tools & processing, making Clas-SiC a unique start-up
- Clas-SiC offering provides fast prototyping cycle times for SiC wafer fabrication to accelerate R&D and time to market for new device designs through process design kits (PDK) and a library of "off the shelf" Process Module IP.

Available SiC Process Design Kits
650-2500V JBS/MPS **Diode** PDK
1200V **MOSFET** PDK
1700V **MOSFET** Alpha PDK
3300V **MOSFET** Alpha PDK

SiC Device Market:
The projections and the experience

- The Yole report of 2022 forecast the power SiC device market would be >$1.5BN, having grown by >40% over 2021, CAGR of 37% to 2027

- Over the last year Clas-SiC have seen:
  - Revenue increase by > 300%, dominated by MOSFET's
  - Number of active customers increase by 100%
  - Moving from 5 day operation to full 24/7, 6 months earlier than forecast

- Anecdotal reports in the industry are that:
  - SiC device wafer fabrication is at premium, particularly for custom devices
  - Long queue times are being experienced at pure-play foundries
  - Demand is being driven predominantly by the EV market

SiC Wafer Fabrication: Constraints in Raw Material Supply

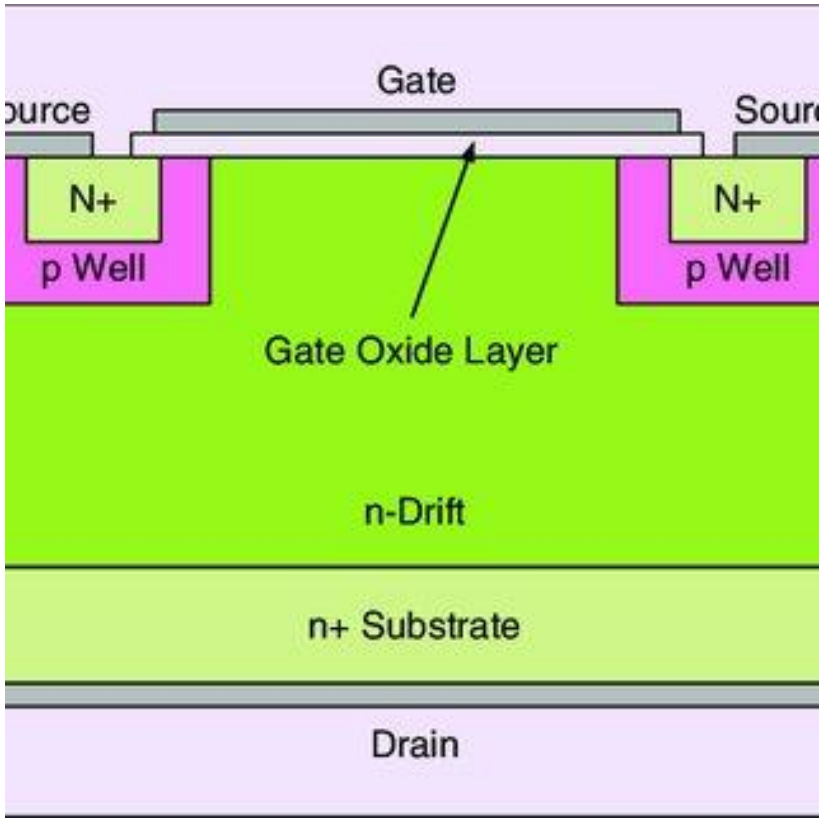
- Scaling up SiC Wafer Production is currently greatly limited by availability of SiC substrates
  - Vendors are requiring order coverage for 12 months ahead
  - New vendors are coming onto the scene but their capacity is quickly being secured
  - Good supply chain partnerships and diversification of supply base is essential to maintain supply
  - The alternative is to bring the supply in-house and some bigger SiC Wafer Fab's are doing this

- Scaling up SiC epitaxy is also a challenge, but is secondary to the substrate challenge
  - Existing epi houses are aggressively increasing capacity
  - Again, good supply chain partnerships are essential to maintain supply
  - A common solution for larger fab's is to bring SiC epitaxy in-house

Further from Epi Supply Challenges

- The forecast for the industry is that the trend towards higher bus voltages will continue
  - 650V devices are being displaced by 1200V
  - 1700V devices can be expected to displace 1200V
  - But will this continue?

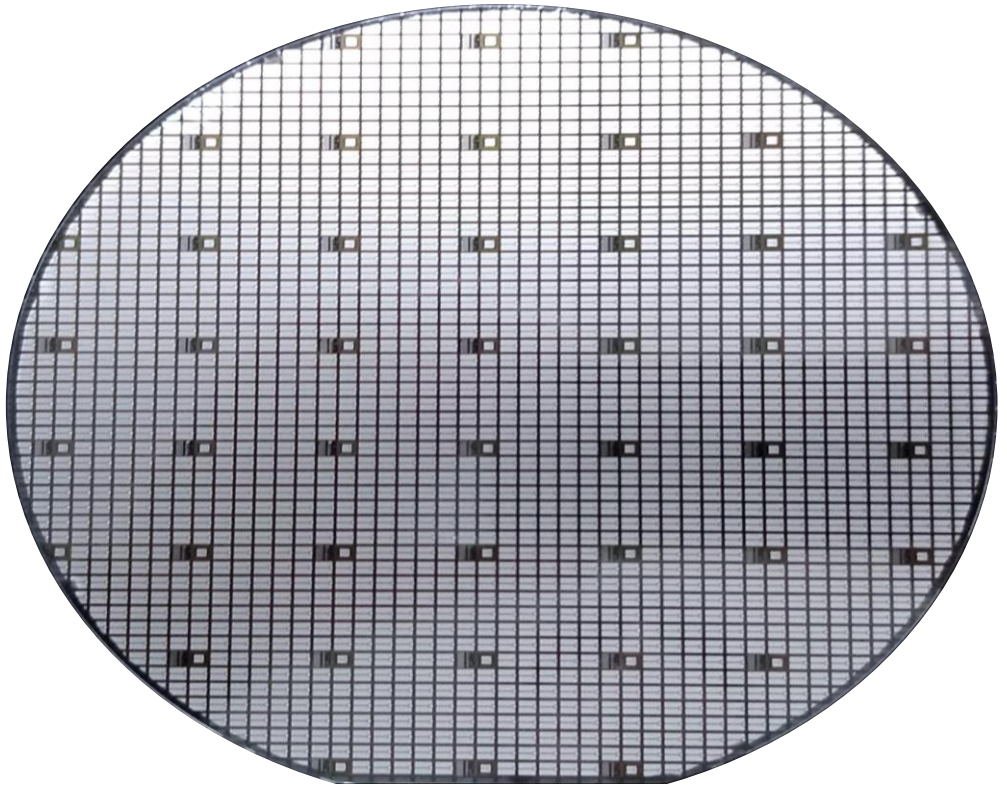
- SiC epitaxy is a challenge in scaling this up
  - The higher voltages need thicker n-drift epitaxy
  - But small epi defects magnify with epi thickness
  - So improvements in thick epitaxy quality are required to provide economic die yields



Scaling Up by increasing SiC Wafer Size

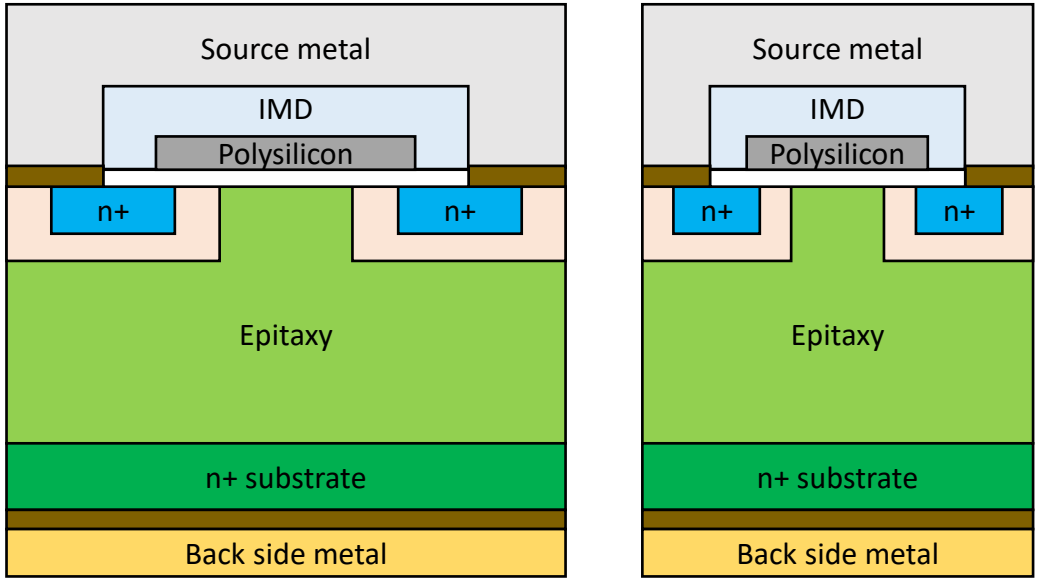
- Scaling the wafer size from 4” to 6” increased the wafer area by a factor of 2.25
  - Wafer thickness was maintained at 350µm
  - The incoming wafer/epitaxy price did increase
  - But wafer fabrication costs remained the same
  - So cost/die was reduced

- Scaling the wafer size from 6” to 8” would be expected to give similar benefits
  - But wafer area increases by a factor of 1.77
  - And wafer thickness increased to 500µm
  - So cost efficiency of the 8” transition is not as good
  - Also, availability of 8” wafers is very limited, with restricted supply forecast until 2025
  - The 6”/8” transition is predicted to be significantly slower than for 4”/6”



Scaling Up by Obtaining more Die/Wafer

- The obvious way to scale up SiC device fabrication is by producing more die for a given wafer size
- Reducing specific on resistance is the key challenge, and this can be achieved by one or more of:
  - Shrinking layout pitch

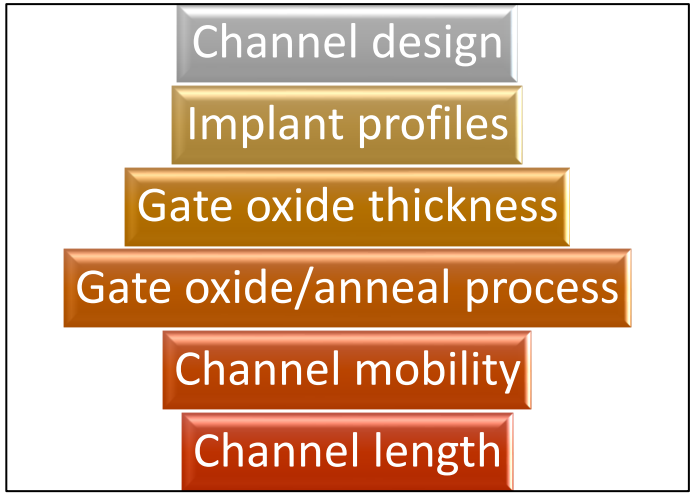


Scaling Up by Obtaining more Die/Wafer

- The obvious way to scale up SiC device fabrication is by producing more die for a given wafer size

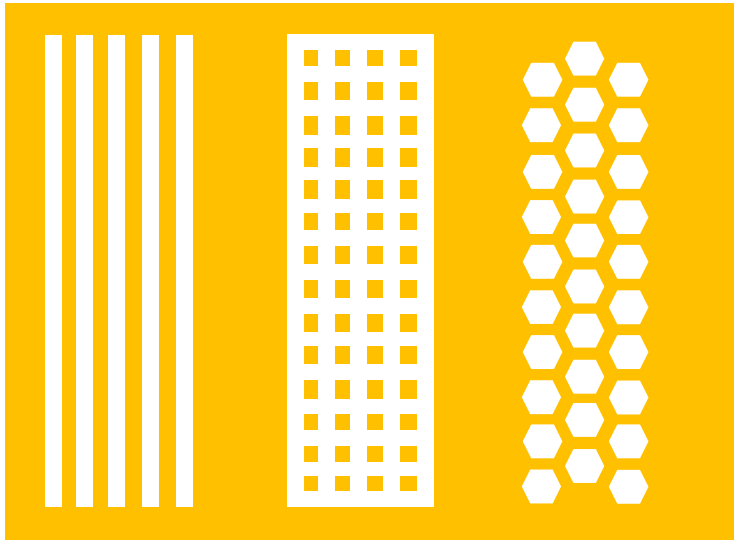
- Reducing specific on resistance is the key challenge, and this can be achieved by one or more of:
  - Shrinking layout pitch

  - Re-engineering the transistor for higher current gain



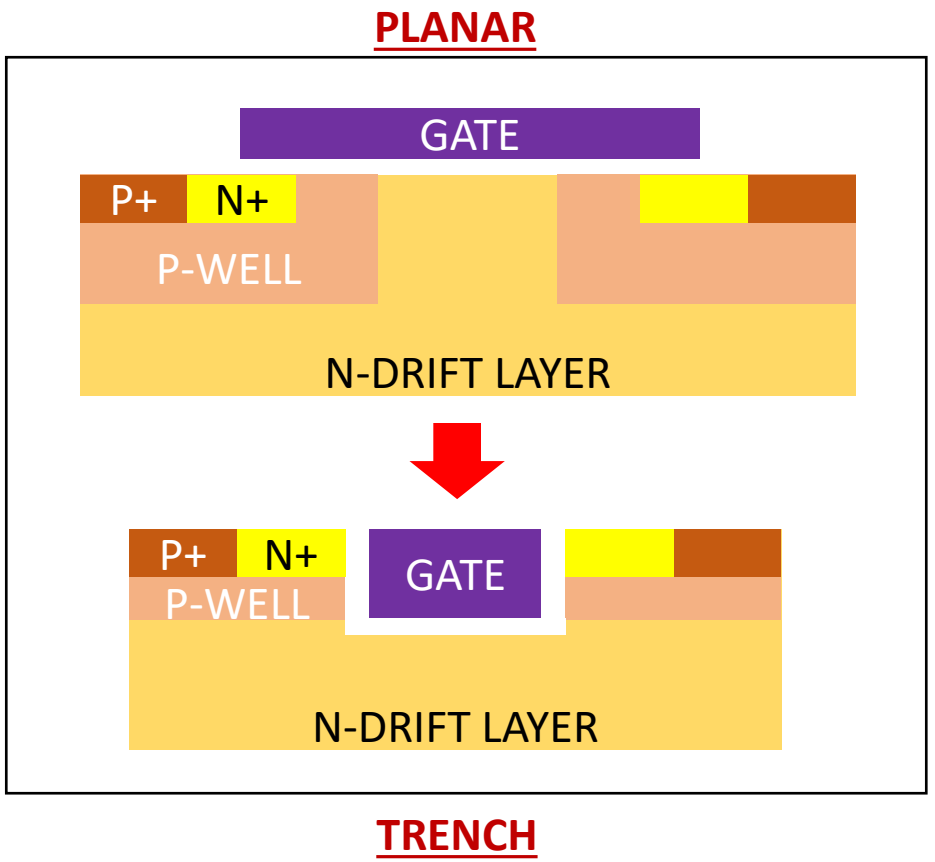
Scaling Up by Obtaining more Die/Wafer

- The obvious way to scale up SiC device fabrication is by producing more die for a given wafer size
- Reducing specific on resistance is the key challenge, and this can be achieved by one or more of:
  - Shrinking layout pitch
  - Re-engineering the transistor for higher current gain
  - Using a more space-efficient layout technique



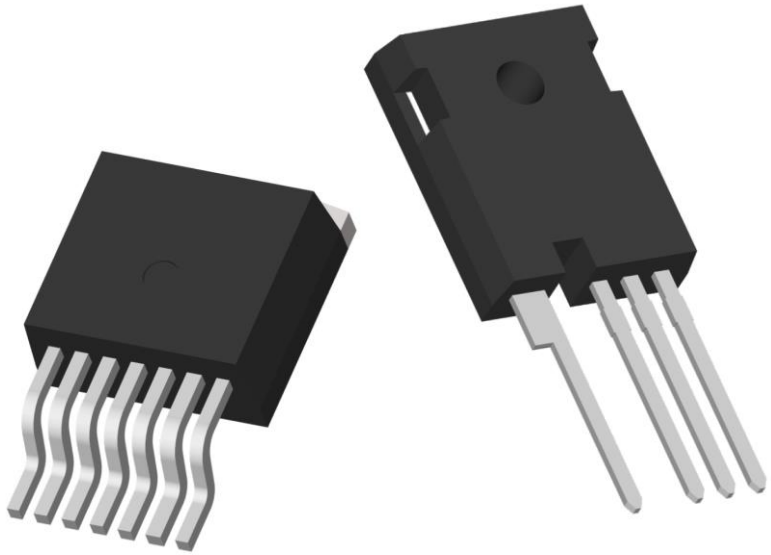
Scaling Up by Obtaining more Die/Wafer

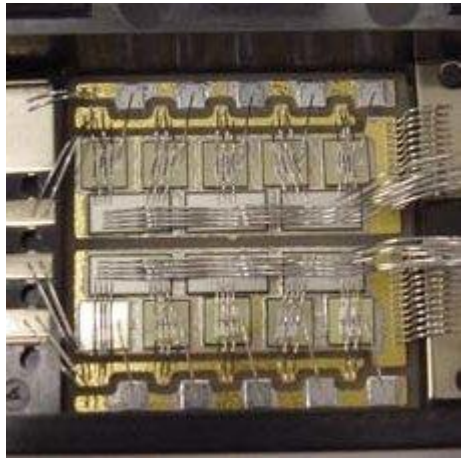
- The obvious way to scale up SiC device fabrication is by producing more die for a given wafer size
- Reducing specific on resistance is the key challenge, and this can be achieved by one or more of:
  - Shrinking layout pitch
  - Re-engineering the transistor for higher current gain
  - Using a more space-efficient layout technique
  - Moving from planar to trench technology
  - But trench is more technically difficult and more expensive to manufacture, so has been slow to be widely adopted
  - The trend however is likely to be towards a more widespread adoption of trench technology
  - But the advantages of trench are less for higher voltage devices
  - So we can expect planar and trench to co-exist to some extent



Innovation required by the Supply Chain

- Closer integration of power semiconductors with modules is needed to enable smaller, lighter, cheaper systems
- Initially, plastic packaged die were the normal manifestation for SiC MOSFET's – eg TO-247, TO-263
- To reduce switching losses, the trend is now firmly towards embedding bare SiC die within modules
  - Custom layouts to support die/module integration are therefore required
  - Custom metal finishes – eg Ag, Au, Cu are also required
  - But these are not commonly available off the shelf
- Other innovations we can expect to see include
  - On-MOSFET integration of temperature and current sensors
  - On-MOSFET integration of Schottky diodes





Source: AFRL

Clas-SiC Involvement in Advanced UK Projects

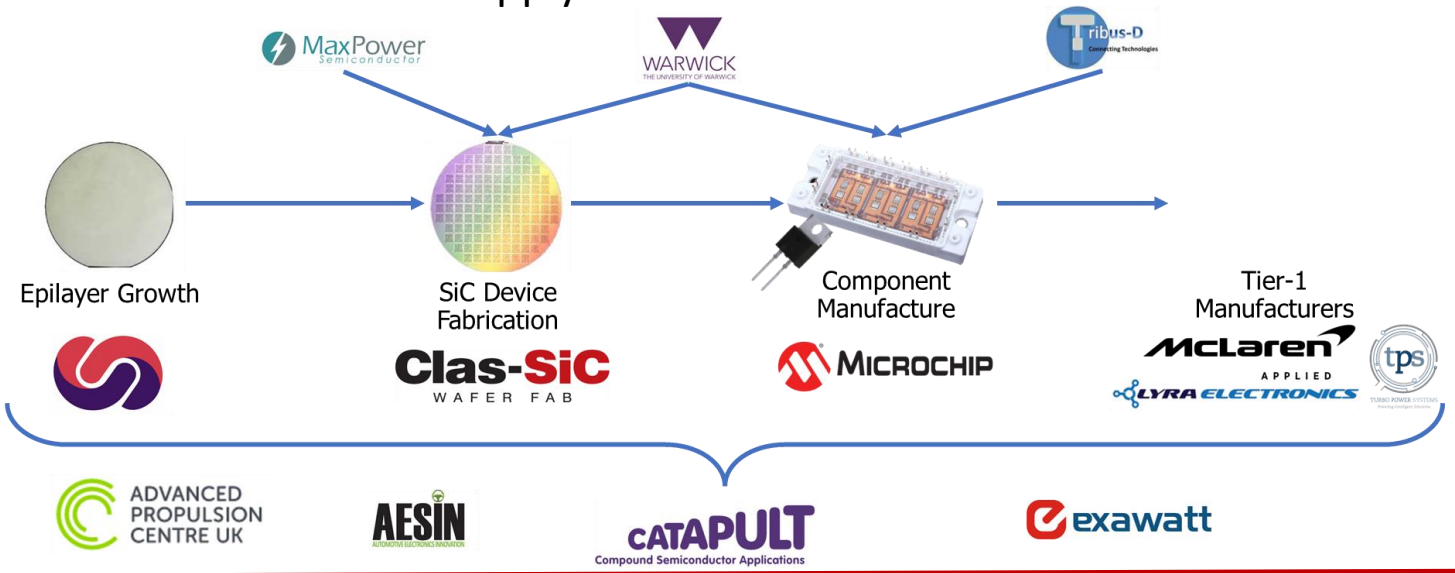
CELERITAS - Ultra-fast charging batteries for EV's and FCEV's

Partner	Role
tae Power Solutions Engineering	Lead Partner Battery Design & development Integrated DCDC, BMS & Charger interfaces, design & development
amte power	Cell development & manufacture
bp	Immersive coolant supplier Coolant analysis and module /pack test facilities provider
tae Power Solutions Manufacturing	Battery pack assembly & EOL Test
Clas-SiC WAFER FAB	Semiconductor manufacturer 1200V MOSFET for higher voltages
BMW	Provide OEM focus and requirements for FCHEV

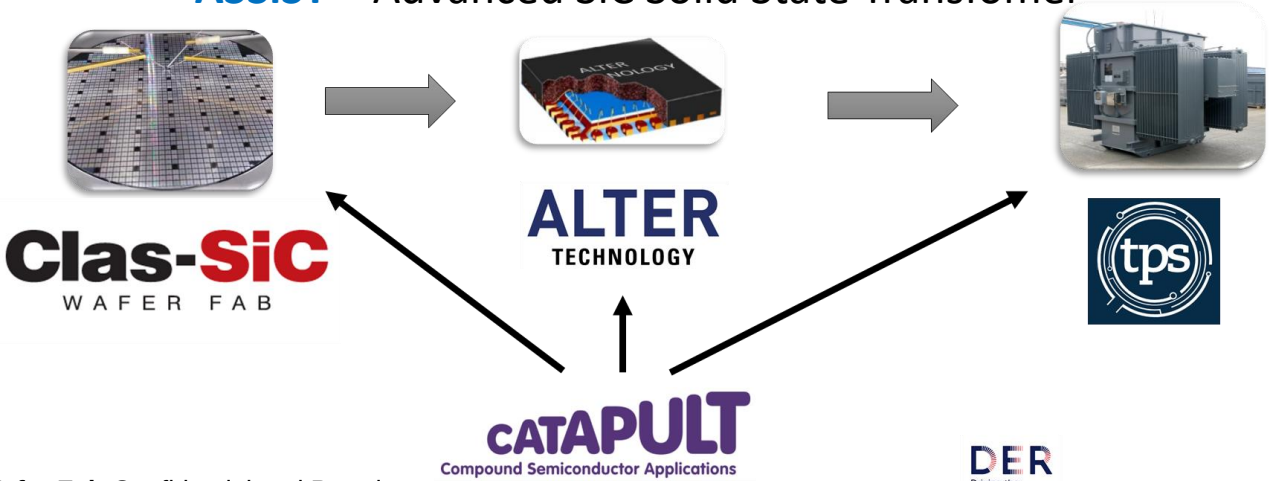
Focus Group: Nissan and Aston Martin

ADVANCED PROPULSION CENTRE UK

ESCAPE – End-End Supply Chain for Automotive Power Electronics



ASSiST – Advanced SiC Solid State Transfomer



DER Driving the Electric Revolution Industrialisation Centres

Summary of Opportunities for SiC

- SiC Power Device Market >$1.5BN in 2022 and CAGR of 34% forecast to 2027
  - Huge opportunities in EV applications, especially as bus voltages increase to 800V and possibly higher
  - SiC is key to power converter efficiency
    - Same current at higher voltages - > more power
    - Same power at higher voltages -> less i2R losses
    - Same power at higher frequency -> smaller, lighter magnetics
    - Although SiC devices cost more than silicon, they do contribute to lower system cost and improved system performance
  - Fantastic opportunities also in wind, solar, traction, aviation and power transmission
    - Some of these are lower volume but high margin, so an interesting market space

Clas-SiC
WAFER FAB

Thank you

david.clark@clas-sic.com

PE INTERNATIONAL CONFERENCE
ANGELTECH

From concept to prototype to manufacture