PUREON

Rapid Thinning for SiC Wafers for Sustainable and Cost-Effective Wafers

PE International Conference, Brussels, 2024

April 16th 2023, Dr. Ravi Bollina

SiC wafering process

Our success story

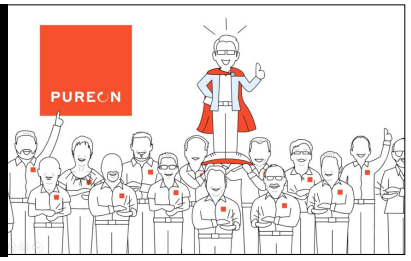
- **1970** Invention of the first stable diamond suspension
- **1995** Invention of GAF (guaranteed agglomerate-free) liquid diamond
- **2008** Introduction of ULTRA-SOL STD slurries for SiC wafer polishing
- **2014** Launch of SQUADRO, the new generation fine grinding pad
- **2016** Launch and patenting of IRINO composite pad
- **2022** US patent for next generation ULTRA-SOL STD slurry for SiC wafer polishing

3rd
Generation Family Business

7
Subsidiaries in USA, Europe & Asia

1952
Founded

20+
years of experience in SiC market



The building blocks of perfect surfaces - A wide, customized product range

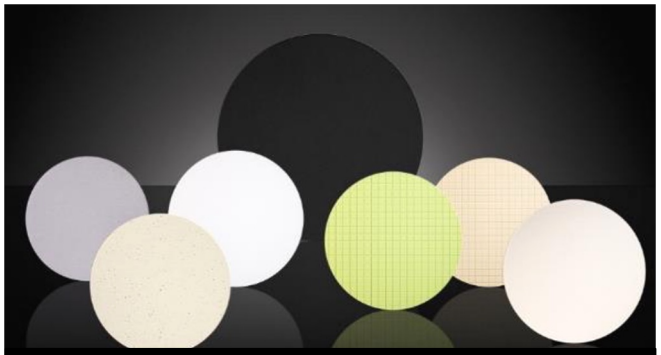
Diamond powders and Liquid Diamond

Lapping and polishing slurries

Compounds

Wafering, slicing, wire sawing

Grinding pads

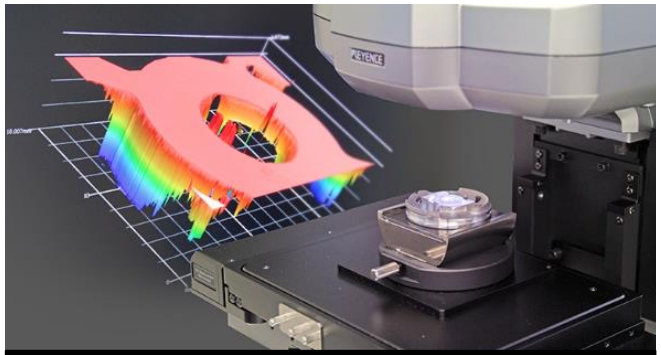


Polishing pads

The building blocks of perfect surfaces – Inhouse R&D and Surface Lab

From conception through process development to sharing know-how with our customers: Application expertise made in our Surface Lab.

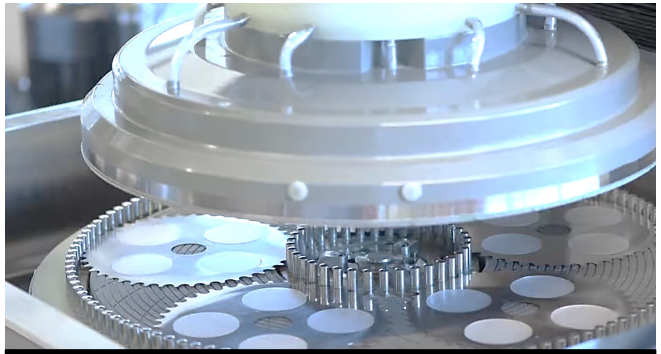
Advanced analytics



Surface and 3D measurement systems

Available for visits

Located at our headquarters in Lengwil, CH

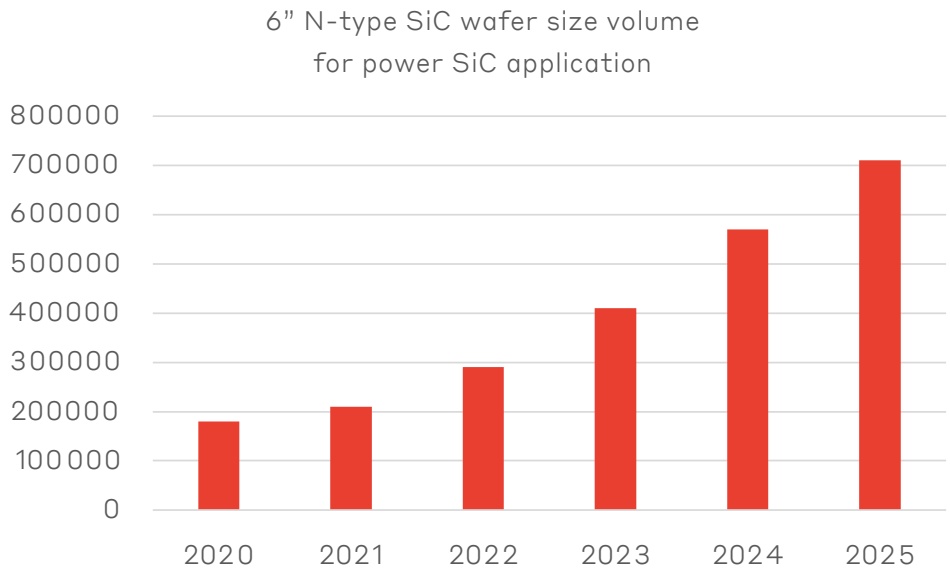


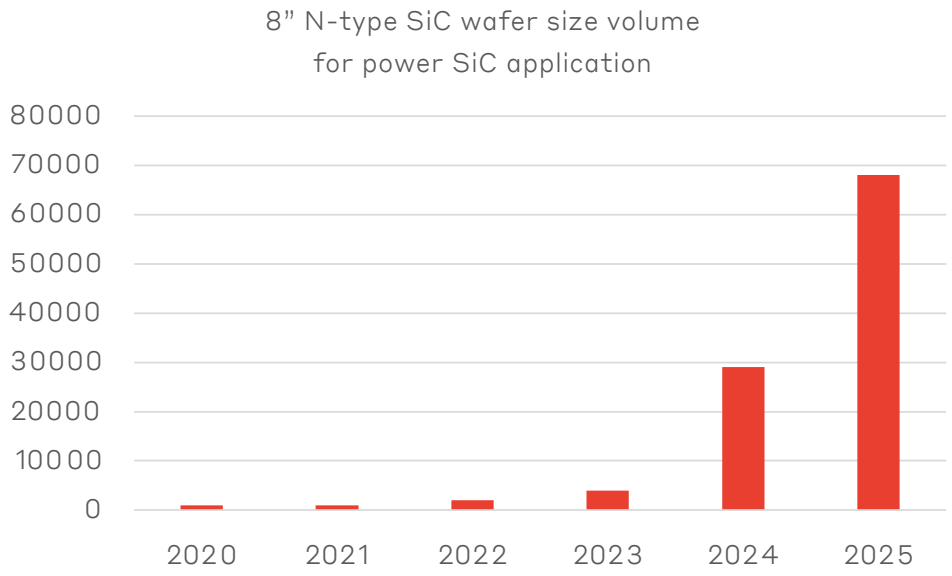
State-of-the-art machinery

SiC wafering process

SiC wafer requirement roadmap till 2025

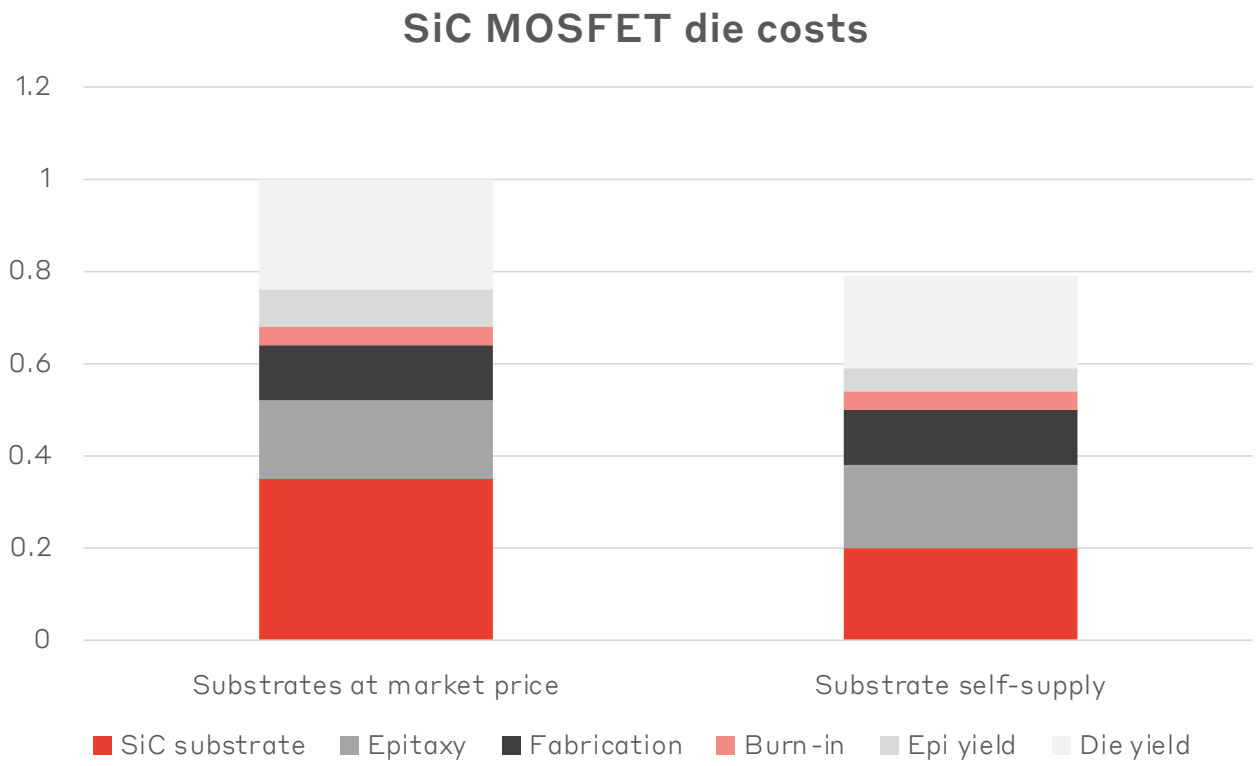
- Growing SiC wafers demand anticipated for the next decade
- 200 mm wafers will become increasingly available only in 2 – 4 years from now





Source: Yole Développement, 2021

SiC substrate cost is CRITICAL for lowering the die costs

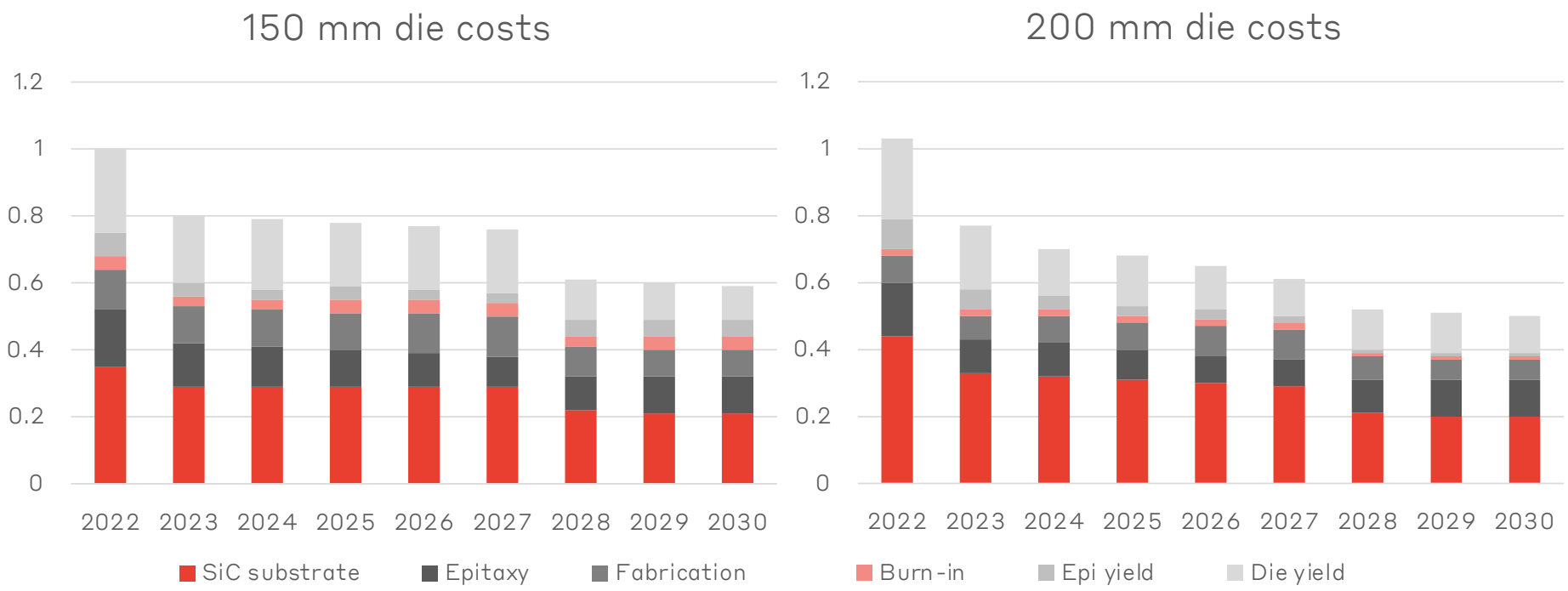


SiC Substrate
= 25 – 40%
of the die cost

Source: PGC consultancy

SiC substrate cost - WILL NOT GO AWAY

A breakdown of the costs that contribute to the total projected 150 and 200-mm die costs



The baseline results are further expanded to include their year-on-year contributions. The negative effect of yield on the early 200 mm wafers can be seen, with this being a major portion early in their adoption. By 2030, the lower fabrication costs per die of the larger 200 mm substrates are fully evident in the data.

Source: PGC consultancy

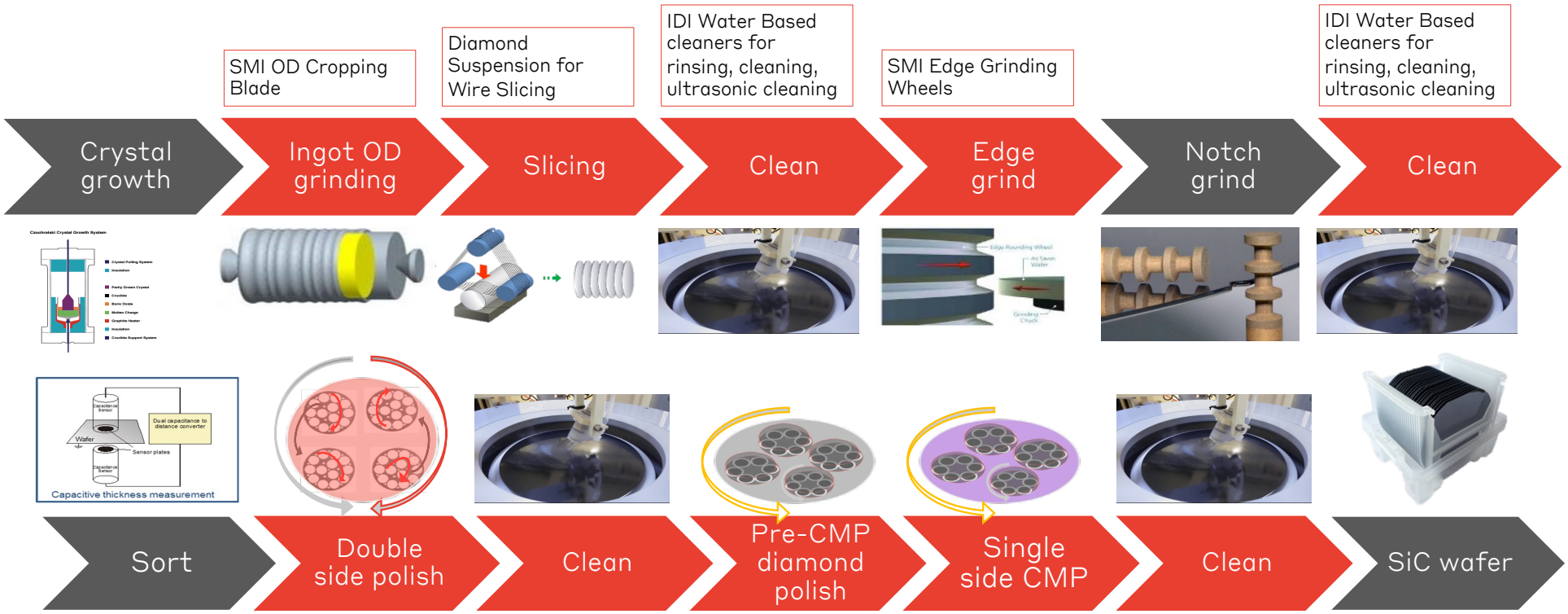
SiC substrate cost – WILL NOT GO AWAY

- However, the share of the substrate at the total CoO will remain between 25 …. 30%.
- Enough of good reasons to constantly check the existing cutting and polishing processes to become:
  - Faster
  - Better
  - Cheaper
- This is where Pureon can help with 20+ years of experience in SiC-processing!!

SiC wafering process

Pureon solutions in the wafer manufacturing process

Pureon Participation



Legacy SiC wafer process

Current Common Batch Processing

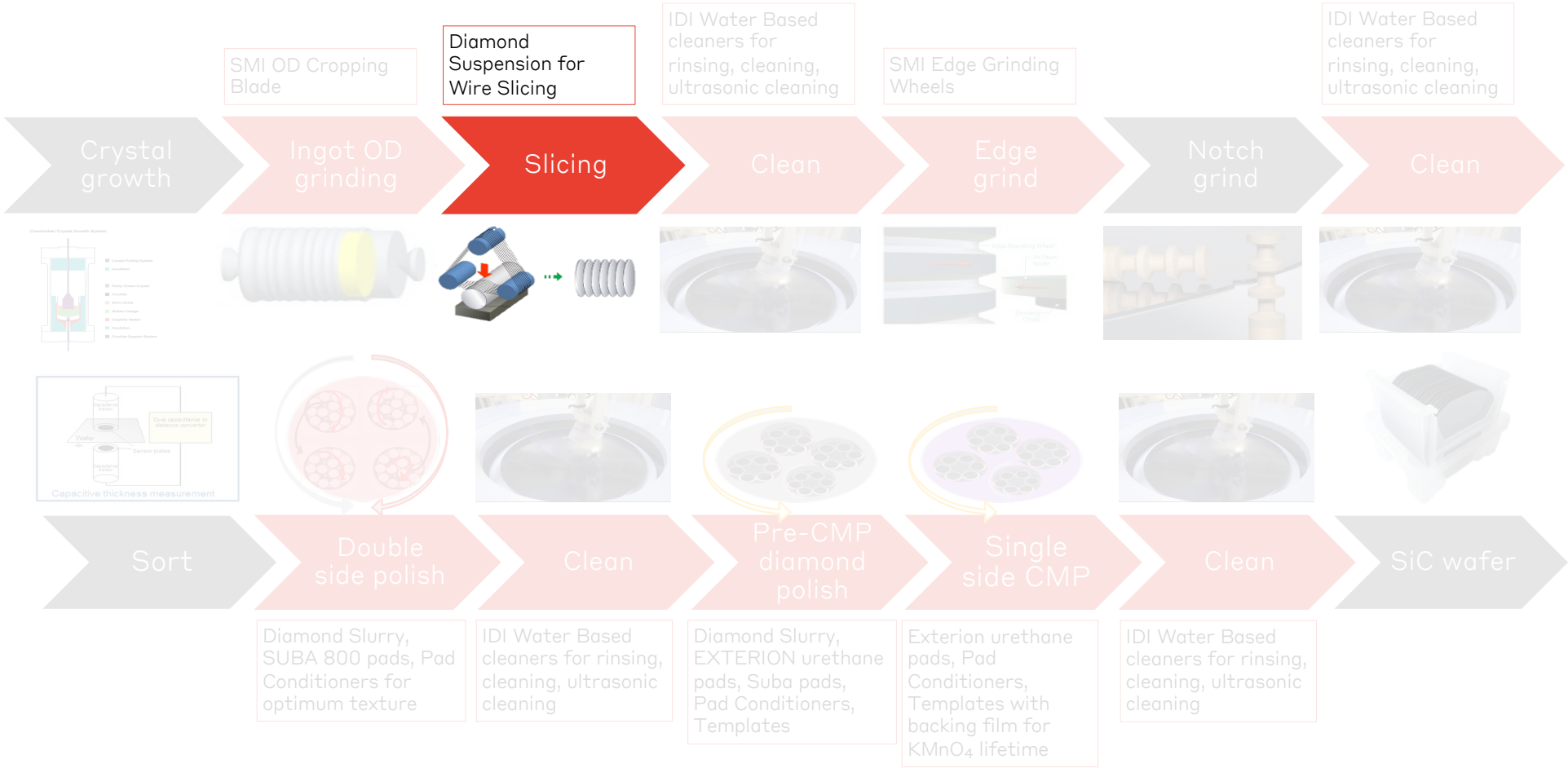
Process	Key Output	Pureon Consumable Solutions
Slicing	– Reducing the kerf loss – Reducing the thickness variation – Reducing Subsurface damage	– Wire – **Diamond-Slurry** – Diamond Wire
Double Side Polishing	– Removal from between 60-120 microns – Establish geometry: TTV, Bow, Warp and Thickness	– **Diamond-Slurry (Mono, Poly, Hybrid)** – **Composite Pads (Irino-Pro)** – **Polishing pads (MH, Suba, etc..)**
	– Minimize subsurface damage – Improves site flatness – Improves surface quality	– **Diamond-Slurry (Mono, Poly, Hybrid)** – **Non-woven Pads (Suba)** – **PU pads (MH)**
CMP Final polishing	– Provide an EPI-ready surface – Meet final wafer specifications	– **Permanganate based Slurry** – **Non-woven Pad (Suba)** – **PU pad (MH)** – **Templates and films**

* Pre-CMP is not part of legacy process, but additional step gaining interest

SiC wafering process

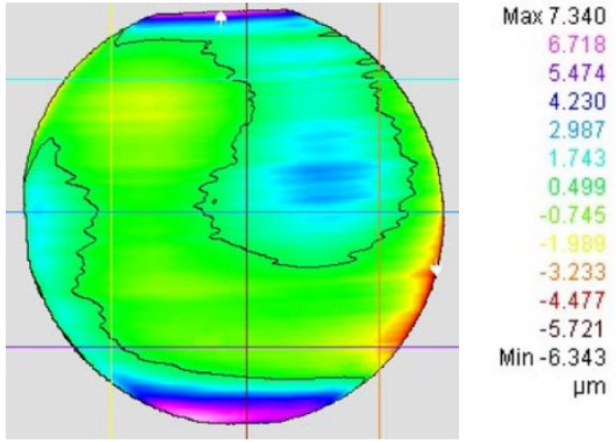
Pureon solutions in the wafer manufacturing process

Pureon Participation



Process step slicing

Process steps	Slicing
OEM tools	PW WaferTec DW288S4
General process parameters	Wire rate: 10 – 15 m/sec Tension: 20 – 40 N Flow rate: 1'800 l/h
Pureon solution	Slurry: WSG-56/500 Mono 3-6
Benefits vs POR	– Eco-friendly (no oil) – Improved geometry – Faster cutting times



Process solution for Wire Saw slicing with WSG-56/500 Mono 3-6

Range for Inputs

Parameter	Value
Wire feed rate	10 – 15 m/sec
Slurry flow	1'500 – 2'000 l/h
Tension	20 – 40 N
Rocking angle	3 – 12°
Stack length	150 – 300 mm
Diamond concentration	500 cts/liter
Wire diameter	100 – 160 µm (straight or structured)

Expected Outputs

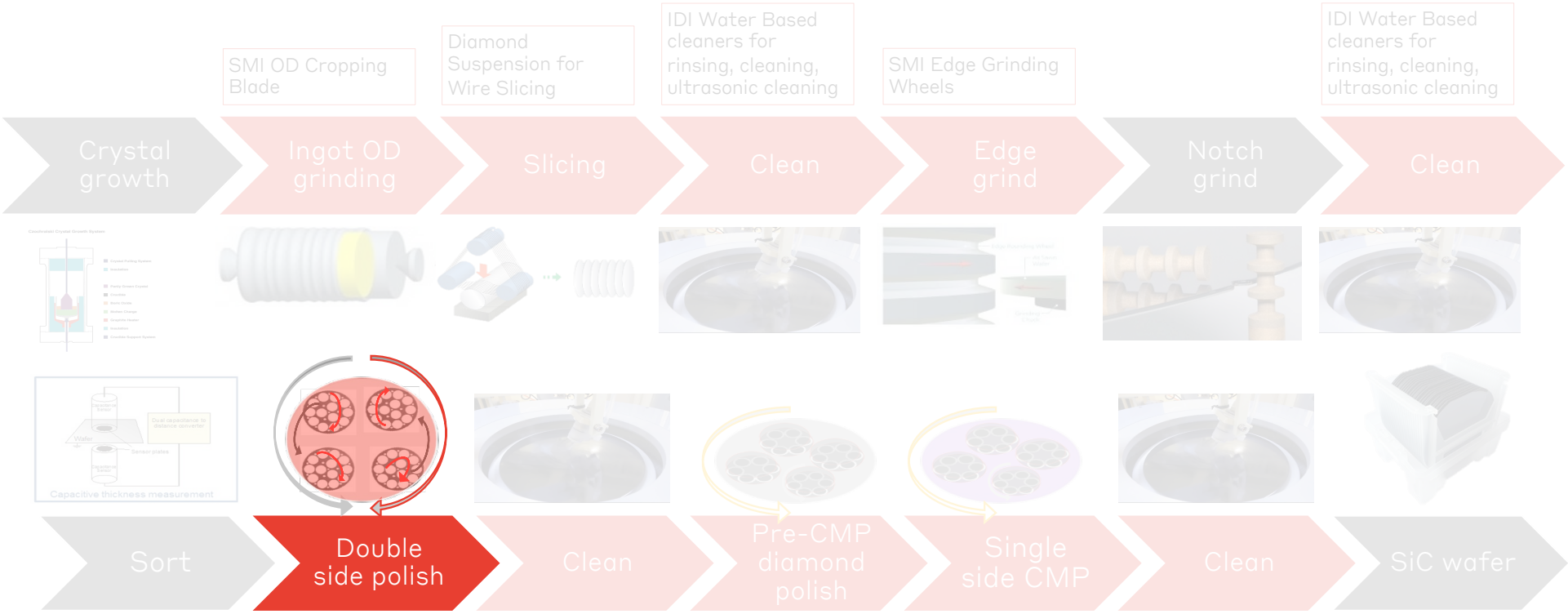
Parameter	Value
Cut time	60 – 120 hrs. for 150 mm wafers
Average bow	< 10 µm
Average warp	< 20 µm
Average TTV	< 6 µm
Lifetime of slurry	As per customer process
Kerf loss	115 – 175 µm

Process outputs are dependent on diameter of ingot, wire, and stack length.
Also, concentration of diamonds.

SiC wafering process

Pureon solutions in the wafer manufacturing process

Pureon Participation



Diamond Slurry for SiC wafer thinning- DMP 1

Process steps	DMP1
Customer specifications	Bow: 10–20µm Warp: 20-40µm TTV: < 3-5µm
OEM tools	Wolters AC1200
General process parameters	Plates: 0.9-1.1m/s Carrier: 3-6 orbits Pressure: 1.8-2.5PSI Flow rate: 40-80ml/min
Pureon solution	Slurry: OPW-21 Pad: MHS15S
Benefits vs POR	Reduced thinning time through optimized pad & slurry

Process solution for DMP1 (bulk removal) with OPW-21 on MHS15S pad

Range for Inputs

Parameter	Value
Lower plate speed	0.9-1.1m/sec CCW
Upper plate speed	0.9-1.1m/sec CW
Carrier	3-6orbits/min
Flow rate	40-80ml/min
Down force	1.5-2.5PSI
Pad	MHS15S
Slurry	OPW-21/FG

Expected Outputs

Parameter	Value
Removal rate	0.4-0.8µm/min
TTV	< 3µm
Bow	10-20µm
Warp	20-40µm
Surface quality	< 3nm Ra
Typical cycle time	60-180mins
Pad lifetime	40-80 cycles

Process outputs dependent on wafer diameter, number of wafers per load.
Lower platen rotates

Diamond slurry for wafer thinning- DMP 2

Process steps	DMP 2
OEM tools	Lapmaster Wolters AC 1200P
General process parameters	Plates: 0.9 – 1.1 m/s Carrier: 3 – 6 orbits Pressure: 0.3 daN Flow rate: 60 ml/min
Pureon solution	Slurry: OPW-21/25 FG 3 Pad: MHS15S
Benefits vs POR	– Reduced thinning time through optimized pad & slurry – Focus on TTV and surface roughness

Process solution for DMP2 (high quality polishing) with diamond slurry on PU-pads (double side polishing)

Range for Inputs

Parameter	Value
Lower plate speed	0.9 – 1.1 m/sec CCW
Upper plate speed	0.9 – 1.1 m/sec CW
Carrier	4 rpm
Flow rate	60 ml/min
Down force	0.3 daN
Pad	MHS15S
Slurry	OPW-21/25 FG3

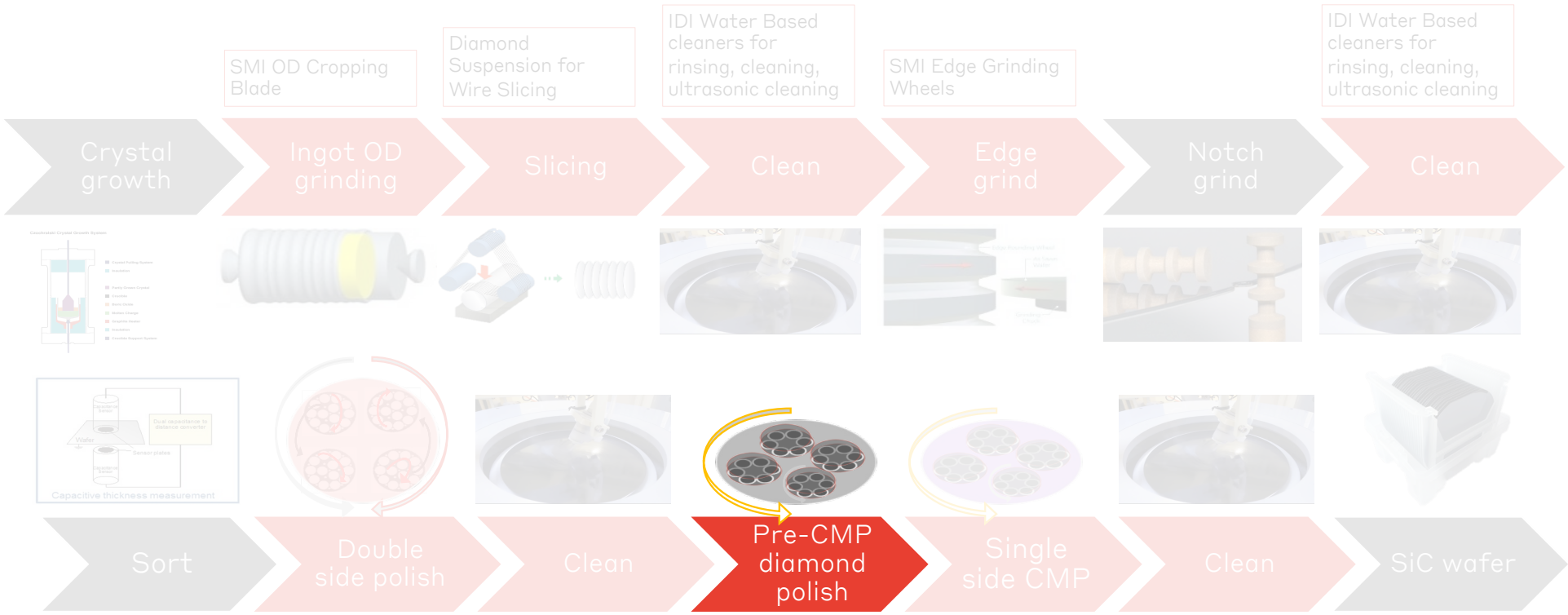
Expected Outputs

Parameter	Value
Removal rate	0.4 µm/min
TTV	< 1 µm
Bow	10 – 20 µm
Warp	20 – 40 µm
Surface quality	< 1 nm Ra
Typical cycle time	25 mins
Pad lifetime	60 – 80 cycles

Process outputs are dependent on wafer diameter and number of wafers per load.
Lower platen rotates.

Pureon solutions in the wafer manufacturing process

Pureon Participation



Pureon solution DMP – Single side polishing

Process steps	Pre-CMP
OEM tool	GigaMat 3808
General process parameters	Platen speed: 2.8 – 3.5 m/s Head speed: 2.8 – 3.5 m/s Pressure: 5 – 7 PSI Flow rate: 120 – 180 ml/min
Pureon solution	Slurry: STD < 1 µ Pad: SUBA 800 Templates: DF-200
Benefits vs POR	– Improved incoming conditions to CMP – Lowers total CoO

Pureon process solution for Pre-CMP
Single side batch process

Range for Inputs

Parameter	Value
Plated speed	2.8 – 3.5 m/s CCW
Head speed	0.9 – 1.1 m/s CW
Flow rate	150 ml/min
Down Force	5 – 7PSI
Pad	SUBA 800
Slurry	STD 0.5 – 1.0 µm
Template	NTA-DF200

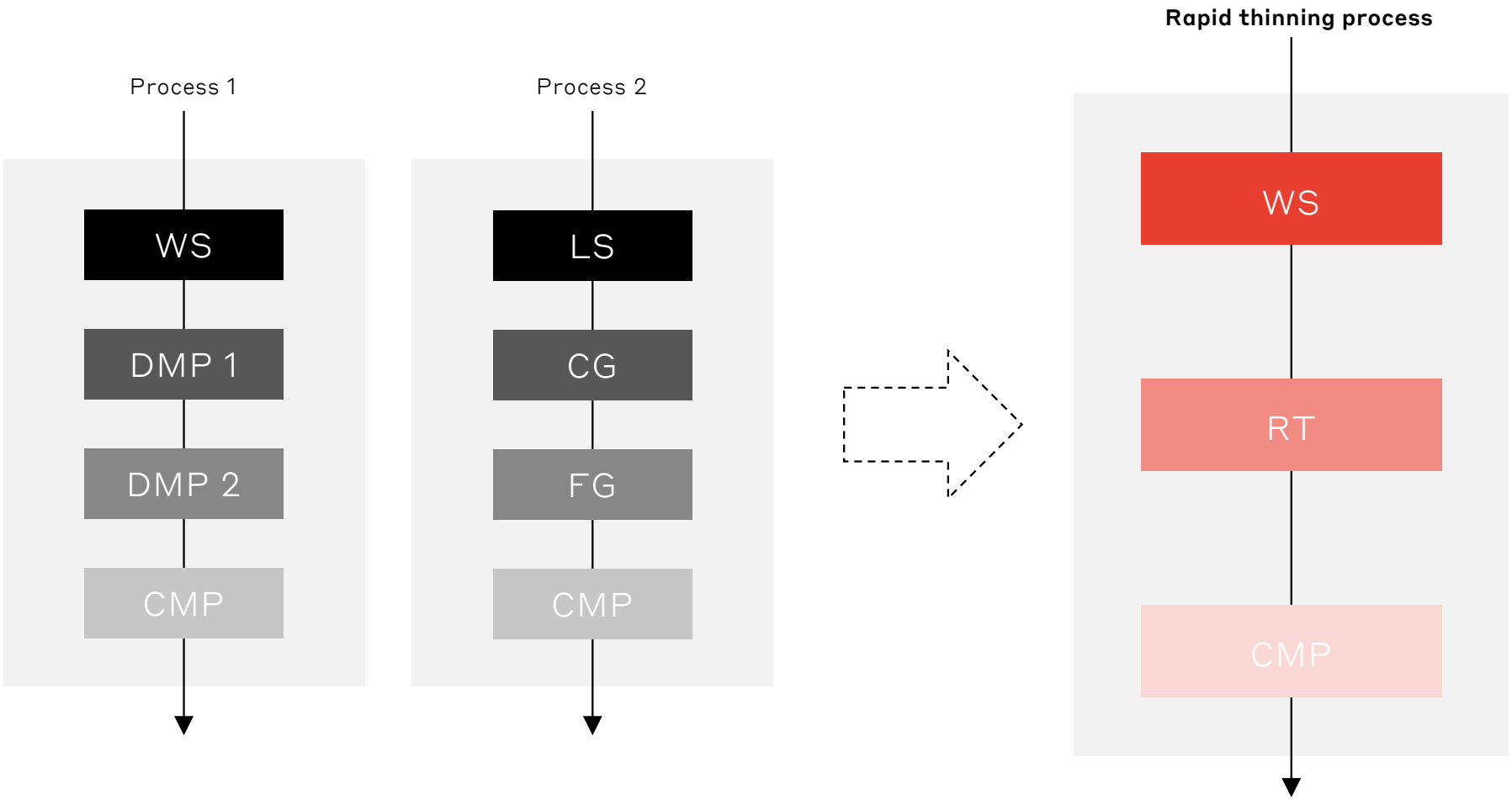
Expected Outputs

Parameter	Value
Removal rate	0.1 – 0.2 µm/min
TTV	< 3 µm
Bow	10 – 20 µm
Warp	20 – 40 µm
Surface quality	< 0.5 nm Ra
Typical cycle time	20 – 40 mins
Pad lifetime	150 – 200 cycles

Process outputs are dependent on diameter of wafer and number of wafers per run.
Removal rate varies between Si and C Face.

SiC wafering process

Rapid thinning approach to SiC wafering



Approach- coarse polishing

Target values after polishing

Polishing parameters	Target values
Removal rate [µm/min]	> 1,0
Surface Roughness Ra [nm]	< 6 nm
TTV [µm]	< 2 nm
LTV [µm]	< 2

CRASH-FREE-POLISHING-PROCESS

Additional requirements

– Lower wafer costs for slurry (3 USD/wafer?)

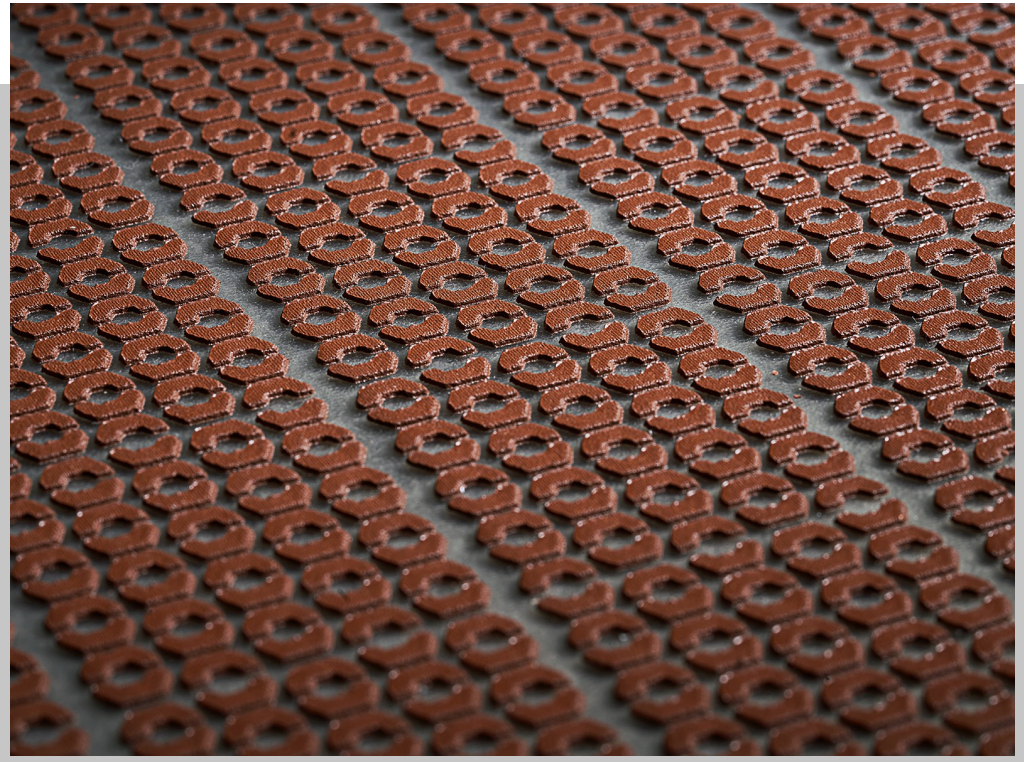
– Slurry flow rate: 15 – 20 ml/min

– Long pad life (> 25 runs)

– Process duration: < 30 min

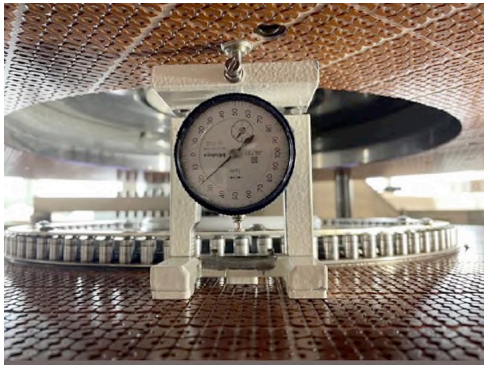
SiC wafering process

Composite pads for rapid thinning- IRINO



Rapid thinning

Development program on 6″ SiC-Wafer



Workpieces: 12 SiC-wafer; diameter: 150 mm

6 carrier rings; 2 wafer per carrier ring

Chosen Machine Pressure: 425 daN

Dosage: L1 = 13% (60 ml/min); L2 = 8% (40 ml/min); L3 = 8% (40 ml/min)

Incoming thickness of the workpieces: 406,2 µm (avg)

Incoming surface quality: not measured („as sawn“)

Thickness of the carrier rings: 300 µm, material: steel

Polishing pad: IRINO-PRO-C 2S264P 1220 x 552mm

Slurry 1: Pureon-SPG ; Slurry 2: SPG-100 Lubricant

Result

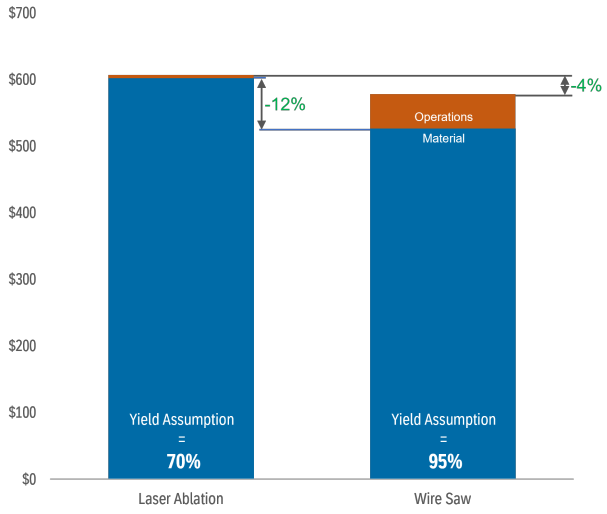
1. Total removal: 406,2 µm (avg) -370,3 µm (avg) = 35,9 µm
2. Polishing time: 25:00 minutes (15:00 minutes in L2)
3. Removal rate: 1,44 µm/min (total); 2,39 µm/min (L2)
4. TTV: 3,2 µm (avg)
5. Surface roughness: Si-side Ra = 5,4 nm, Rz = 38,0 nm; C-side: Ra = 5,9 nm, Rz = 32,7 nm

Cost of ownership lowered by more than 30%

Total Cost of Ownership along complete process chain is mainly improved by

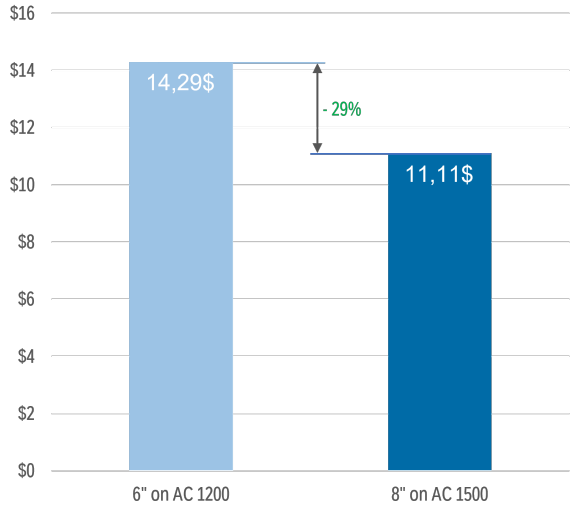
- Yield optimized wire slicing process, along with minimal kerf loss
- Consolidation of Rapid thinning and diamond mechanical polishing (DMP) process
- Consumable optimization for Rapid thinning approach to increase material removal

Cost of Ownership Wafer Slicing



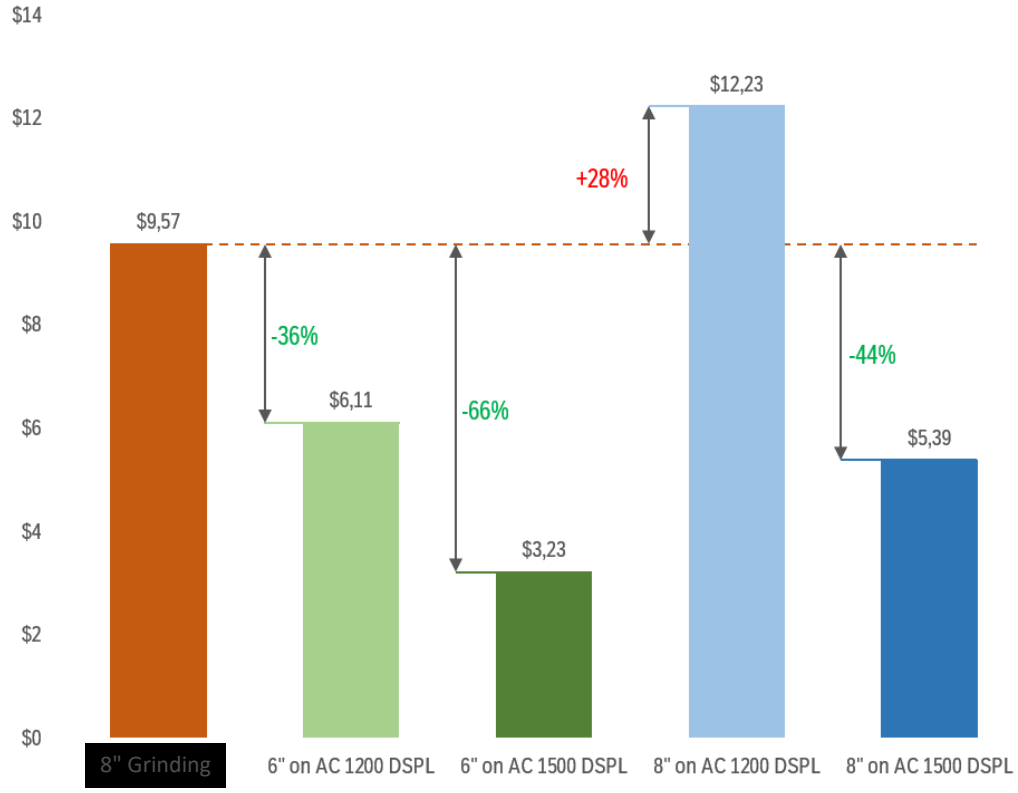
Cost of Ownership Rapid thinning

Cost of Ownership CMP

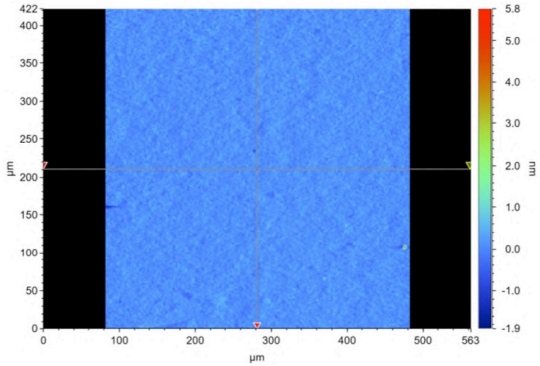


Cost of ownership for Rapid Thinning is over 40% LESS when compared to Grinding approach

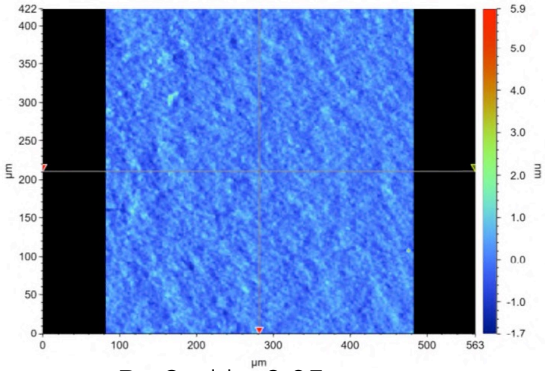
- Optimized process chain including rapid thinning enables optimized Cost of Ownership
- Consumable costs as main driver of CoO
- Rapid Thinning approach offers consumable saving processes compared to grinding
- CoO optimization additionally enabled by batch processing
- High throughput numbers of AC 1500 SiC offer up to 44% lower costs per wafer compared to grinding using the rapid thinning approach



Can we go from Rapid thinning directly to CMP? YES!



Ra Si-side: 0,10 nm



Ra C-side: 0,25 nm

System	CMP
Machine	AC1200-P
Carrier Drive system	12TF/36
Max. Load pressure	0,7 kg/cm^2
Slurry	Potassium-Permanganate pH 7 – 9
Slurry Handling	Recycling
Pad	SUBA 800

Process results		
Number of wafers per batch	14	6″ SiC-Wafer
Removal (1h main load)	7,5	nm
TTV AVG	0,5	nm
Ra Si-side	0,10	nm
Ra C-side	0,25	nm
Visible scratches	none	

SiC wafering process

Summary

- Introduction of the new RAPID THINNING approach is a paradigm shift that can lead to significant reductions in not only the cost of the wafer arising from thinning operations but also the CAPEX for the entire operation
- Cost of ownership using rapid thinning can be as much as 40% lower compared to the grinding process
- Existing Slicing and polishing of SiC-wafers still offers lots of room for further improvements with respect to MRR, geometry, and surface roughness. These improvements will significantly contribute to lower CoO
- Pureon has a very close cooperation with the key OEMs ➔ we have the technology and the know-how to develop new or improve existing processes
- Each customer has different needs ➔ together with the OEMs we develop highly tailor-made, individual slicing and polishing solutions

Acknowledgements

Special thanks to Lapmaster Wolters for the co-operation for conducting the tests together.

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