Tight process control for GaN-based power devices: The potential of connected metrology in semiconductor device production

Dr. Kolja Haberland

CTO

LayTec AG

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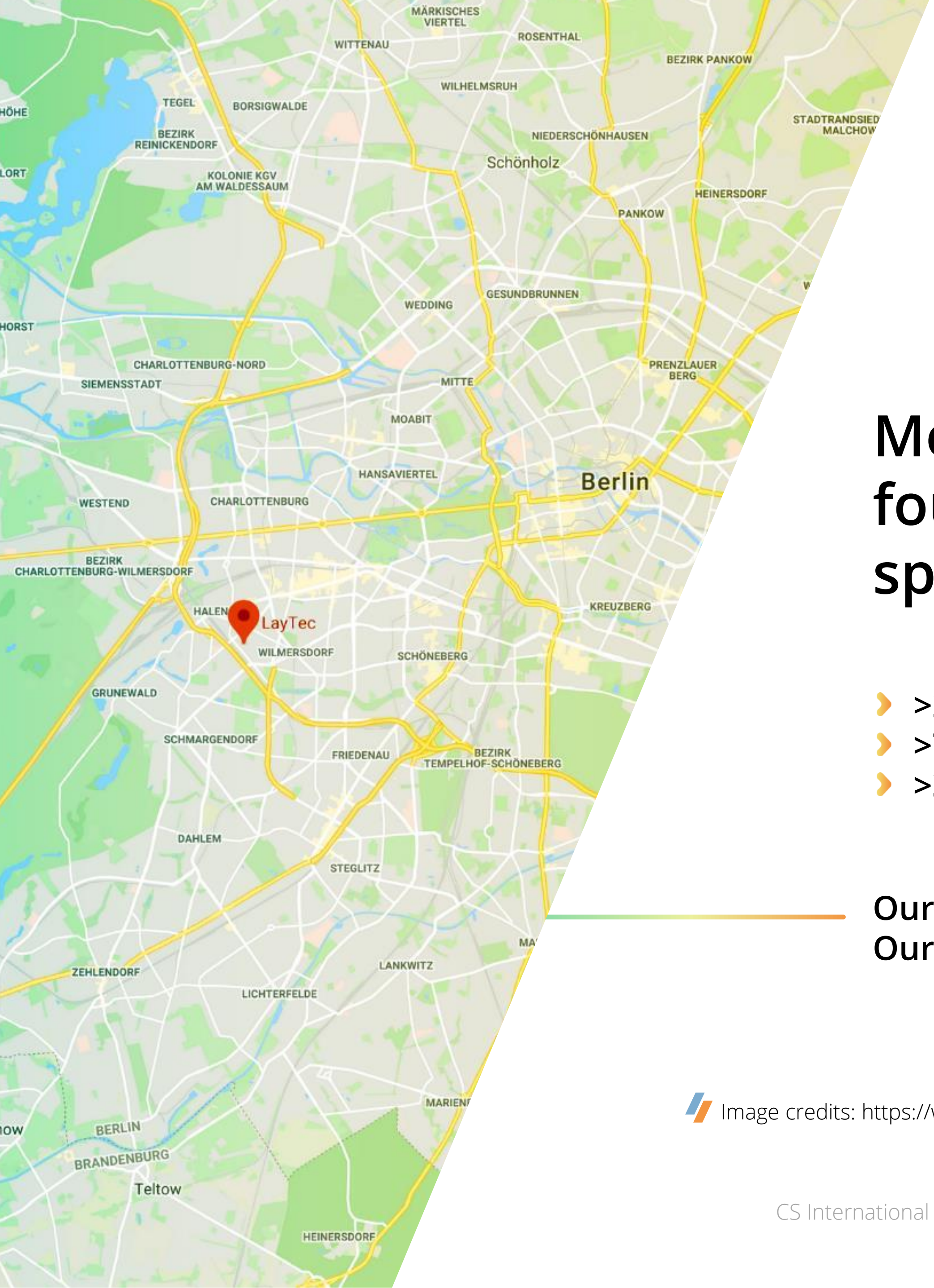

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Metrology company founded 1999 in Berlin spin-off of TU Berlin

- >20 years old
- >75 employees
- >3300 systems sold
- operating worldwide
- member of NYNOMIC THE PHOTONICS GROUP

Our business: Process-integrated optical metrology

Our markets: Semiconductor and thin-film industry & academia incl. lighting, laser, PV, glass coating …

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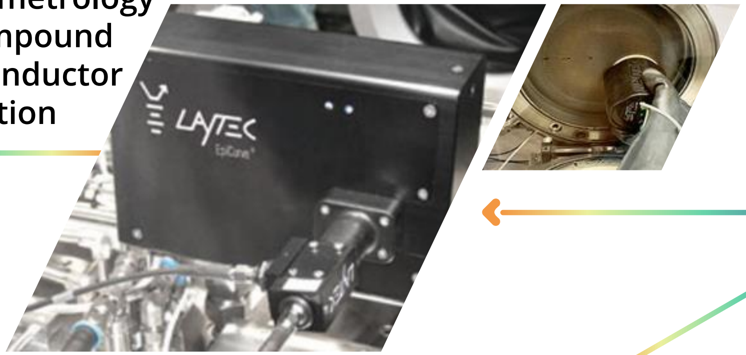
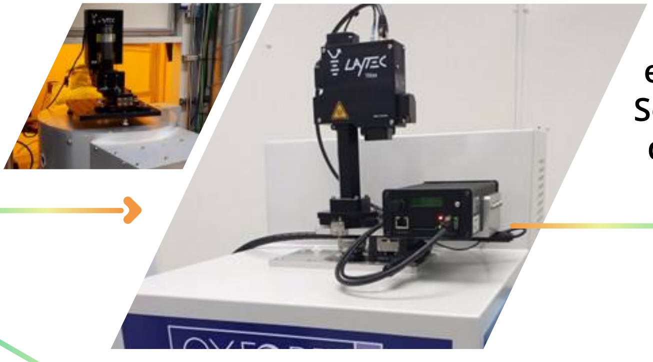
LayTec – expertise and applications in metrology for …

MOCVD



In-situ metrology for Compound Semiconductor Deposition

Etch

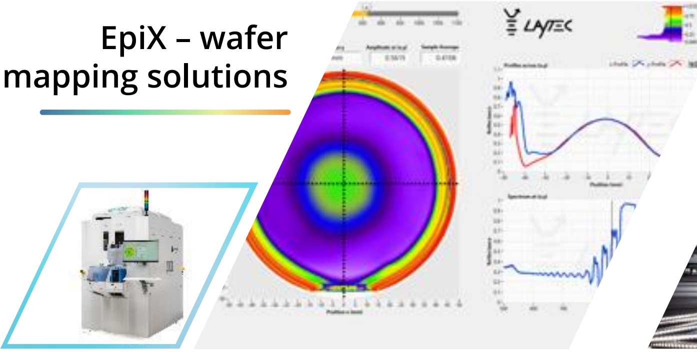


Optical endpointing Solutions for dry and wet Etching

PV

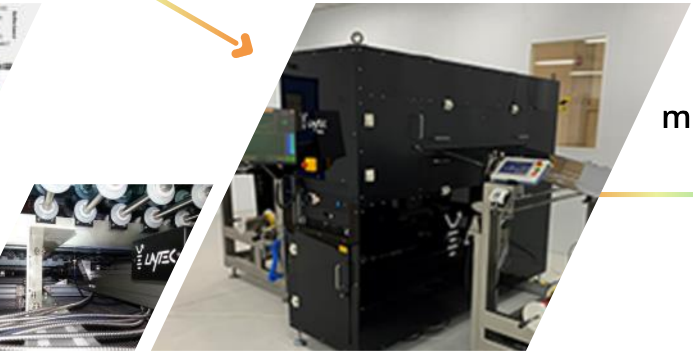
Metrology for characterization of high efficiency Photovoltaics

Mapping



EpiX – wafer mapping solutions

R2R



ILMetro – in-line measurement stations

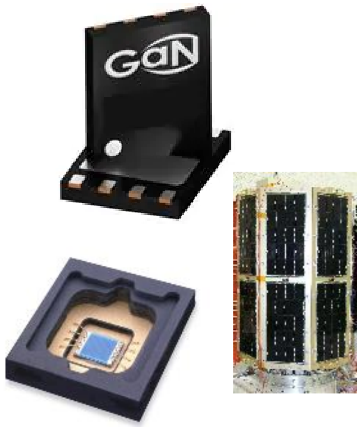
(Some of) todays challenges in semiconductor industry

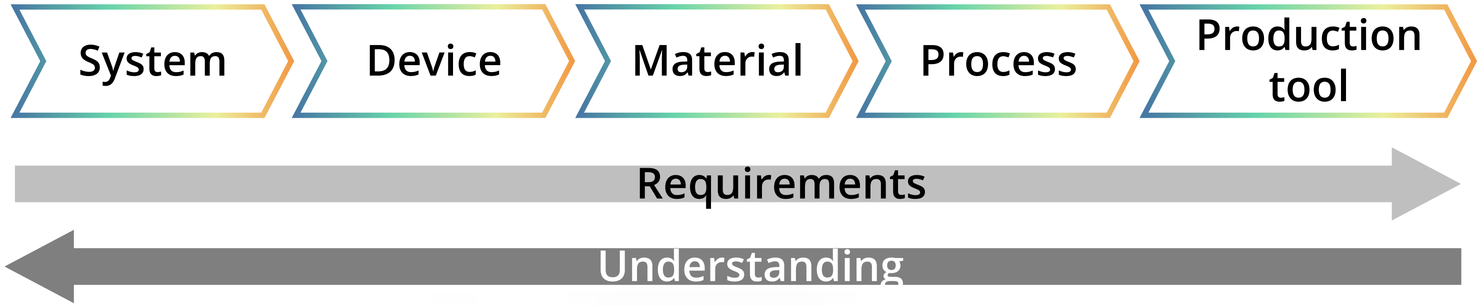
- **Diversification and Resilience of Global Supply Chains**
  - Fab-to-Fab process matching (Asia, Europe, North America)
- **Increasing complexity of devices required for higher device performance**
  - increasing number of layers
  - more complex layer structures
  - tighter specifications for individual layer
- **Increase yield**
- **Reduce cost**

Problem:
No MOCVD system or plasma etch tool has any knobs that say „device performance", „gain", „breakdown voltage", „switching frequency" etc.

→ You need all the help you can get to bridge that gap!

On the road to higher performance, higher yield and lower cost ...





System

Device

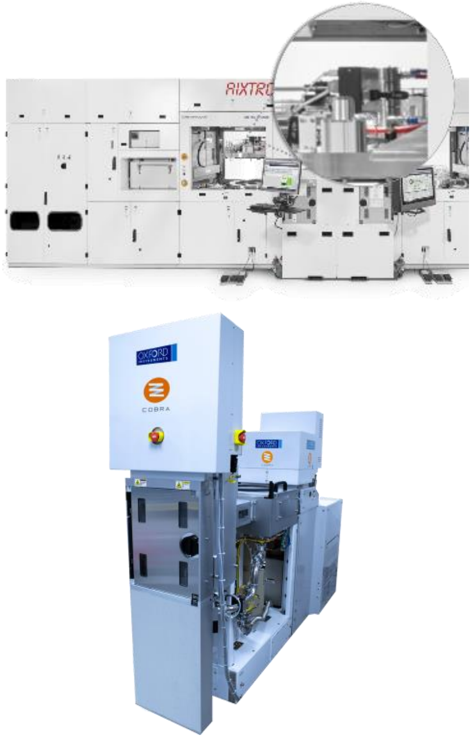
Material

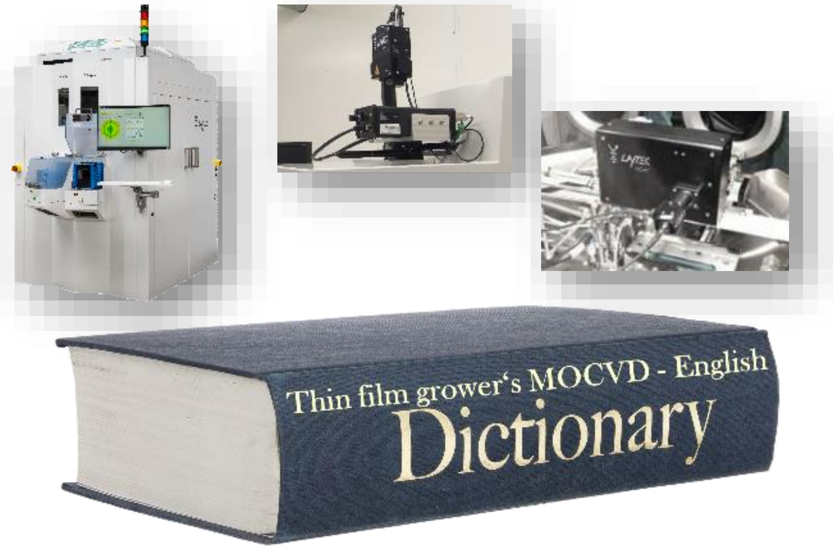
Process

Production tool

Requirements

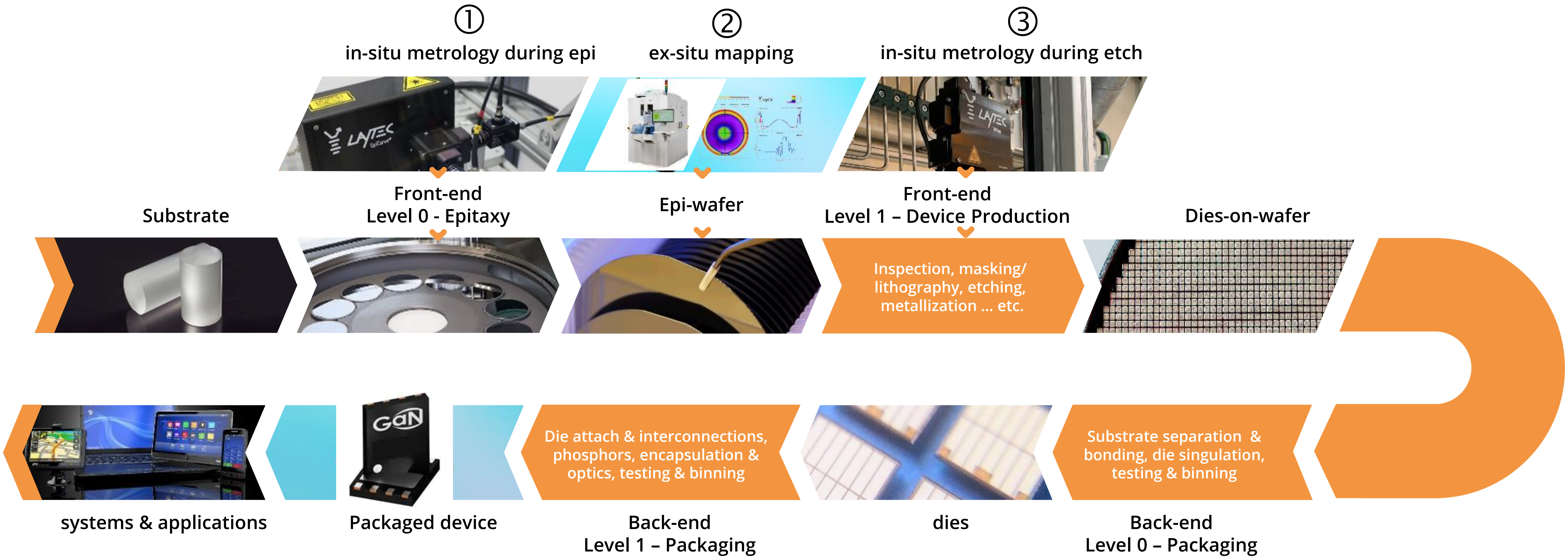
Understanding





→ Metrology helps you to understand – metrology can be your dictionary!

Optical metrology along the semiconductor manufacturing chain



① in-situ metrology during epi

② ex-situ mapping

③ in-situ metrology during etch

Substrate

Front-end
Level 0 - Epitaxy

Epi-wafer

Front-end
Level 1 – Device Production

Inspection, masking/
lithography, etching,
metallization … etc.

Dies-on-wafer

Back-end
Level 0 – Packaging

Substrate separation &
bonding, die singulation,
testing & binning

dies

Back-end
Level 1 – Packaging

Die attach & interconnections,
phosphors, encapsulation &
optics, testing & binning

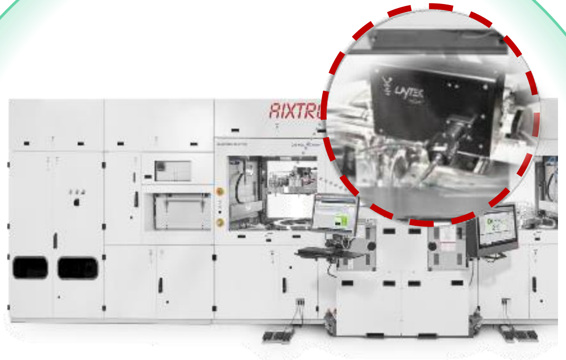
Packaged device

systems & applications

LayTec offers various metrology solutions along the manufacturing chain

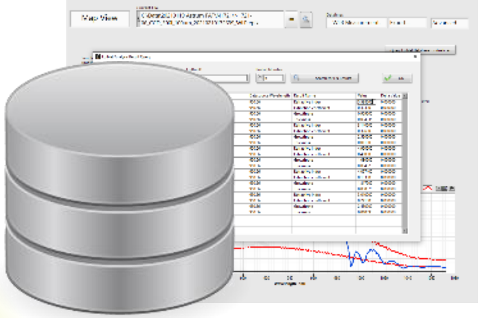
LayTec "Metrology Ecosystem"

EpiCurveTT:
in-situ measured layer thickness
and other layer properties



In-situ metrology
during MOCVD

Database of measured data



Wafer mapping

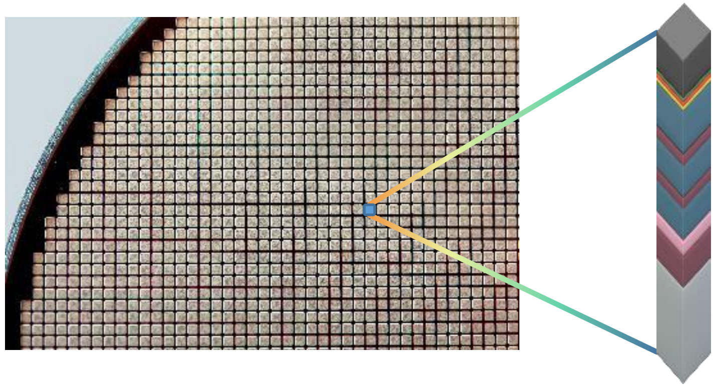
EpiX:
spatial variation
of layer properties

Etchpoint and *TRIton*:
end point detection based
on actual layer thickness

In-situ metrology during
plasma etching

- The same wafer is measured 3+ times
- The amount of information increases
- and is combined for improved analysis in downstream processes

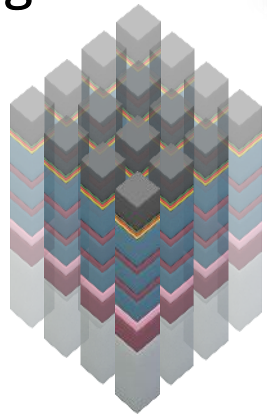
Goal of connected metrology



- Full quantification of critical layers on die-level
  - layer thicknesses
  - layer compositions
  - layer strain / relaxation …

How do we get to "*Full quantification of critical layers on die-level*" ?

- Characterize wafer in full 3D
- by combining in-situ epi metrology with ex-situ 2D wafer mapping
- Transformation of full 3D wafer data into die matrix

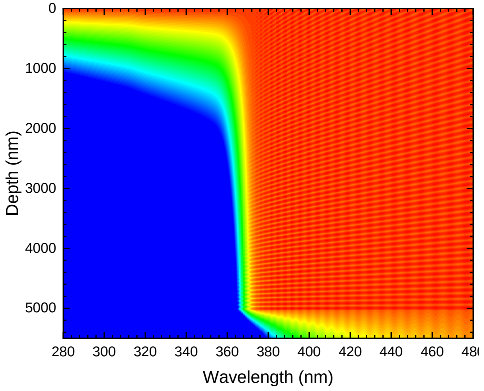


Why is ex-situ optical wafer mapping with stack analysis algorithms not sufficient for full 3D characterization?

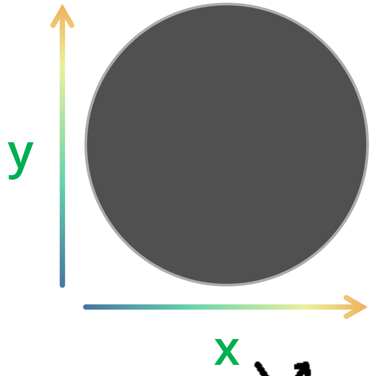
in-situ metrology for
z-axis (*growth direction*)

wafer mapping for
x, y (*lateral*)

Simulated EM field
inside GaN-on-Si HEMT

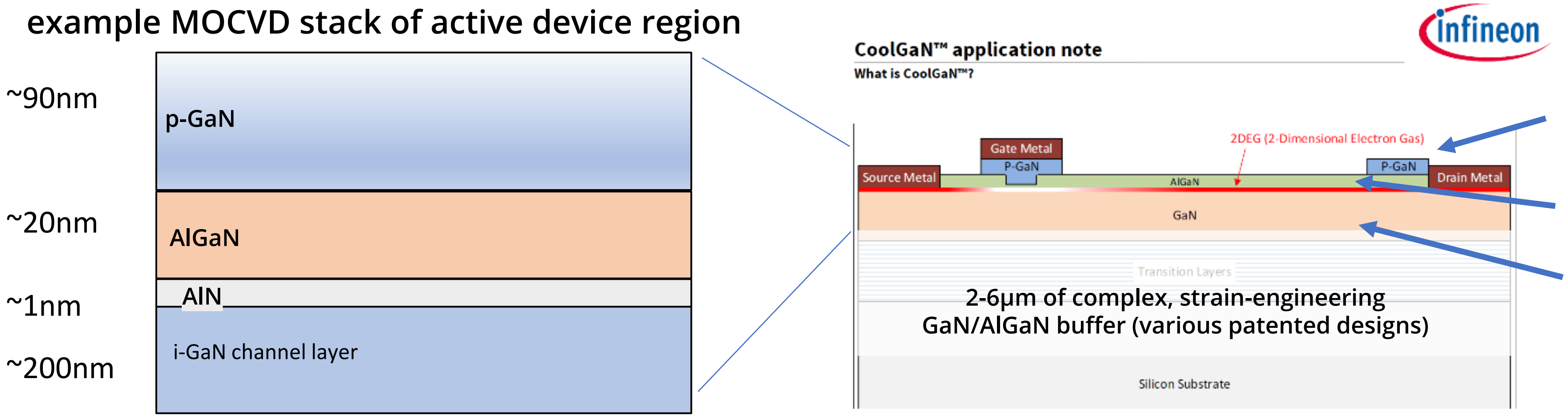


- Depth information usually blocked (UV) / disturbed (vis-NIR) in ex-situ measurements of Epi-wafers
- for complex structures no non-destructive metrology can achieve full 3D characterization alone
- **Need to combine measurement results from complementary metrology tools for advanced 3D layer stack analysis**



GaN/Si HEMT production – film thickness control during MOCVD and Etching

example MOCVD stack of active device region



2-6µm of complex, strain-engineering GaN/AlGaN buffer (various patented designs)

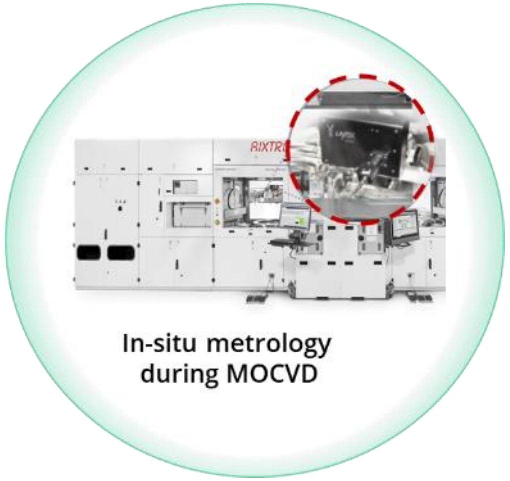
p-GaN: 10nm … 100nm

AlGaN: 10nm … 30nm

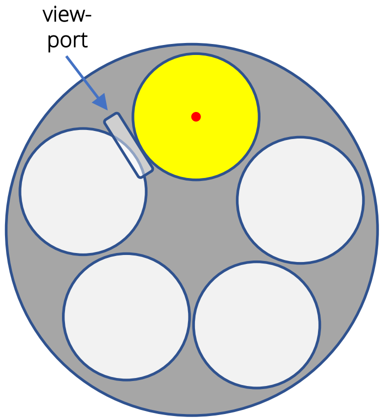
i-GaN: 100nm … 200nm

- For cost reasons: large 200mm (soon: 300mm) silicon wafers and extreme uniform epi and etching is required
- optical in-situ control on the level of 0.5nm (~1 atomic monolayer) is a must

① MOCVD: in-situ measurement in center of one selected wafer

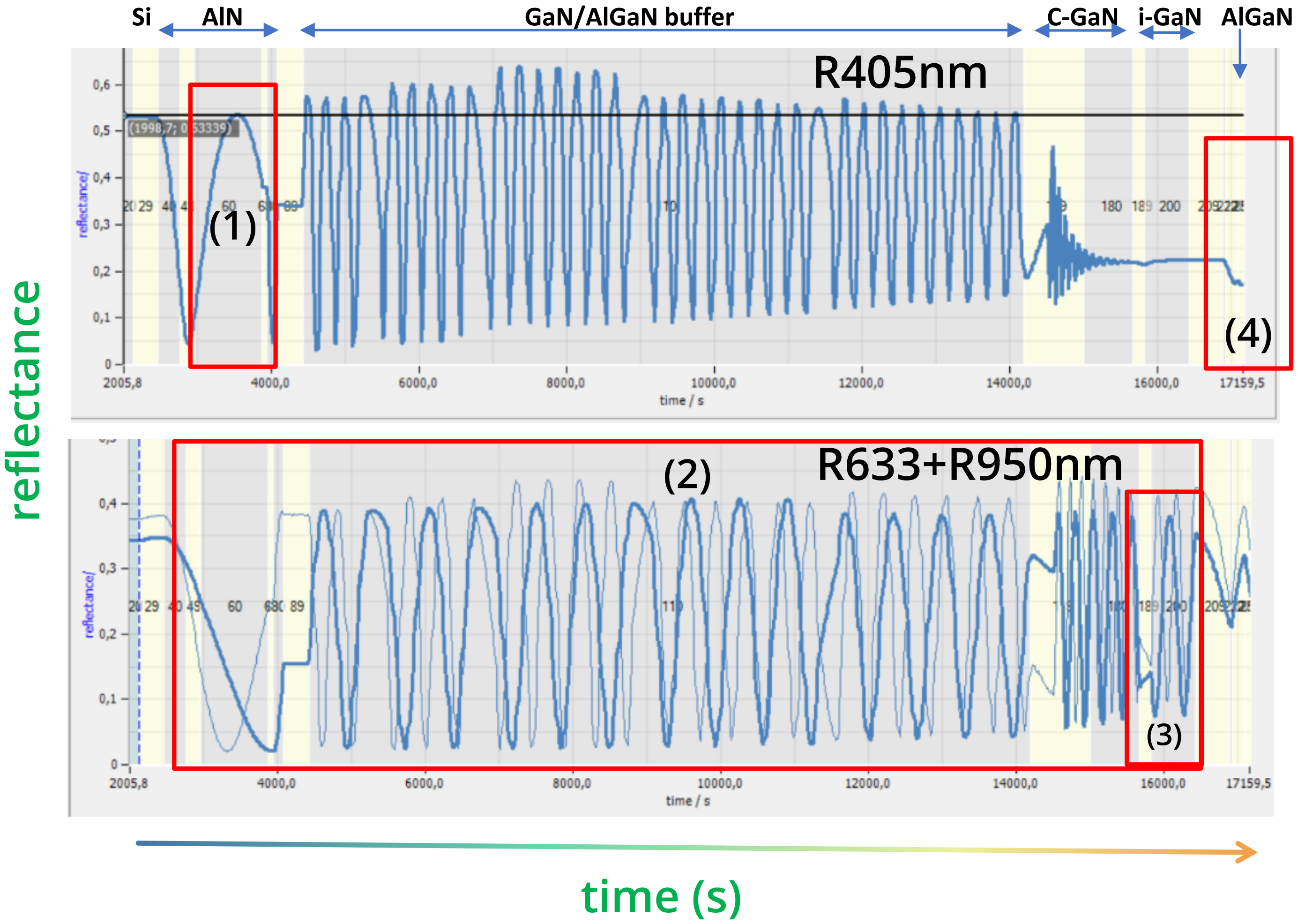


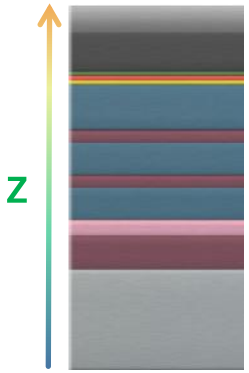
- metrology tool: LayTec EpiCurveTT
- every 2 s measurement of
  - temperature
  - multi-λ reflectance
  - local curvature
- at center of specific wafer
- plus radial scan across wafer (unsynchronized)
- typical growth time: few hours
- sensitivity of in-situ measurement unchanged from first to last layer



Example: 5x 200mm Si,
AIXTRON Planetary Reactor©,
30 RPM

① MOCVD growth analysis





thickness of most critical layers can be determined from in-situ data

- Increasing complexity of devices requires continuous enhancements of individual measurement methods
  - short reflectance wavelengths to analyze thinner layers (with higher Al-content)
  - advanced analysis algorithms for multi-layer-analysis / multi-wavelength-fits / …

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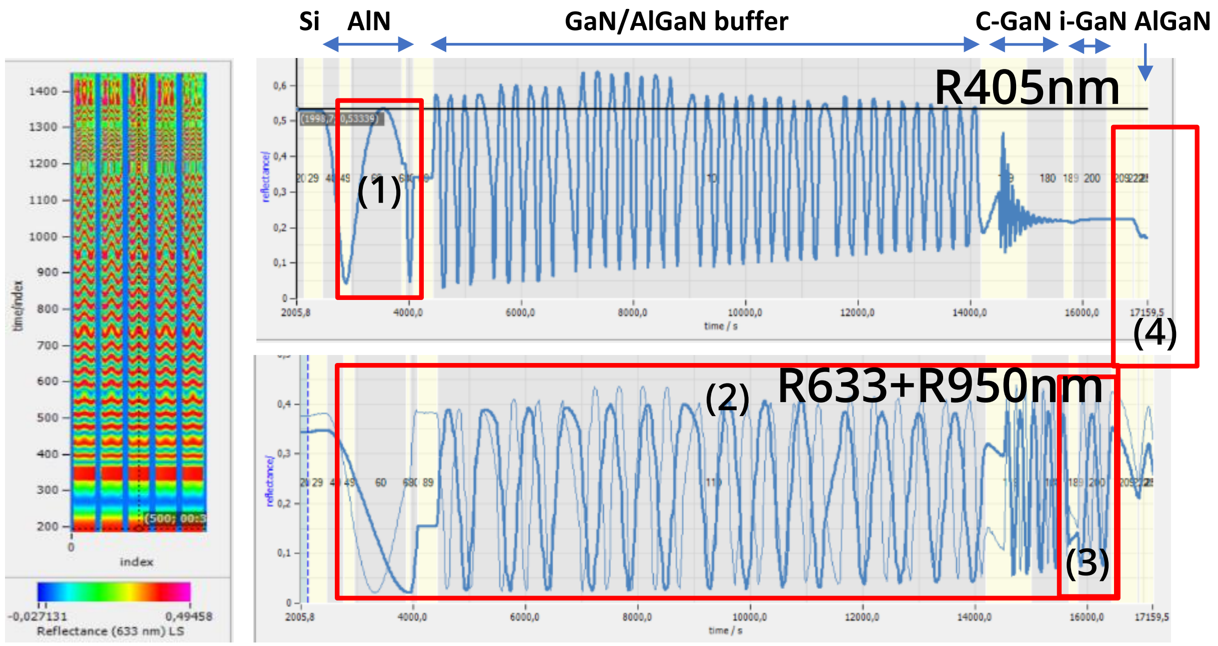
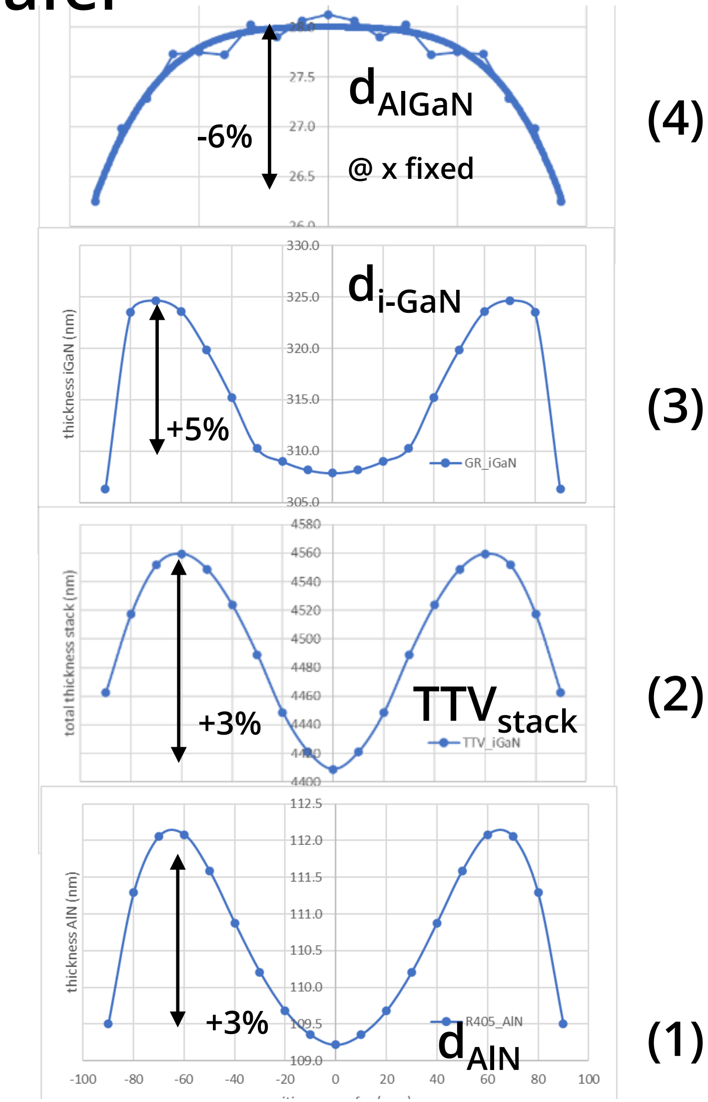
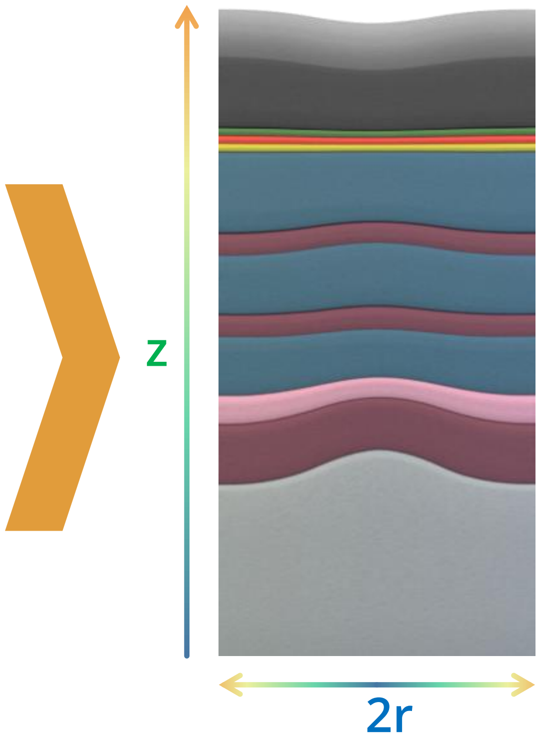
① MOCVD: extending analysis across wafer



- Identical analysis recipe as for wafer center gives radial distribution of individual layer parameters

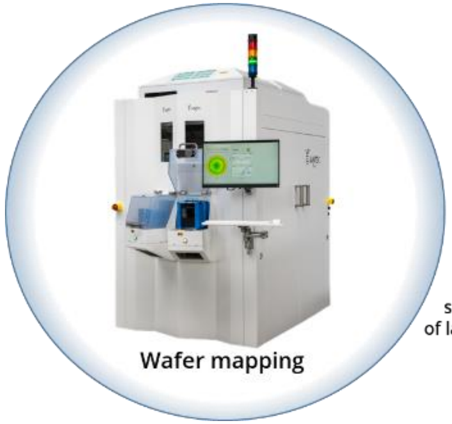


10 wafer zones → 19 radial points



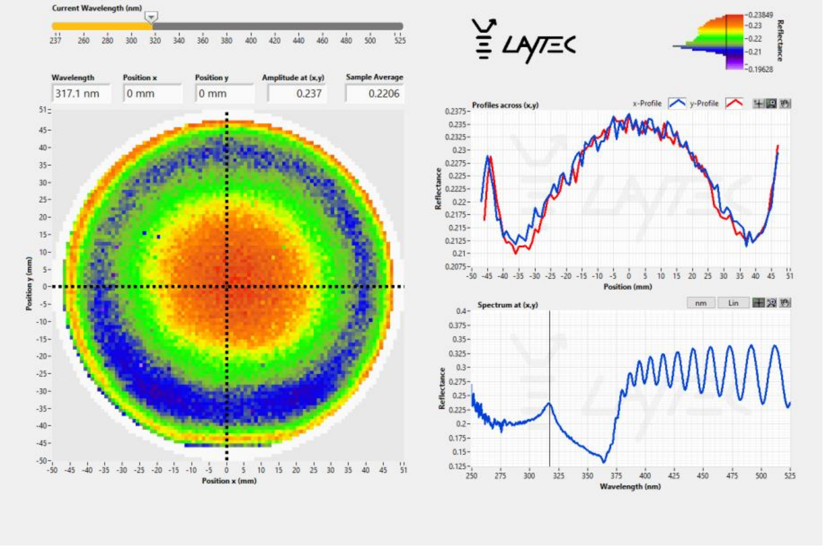
Radially resolved stack information

② Post epi wafer mapping



EpiX:
spatial variation
of layer properties

- Metrology tool: LayTec EpiX
- Ex-situ wafer mapping
- White light reflectance and photoluminescence
- x,y mapping @ 250-2400 nm
- Goal
  - obtain x,y quantification of critical layers (e.g., barrier)
  - derive die-level quantification of entire stack
- Using layer thickness values (radial profile data) determined from in-situ reflectance as starting values



Wavelength: 317.1 nm
Position x: 0 mm
Position y: 0 mm
Amplitude at (x,y): 0.237
Sample Average: 0.2206

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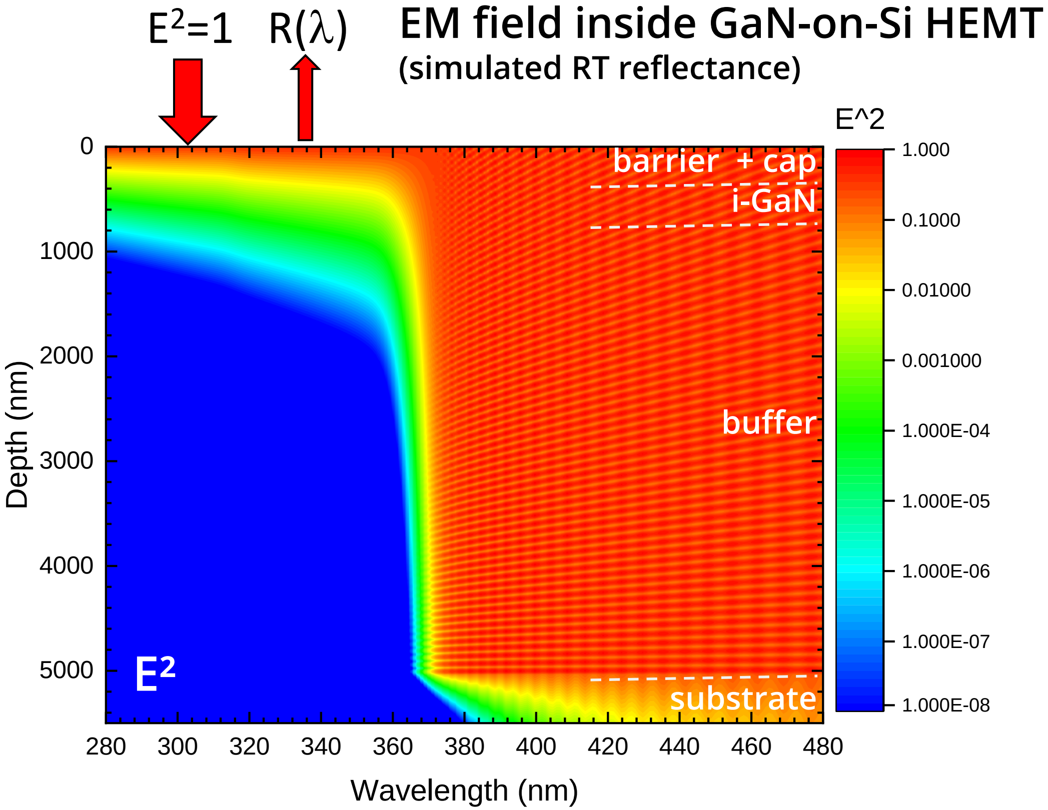
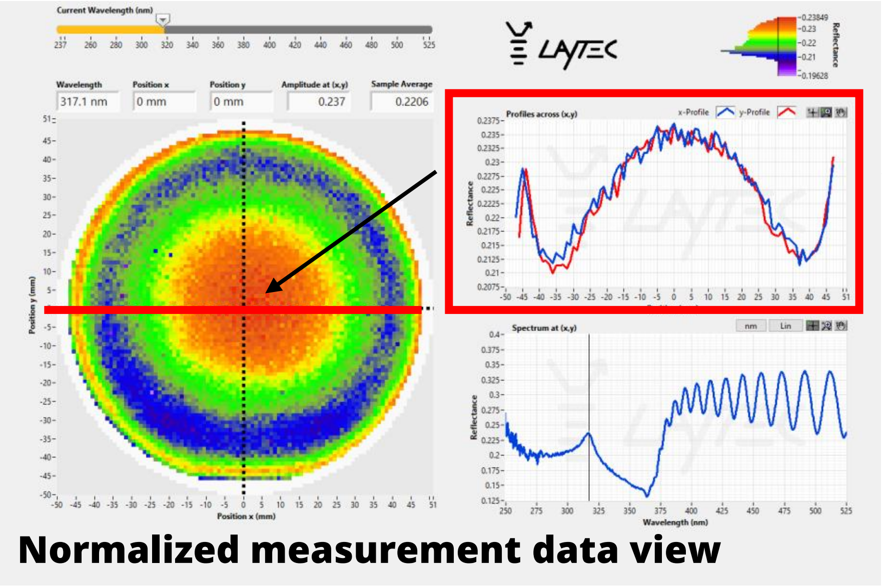
② Post epi wafer mapping

EM field inside GaN-on-Si HEMT
(simulated RT reflectance)

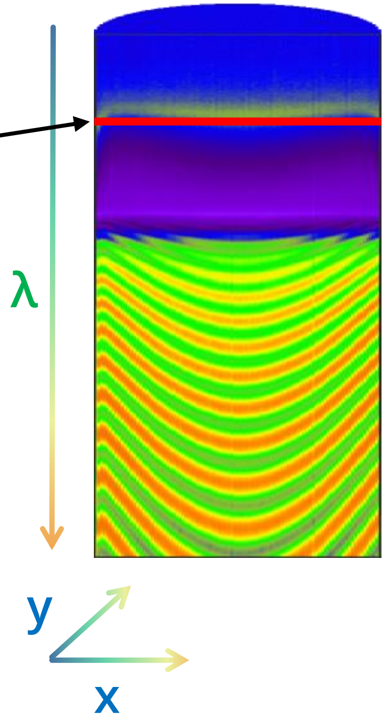


Color-Code = Lg-scale, normalized to incoming intensity of 1.0



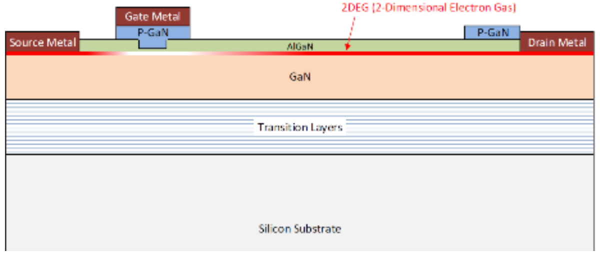
Wavelength: 317.1 nm
Position x: 0 mm
Position y: 0 mm
Amplitude at (x,y): 0.237
Sample Average: 0.2206

Normalized measurement data view

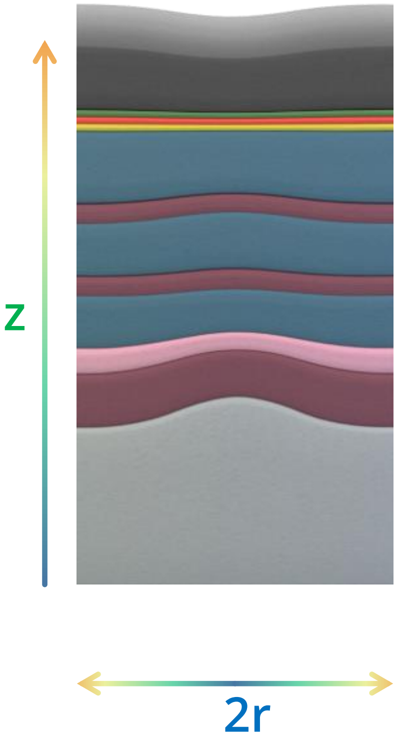


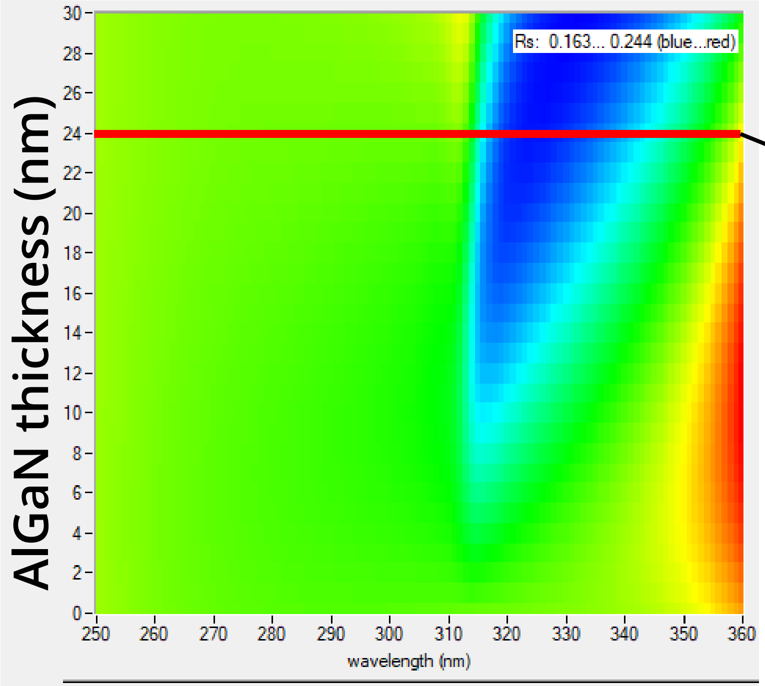
- selection of suitable spectral region for analysis of dedicated layers
- UV → upmost few hundred nm → barrier and neighboring layers
- visible → total thickness variation → mainly buffer

② Post epi wafer mapping – UV spectral fitting of HEMT structures

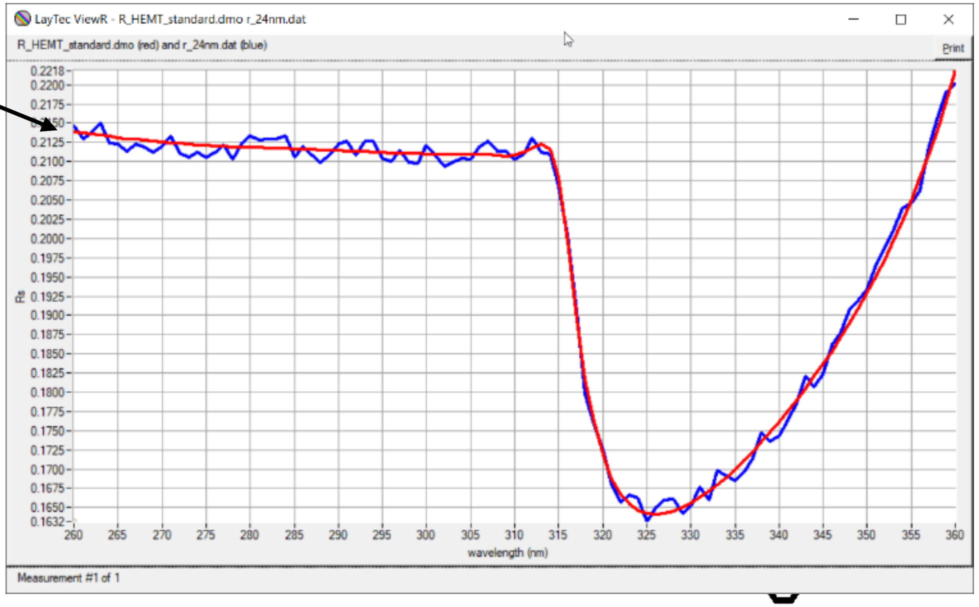


- radial profile of layer properties of entire stack available from in-situ data
- For critical layers in upmost few hundred nm derive x,y resolved layer properties from full spectral fitting



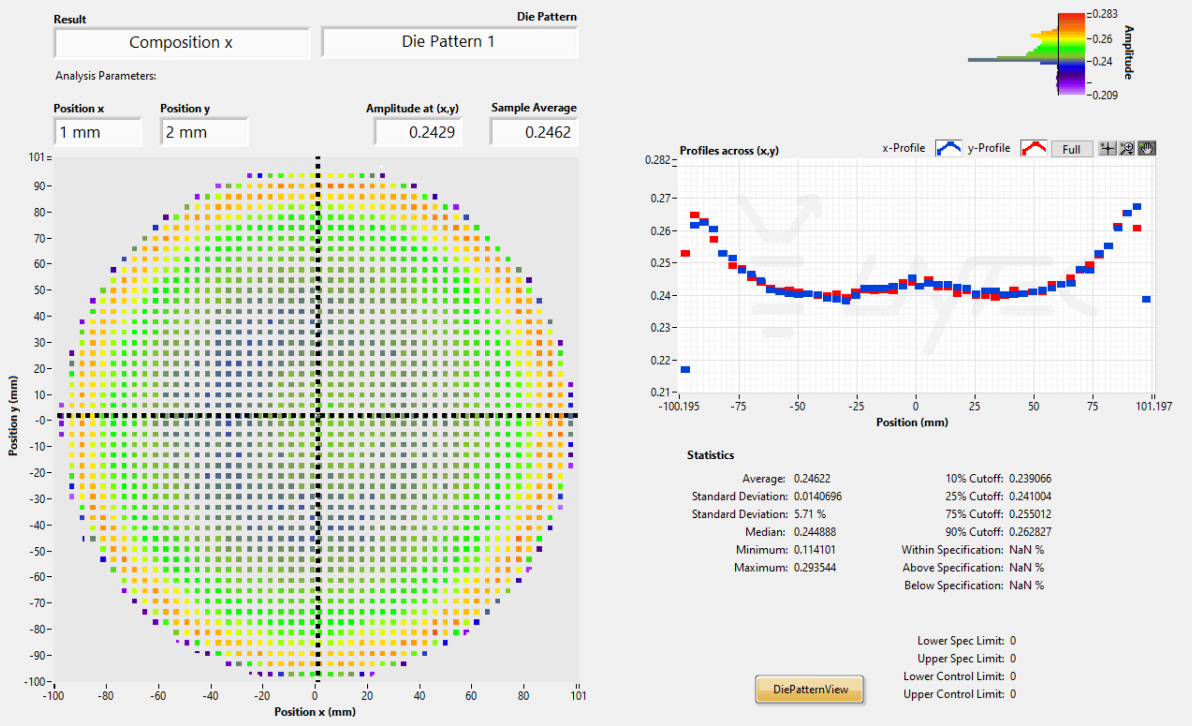


Spectral fitting of barrier composition and thickness of simulated E-Mode HEMT with 50 nm p-GaN


LayTec ViewR - R_HEMT_standard.dmo r_24nm.dat

R_HEMT_standard.dmo (red) and r_24nm.dat (blue)

② Virtual die patterns



Result
Composition x

Die Pattern
Die Pattern 1

Analysis Parameters:

Position x 1 mm
Position y 2 mm
Amplitude at (x,y) 0.2429
Sample Average 0.2462

Statistics

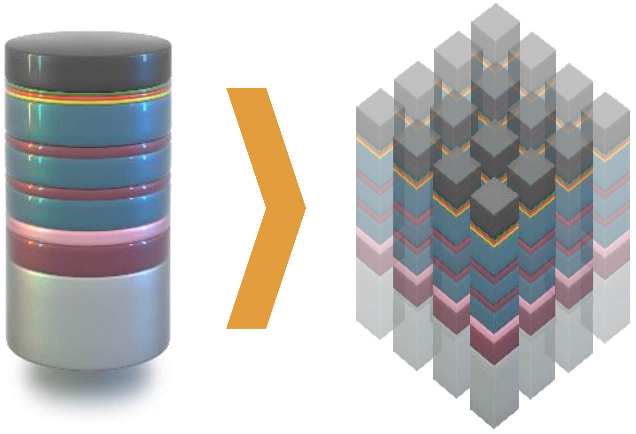
Average: 0.24622
Standard Deviation: 0.0140696
Standard Deviation: 5.71 %
Median: 0.244888
Minimum: 0.114101
Maximum: 0.293544

10% Cutoff: 0.239066
25% Cutoff: 0.241004
75% Cutoff: 0.255012
90% Cutoff: 0.262827
Within Specification: NaN %
Above Specification: NaN %
Below Specification: NaN %

Lower Spec Limit: 0
Upper Spec Limit: 0
Lower Control Limit: 0
Upper Control Limit: 0

Result data: barrier composition – die-level view

- define and apply custom die patterns
- obtain resulting analysis information on die-level
- obtain yield-classification on die-level
- rotate or modify die pattern to improve yield



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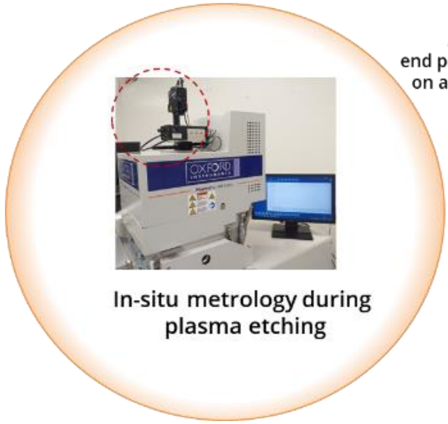
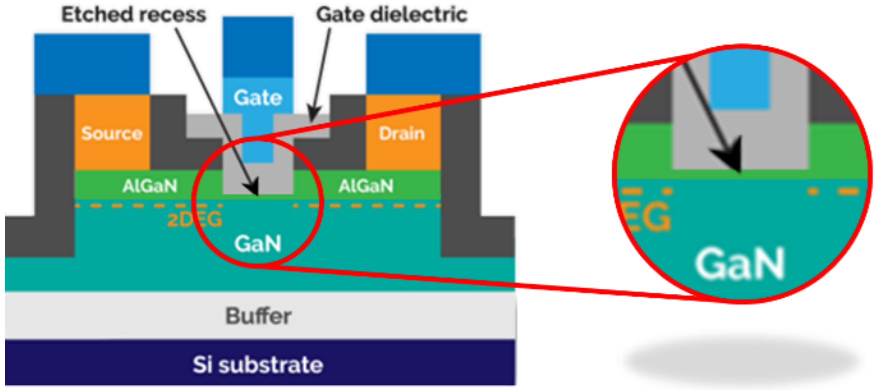
③ Plasma etching of HEMT structures



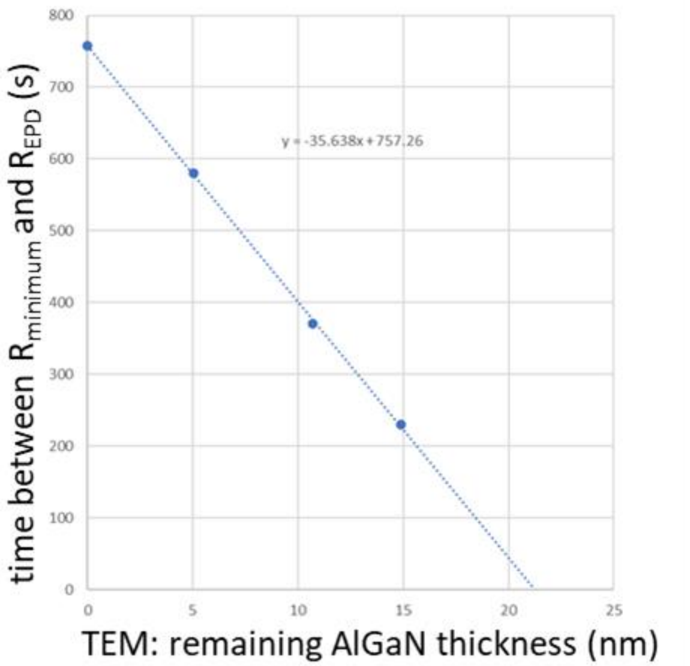
Etchpoint and *TRIton*:
end point detection based
on actual layer thickness

In-situ metrology during plasma etching

- Metrology tool: LayTec Etchpoint or TRIton
- UV-reflectance based
- Measurement of etch rate and remaining layer thickness
- Automated endpointing (EPD) for AlGaN and GaN etch
- e.g. for normally-off recessed gate AlGaN/GaN MISHEMTs



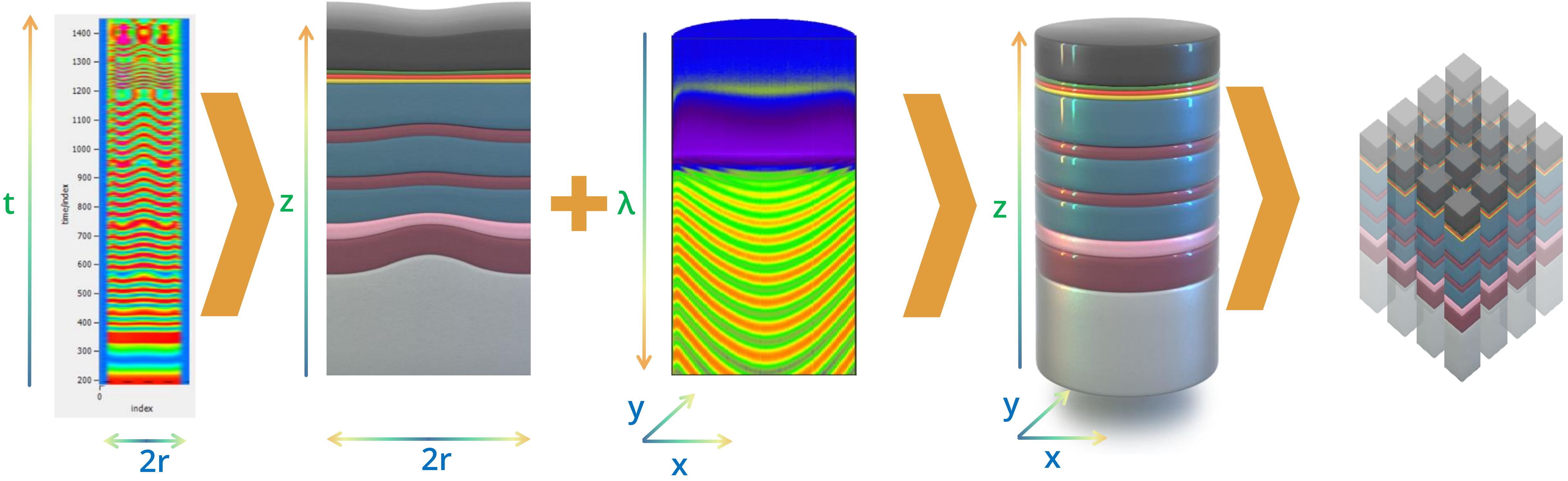
③ Atomic Layer Etch of AlGaN using EPD for recessed gate MISHEMT



in cooperation with

- Sub-nm accuracy for endpointing
- Perfect match between AlGaN thickness (TEM) and in-situ measurement

Summary



multi-λ in-situ measurement

in-situ analysis

ex-situ mapping

combined ex-situ analysis

die-resolved structure quantification

- **By connecting in-situ and ex-situ metrology, we can determine the critical layer parameters of increasingly complex layer structures at die-level**
- **method presented here for GaN-on-Si examples also valid for many other device types (VCSELS, µLEDs, …)**

Acknowledgements

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  Johannes Zettler, Thomas Zettler

Knowledge is key

www.laytec.de

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