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# Silicon MOSFETs and IGBTs: evolving for the future

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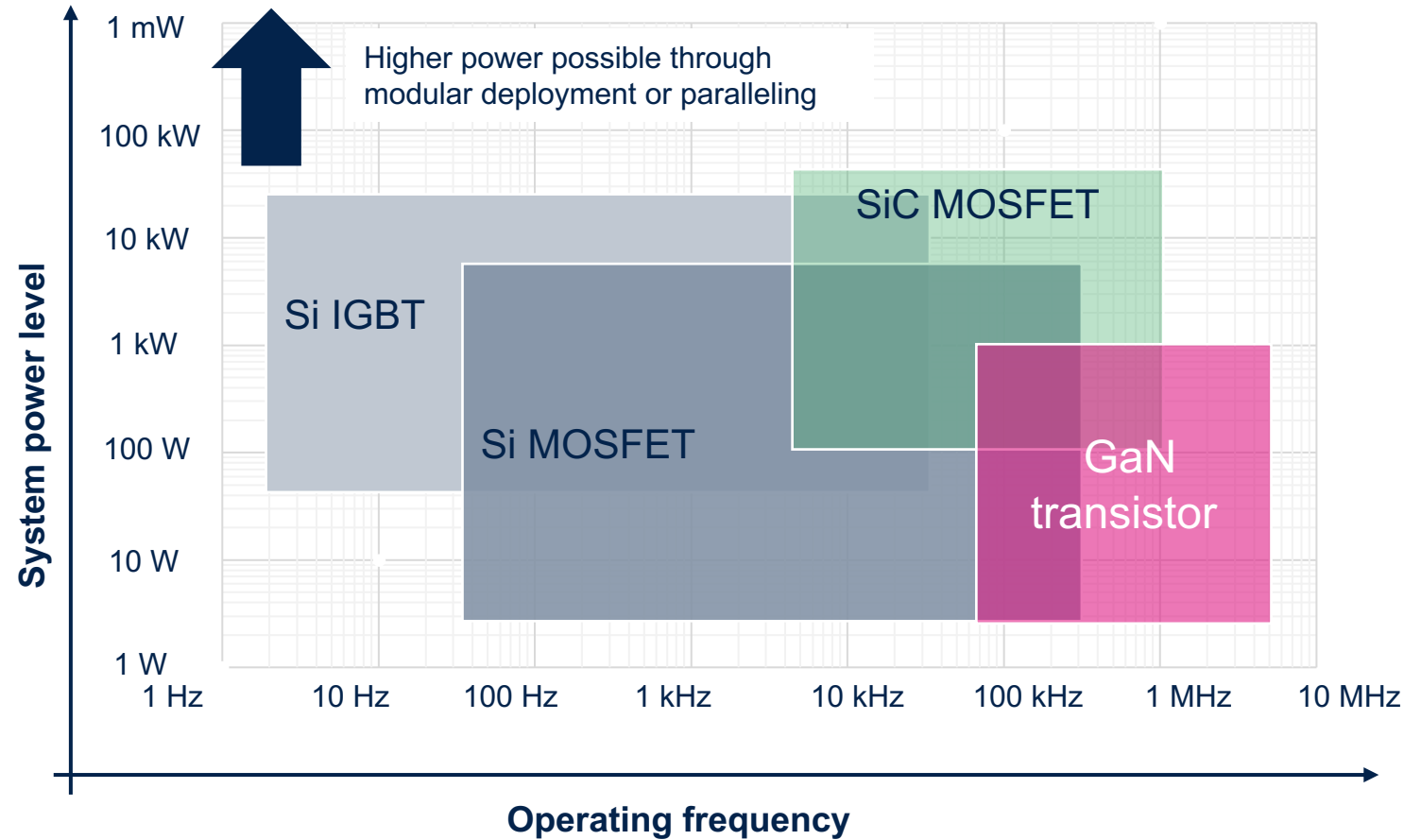
Power Transistor sub-Group

Strategic Marketing Manager

STMicroelectronics



# Power transistor technologies



## Applications



Telecom rack



Server



Renewable



Charging station



Energy storage



On Board charger



DC-DC converter



Traction



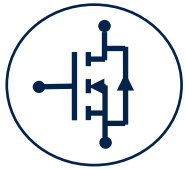
# Silicon MOSFET: From planar toward new structures





# A power MOSFET operates like a switch

Power MOSFET: key player in all applications handling power

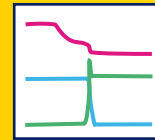


## Main parameters impacting performance

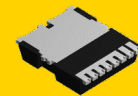
- $R_{DS(on)}$  (On-state resistance) [ $\Omega$ ]
- $Q_G$  (Total gate charge) [nC]
- Package
- Breakdown voltage,  $BVDSS$
- Threshold voltage,  $V_{th}$
- $dv/dt$  capability, output capacitance, more...



$R_{DS(on)}$  impacts conduction losses



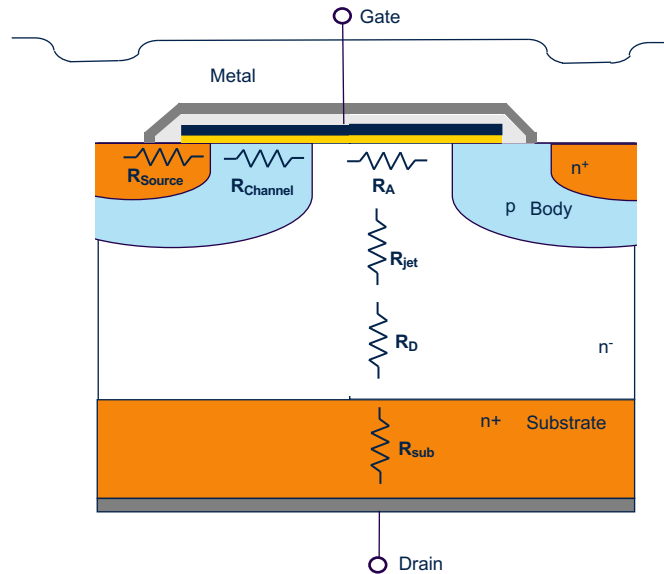
Gate charge  $Q_g$  impacts switching losses



Package impacts power density

# Planar MOSFET

## Conventional structure

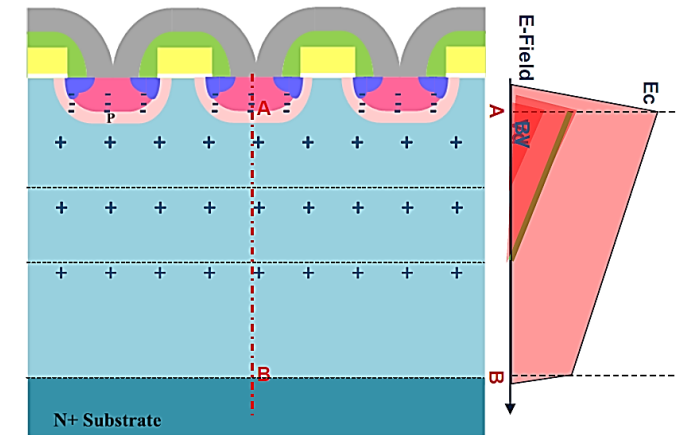


$$R_{DSon} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub}$$

## $R_{DSon}$ contribution

BVDss	30V	100V	600V
$R_{channel}$	35%	8%	3%
$R_{epitaxial}$	35%	88%	93%
$R_{substrate}$	30%	3%	2%

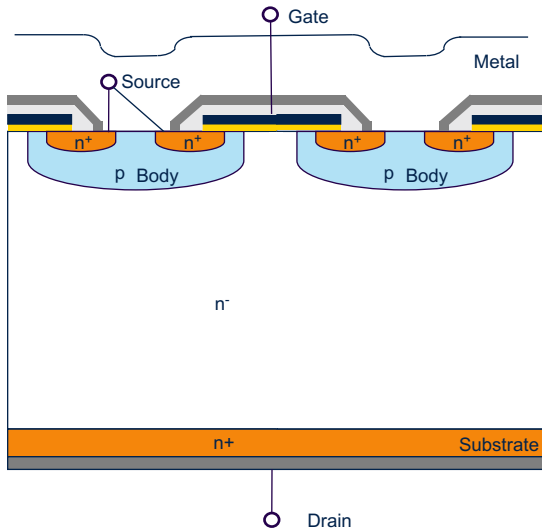
## Electric field



- $R_{DSon}$  is due mainly to the epi-region for high voltage MOSFETs
- The breakdown voltage is determined by the epitaxial layer (drift layer) doping concentration and its thickness

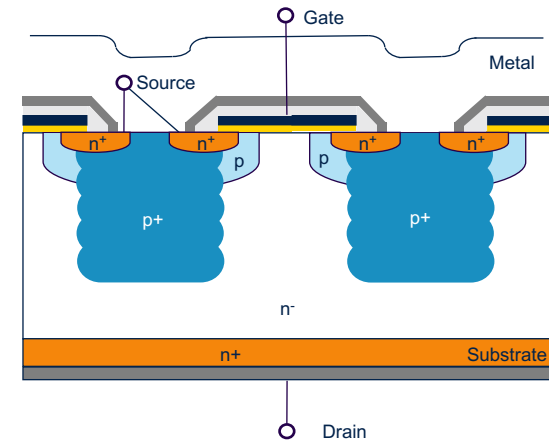
# MOSFET evolution

## Planar



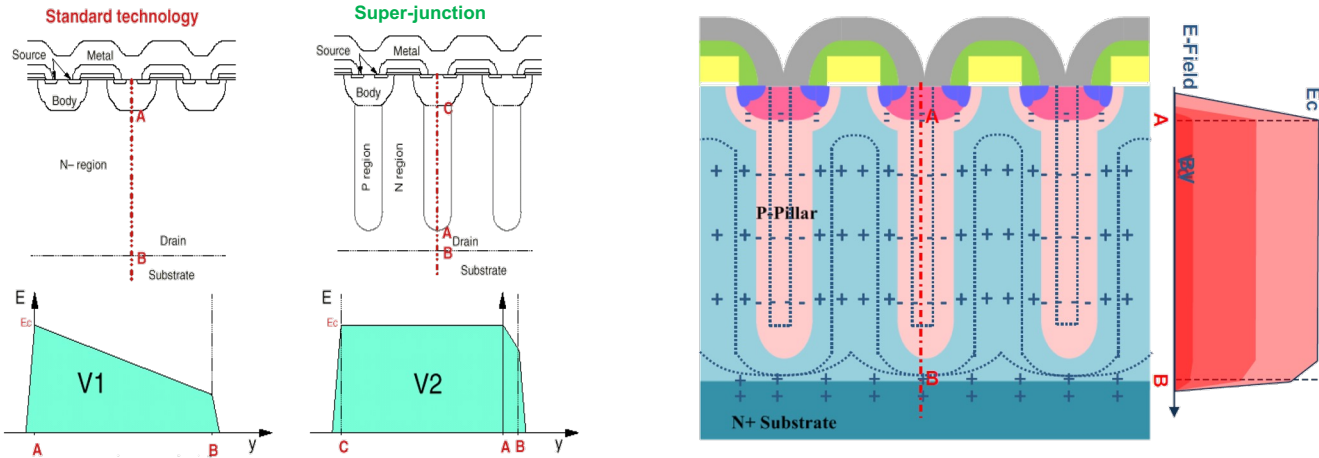
- **Thermal performance** ( $R_{th}$ )
- **Low electromagnetic** effects
- **Extended SOA**

## Super-junction



- **Better control** of the dynamic behavior
- **Improved performance** like lower conduction and switching loss
- Significant  **$R_{th}$  reduction** due to very thin die

# From planar to superjunction structure



## Comparison @ same BV<sub>dss</sub>

Parameter	Planar	Multidrain
Drift doping layer		<b>Higher</b> Increasing dopant concentration
R <sub>DSon</sub>	Related to Epi layer	<b>Lower</b> Epi layer reduced
Electrical Field	Variable During the n region	<b>Higher</b> Increased by column structure

$$V(x) = \int E(x)dx$$

Poisson's Law

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\epsilon_s} = \frac{qN_A}{\epsilon_s}$$

N<sub>A</sub>= Charge density

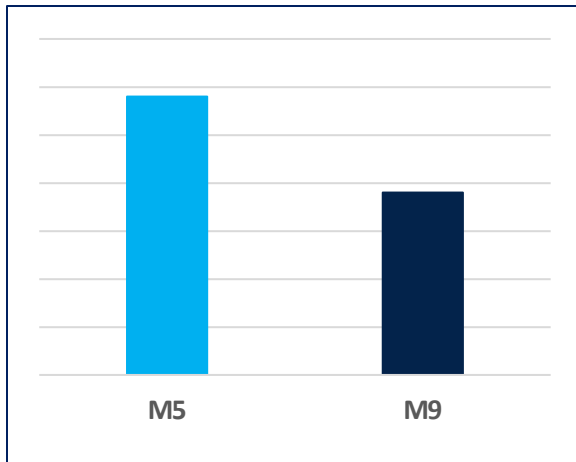
ε<sub>s</sub>=permittivity

## Benefits

- Higher current density
- Lower Z<sub>th</sub>
- Suitable for low thickness packages

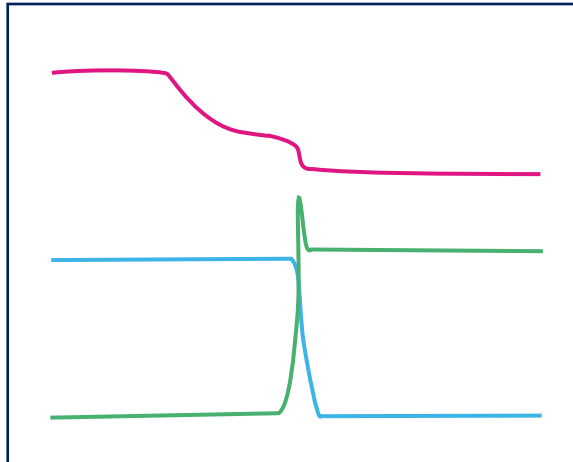
# Main features

## $R_{DS(on)} * \text{Area}$



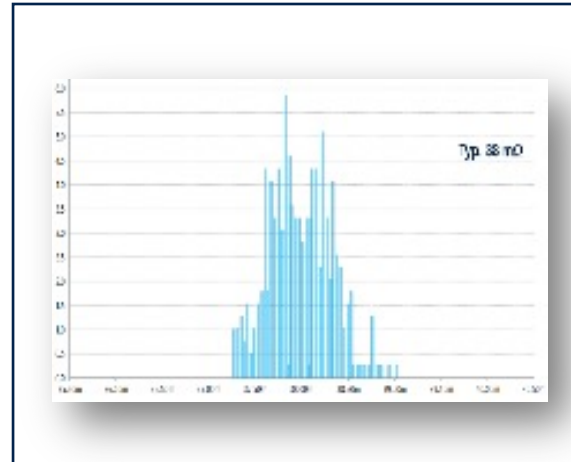
- Very low  $R_{DS(on)}$  per area
- Suitable for hard-switching topologies
- Best choice for resonant high power density systems

## Power losses



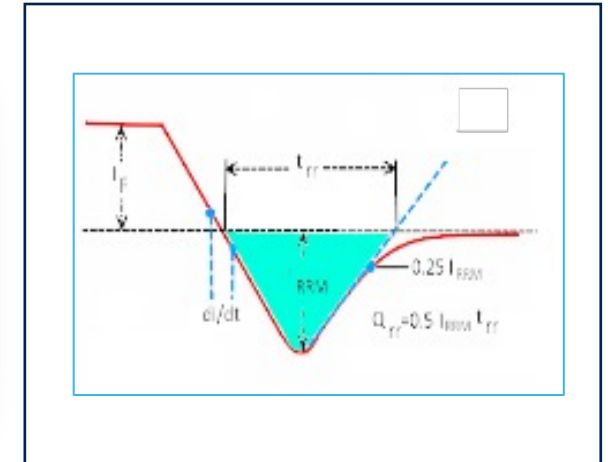
- Reducing switching energy losses
- Reducing switching time
- Increasing switching frequency

## Process



- Reduced  $BV_{dss}$  spread <70V
- Reduced  $V_{th}$  spread <1V
- Higher reliability

## Robustness

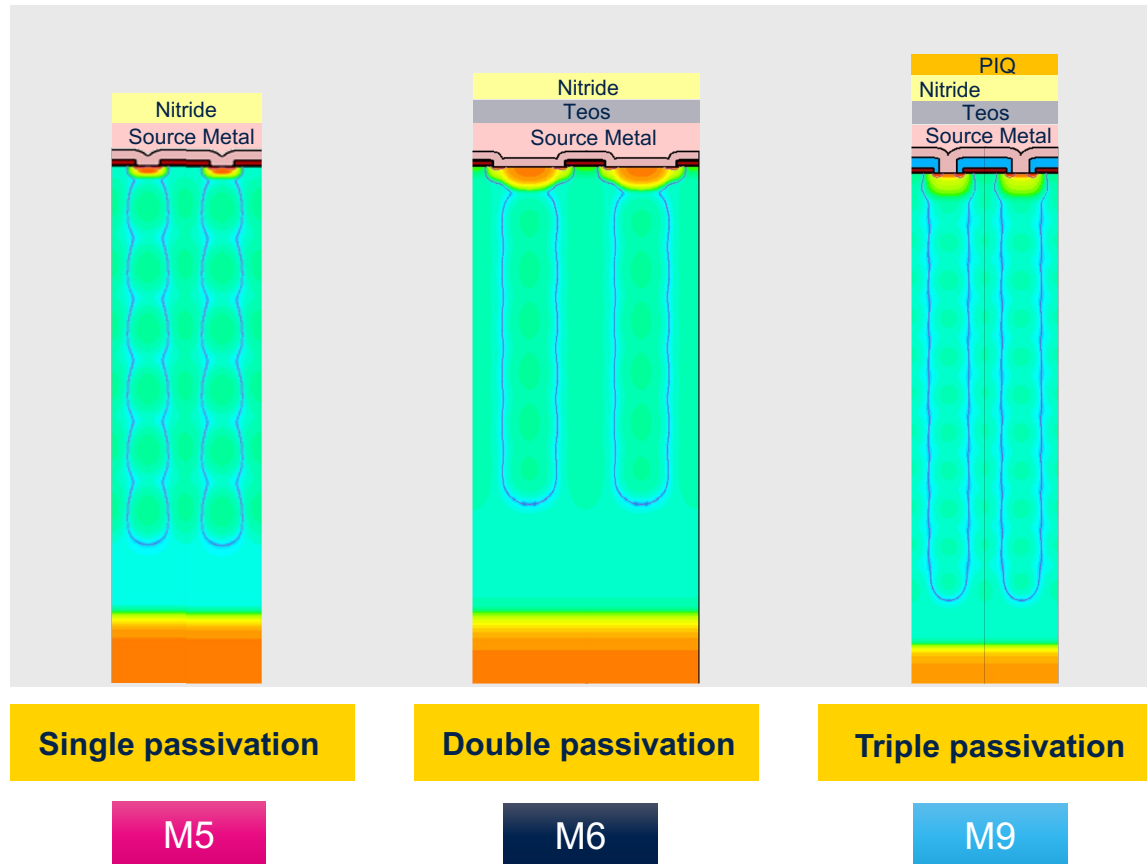


- Static  $dv/dt$  up to 120V/ns
- Dynamic  $dv/dt$  up to 50V/ns
- Dynamic  $dv/dt$  up to 120V/ns



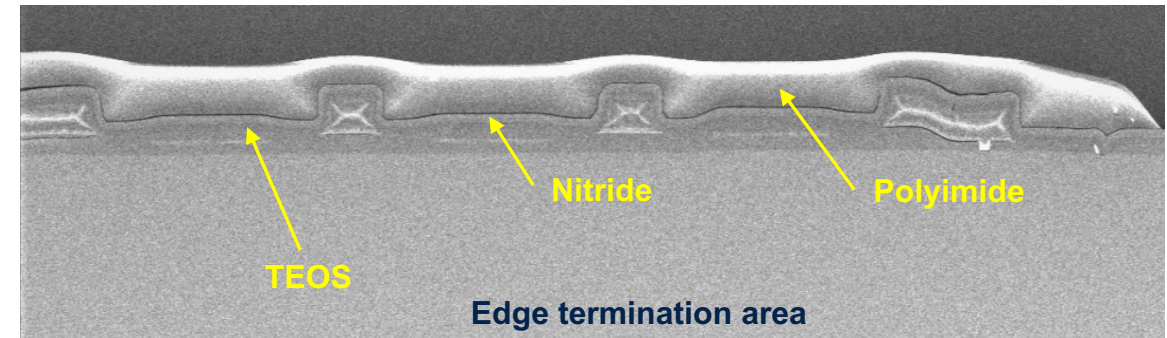
# MOSFET evolution

## Active area: cell structure comparison



## Passivation layers optimization

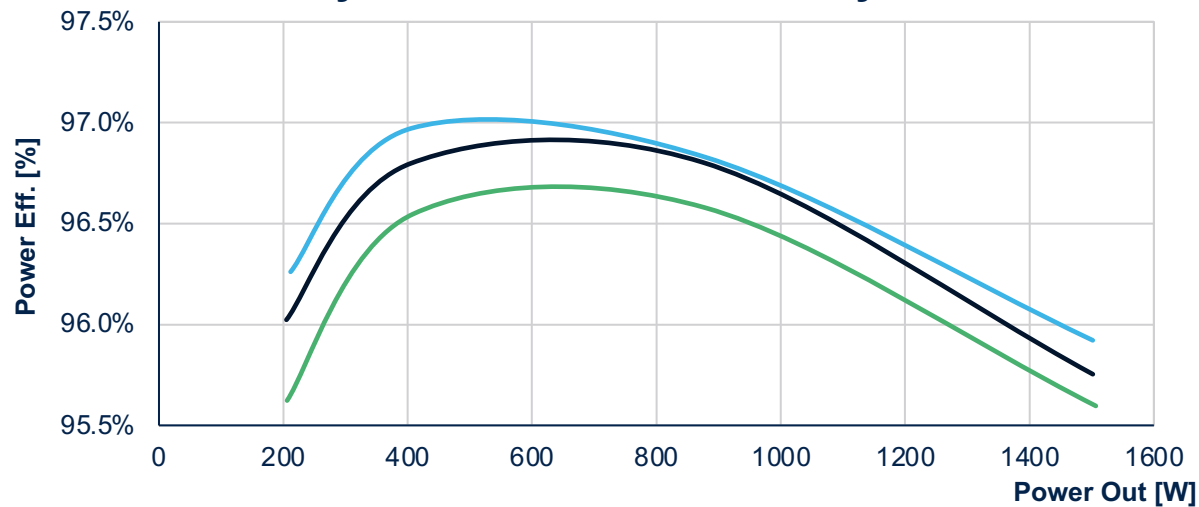
- **Nitride** is an excellent and common passivation layer
- **Teos** layer to reduce Nitride stress
- Extra **polyimide** layer (organic polymer that exhibits excellent mechanical properties and electrical insulation) to reduce the mechanical stress coming from BE processes



# Application test and analysis

## Power factor corrector (PFC) 1500W

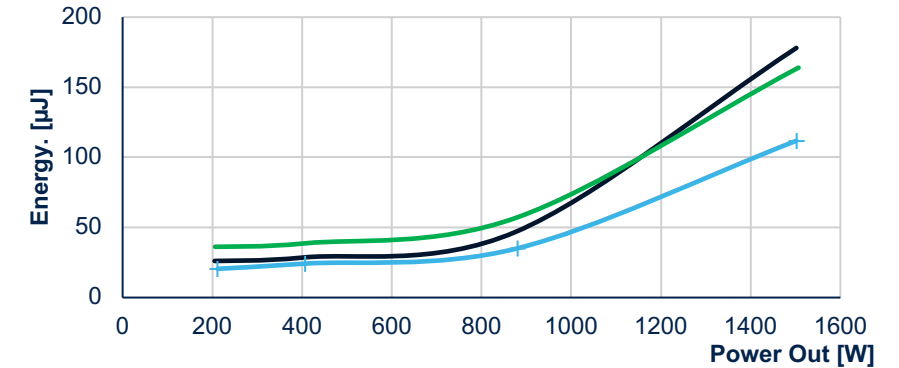
### System Power Efficiency



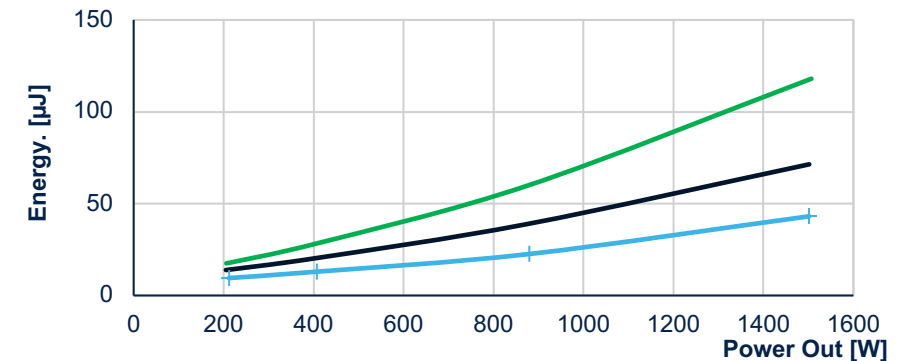
■ M9 ■ M6 ■ M5

Device	BVdss [V] @ 1mA	Vth [V] @ 250uA	R <sub>DS(on)Max</sub> [mΩ]*	Qg [nC]
MDmesh M9	650	3.7	45	80
MDmesh M6	600	4	41	106
MDmesh M5	650	4	45	143

### E<sub>off</sub>



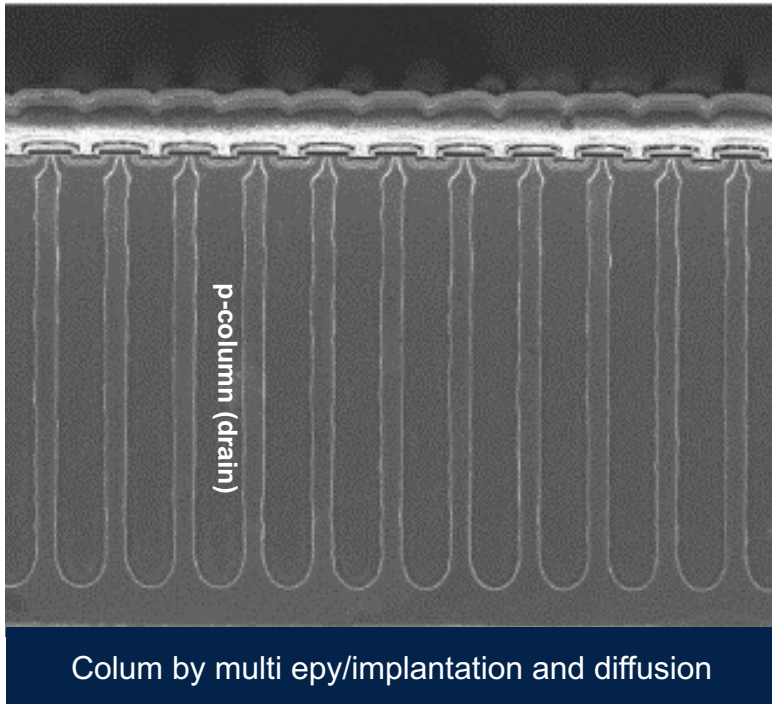
### E<sub>on</sub>



New technology maximizes system efficiency and thermal performances

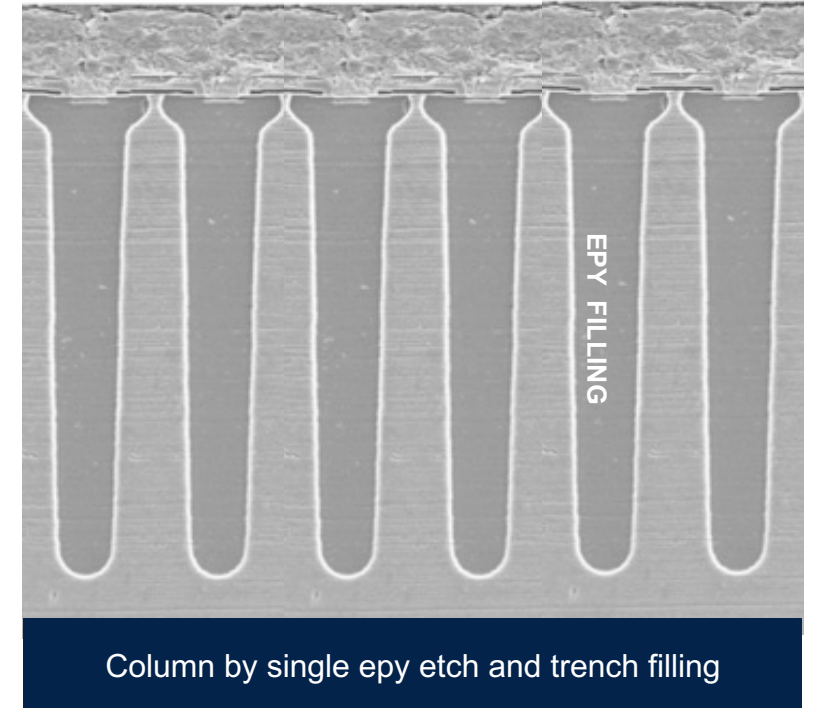
# What is next for superjunction?

## Multidrain approach



From multi-epitaxy to  
"dig & fill" approach

## Trench approach



- Reduced mask levels
- Single epitaxy
- No thermal process for column formation

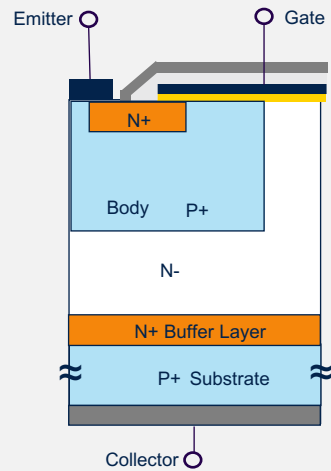


# IGBT: Evolution of a technology



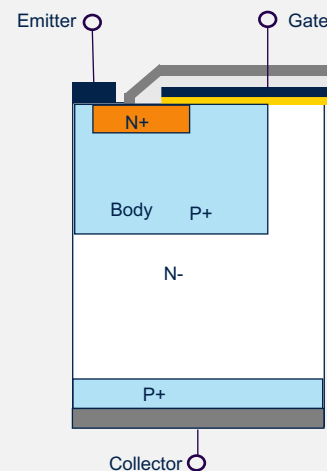
# IGBT technology

## Punch through



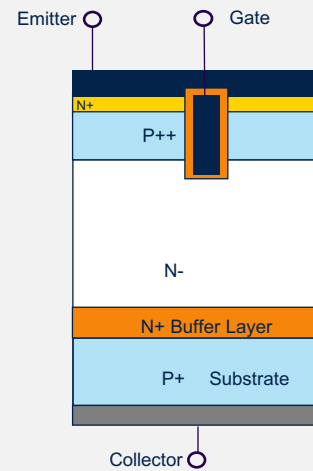
- First IGBT structure
- Faster, but higher  $V_{CEsat}$
- Large  $E_{off}$

## Non-Punch through



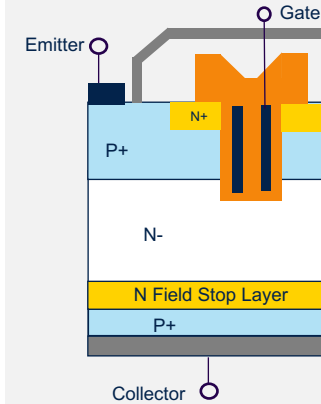
- Thinner substrate
- Lower thermal resistance,
- Lower  $E_{off}$

## Trench PT



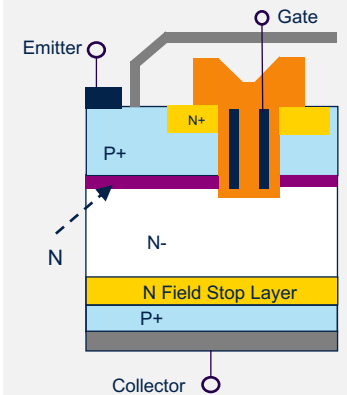
- Vertical Gate
- Optimized channel design
- Lower  $V_{CEsat}$
- Higher current density

## Field-stop



- no tail current
- Reduced switching losses
- Decreased  $V_{CEsat}$
- Thinner n-drift region

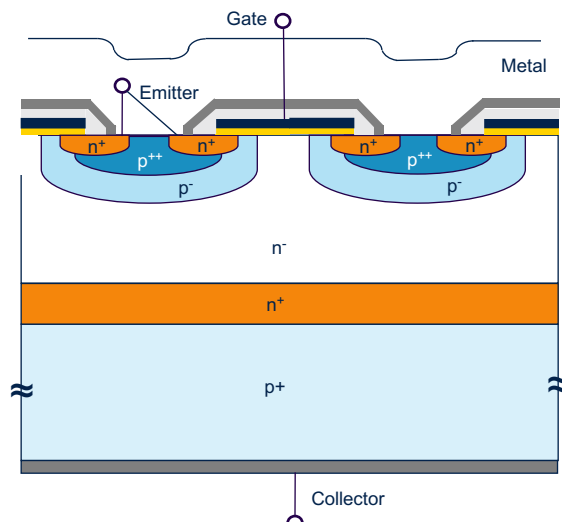
## Hole barrier



- Lower  $V_{CEsat}$
- N+ layer removes JFET resistance
- Carried stored layer fastens turn-on switching ability

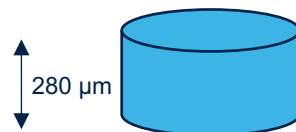
# IGBT evolution

## Punch through (PT)

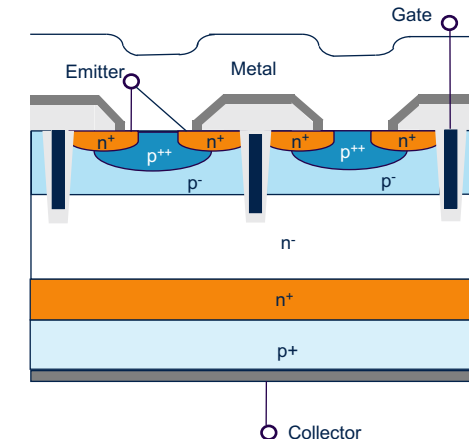


- Asymmetrical configuration
- Low conduction loss
- Less thermal stability

- Not preferred for parallel
- Low switching losses
- Mostly used in DC circuits



## Trench field stop (TFS)



- Absence of JFET region
- Higher current density
- Lower  $V_{CEsat}$

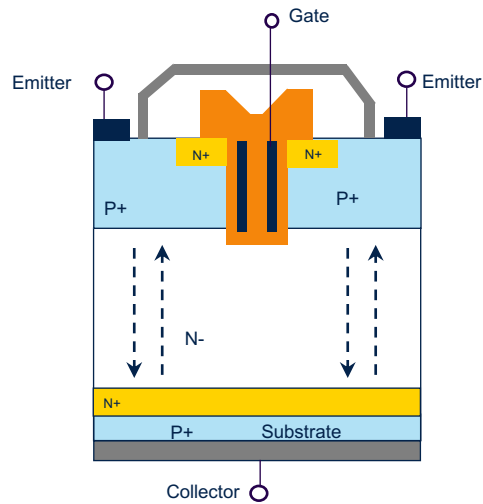
- Implantation of FS and emitter
- Better  $V_{CEsat}/E_{off}$  control
- No need  $\beta$ - irradiation

Parameter	Planar PT	Trench field stop
Switching losses	Low	Low
Conduction losses	High Slightly decrease with T	Low increase with T
Paralleling	Difficult Small positive T coefficient	Easy Positive T coefficient
Short circuit rated	Limited High gain	Yes
i.e. $V_{cesat}$ @10A	2.8V	1.6V

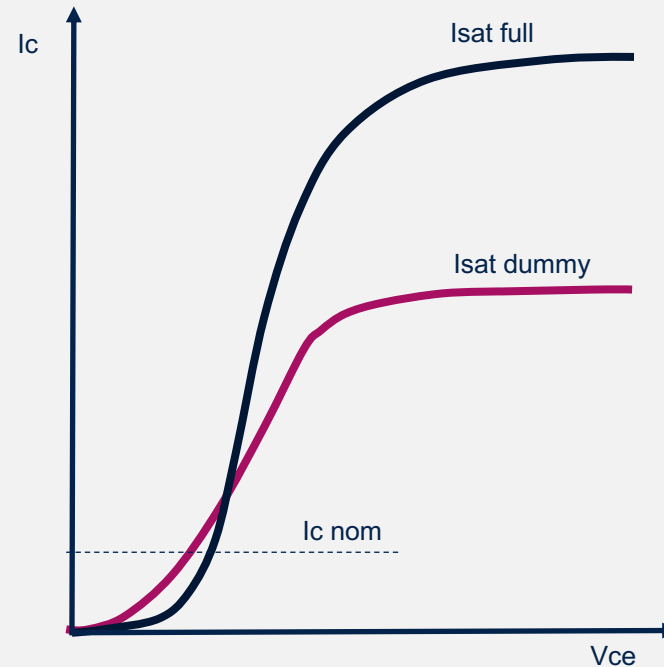


# Trench layout strategy

## Full active

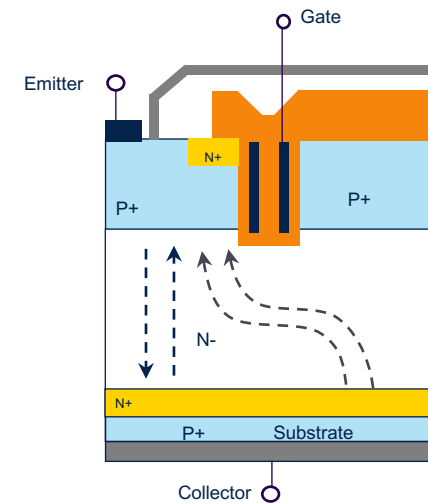


## Output curves



Trench pitch	Full Active	Dummy Cell	Extra Dummy
4 $\mu$ m	4 (low, fast)	4 + 4 (medium, fast)	--
8 $\mu$ m	8 (medium, fast)	8 + 8 (medium, fast, SC rated)	8 + 16 (medium, fast, strong SC rated)

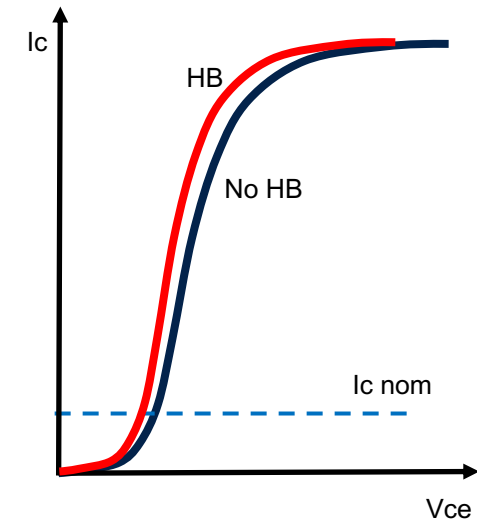
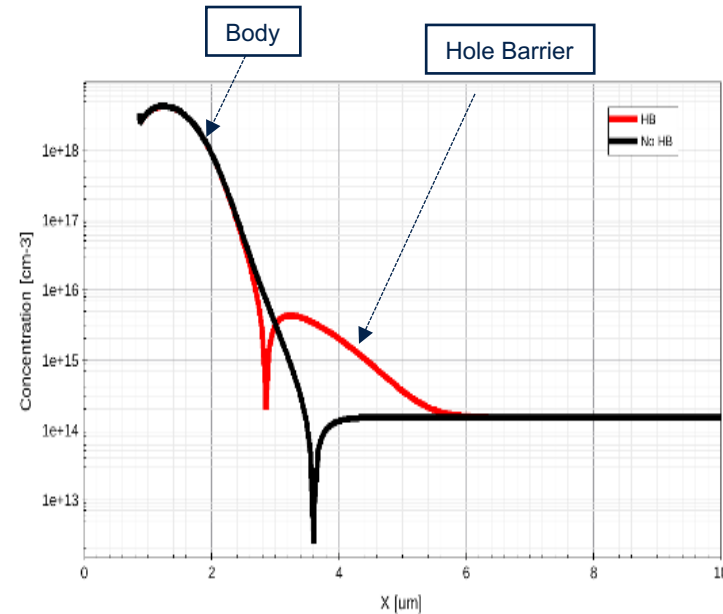
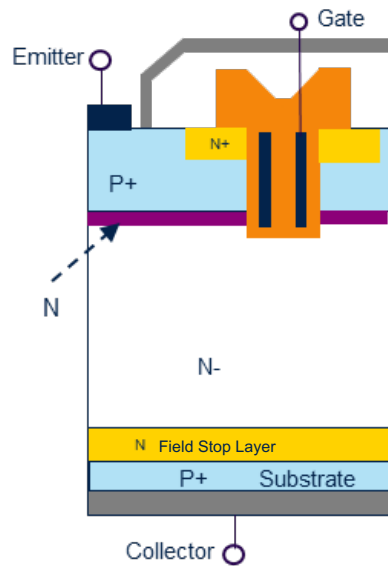
## Half dummy



- Lower active cell density
- Low Ciss, Coss, Crss
- Lower saturation current
- Improved Tsc

# What's next in Trench Field Stop?

## Hole Barrier Structure



- Process Option
- Additional Mask
- Additional Implant Phosphorus
- New vertical profile with additional N-type layer that enhances the majority carriers and so improving the ON state losses

### Benefit

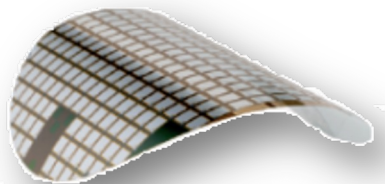
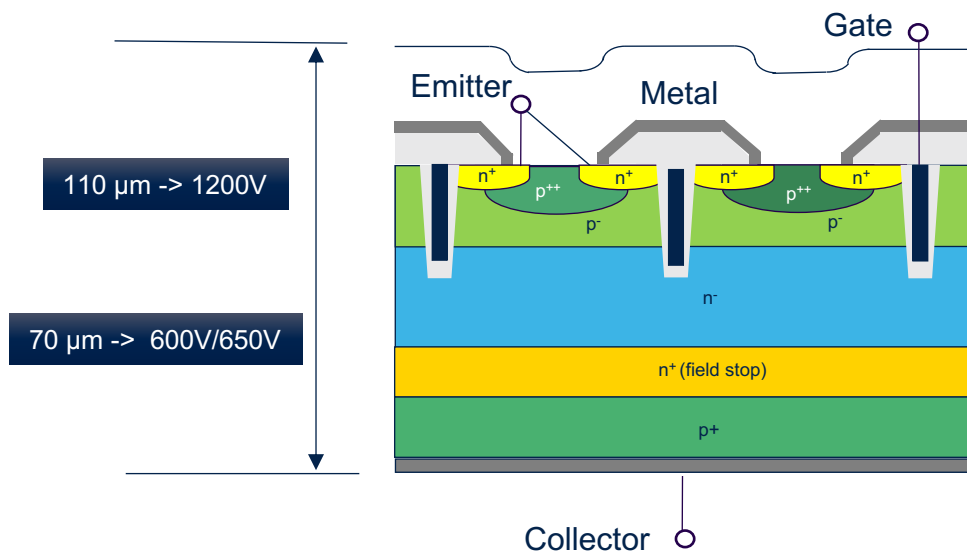
- lower  $V_{ce,sat} \sim 180\text{mV}$

### Warning

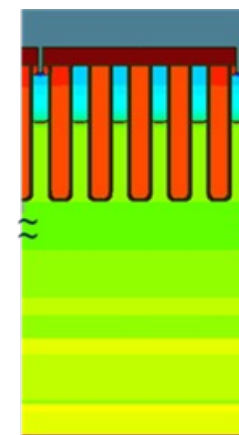
- $V_{th}$  lowering to be retuned
- $BV_{ces}$  lowering

# Narrow Mesa II

## Trench field-stop



## Narrow Mesa II



80 μm → 750V

### Technology features

- Very fine cell pitch
- Trench potential engineered
- Multiple deep field stop

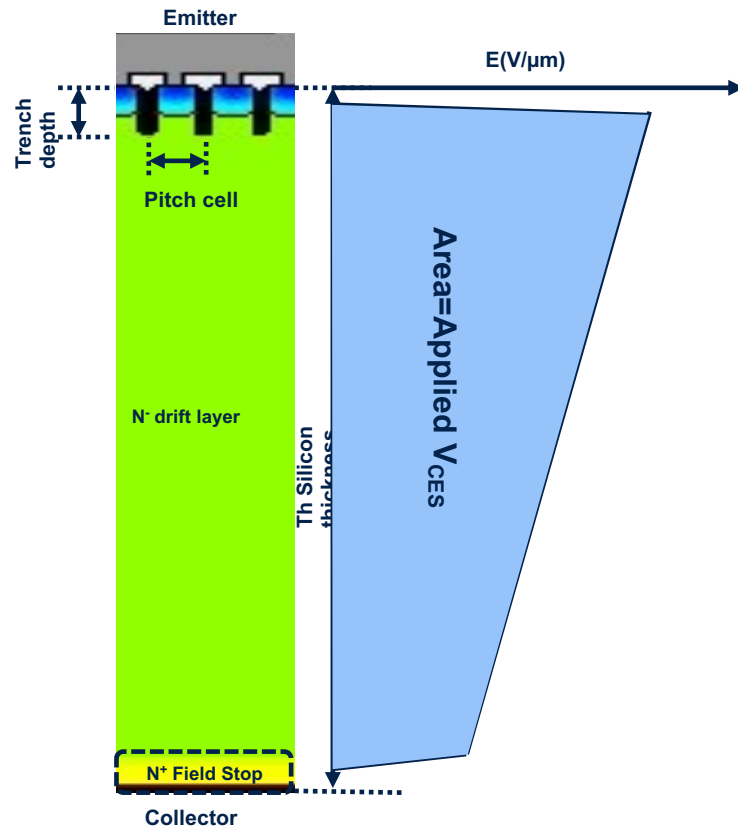
### Benefits

- Lower  $V_{CEsat}$
- Higher current density:
- Better  $V_{CEsat}/E_{off}$  trade-off
- Smoother turn-off

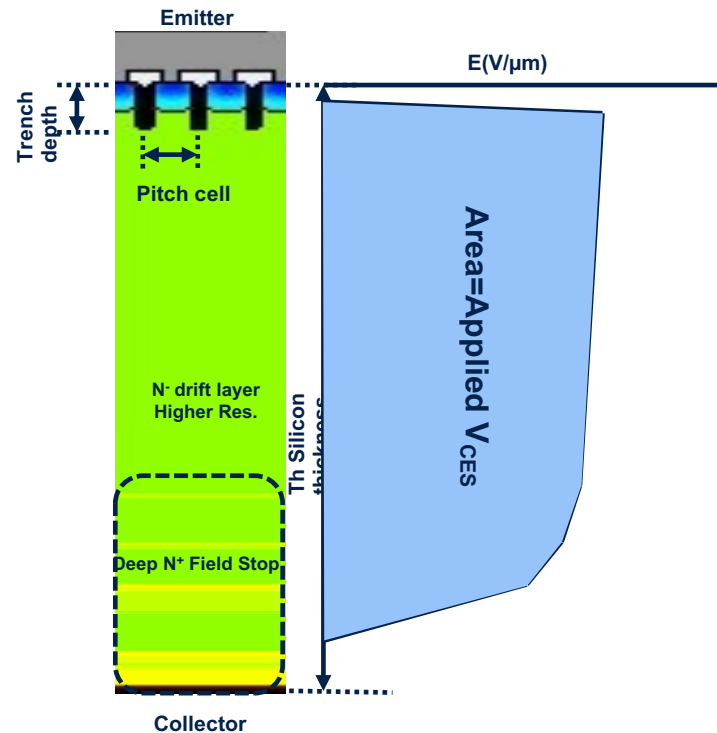


# Main features to improve $V_{CEsat}$ and Turn off

## Trench field-stop



## Narrow Mesa II



### N-Drift Lower Thickness, Higher Resistivity:

- to guarantee the same  $BV_{CES}$ ;
- to improve  $V_{CEsat}$ ;

### Field Stop Design:

- to improve turn-off in thinner wafer;

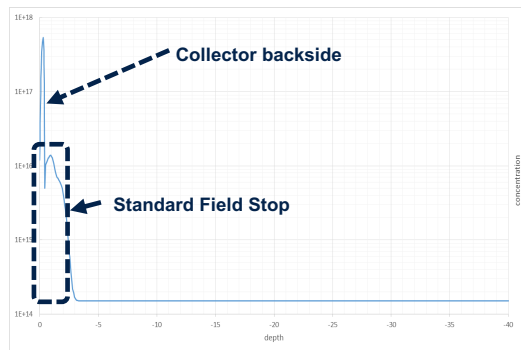
### Main other upgrades:

- Nitride + Polyimide Passivation
- Backside Emitter Activation by Laser Annealing
- Tune-up of the Emitter Efficiency on Collector Backside for the right the trade-off;

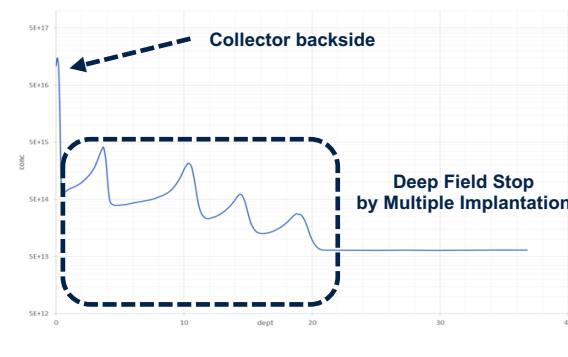
# Static electrical improvements

## Electrical field: Vertical profile

### Standard N+ Field STOP



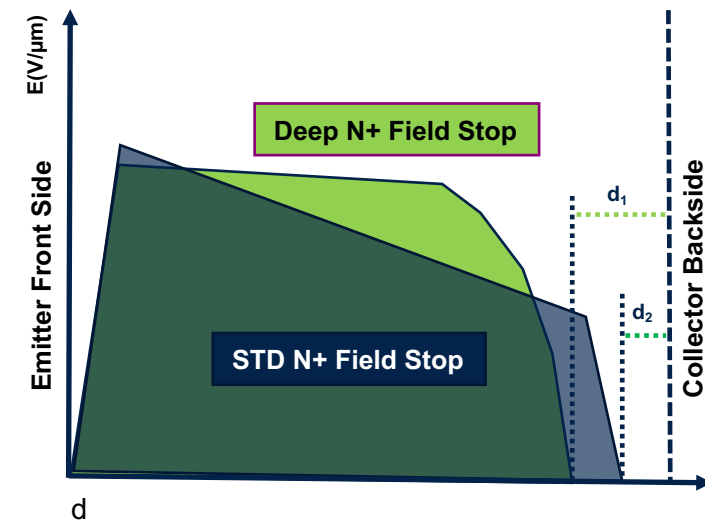
### Deep N+ Field STOP



#### Deep Field Stop Layer;

- To gradually block the electric field near the collector side;
- To reduce  $V_{CE}$  peak at turn-off when “reducing the wafer thickness”;

## Narrow Mesa II



#### Electric field in high voltage withstanding

- Multiple field-stop profile shows better resolution of field slope-down to have more robust devices
- Higher efficiency voltage withstanding

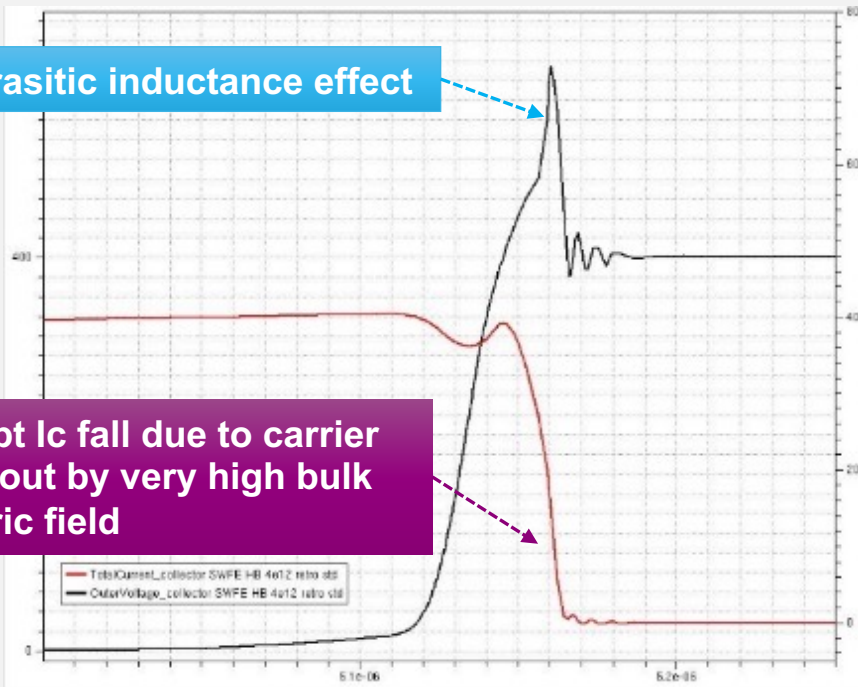
# Dynamic electrical improvements

## Turn OFF simulation

### Standard field stop profile

Parasitic inductance effect

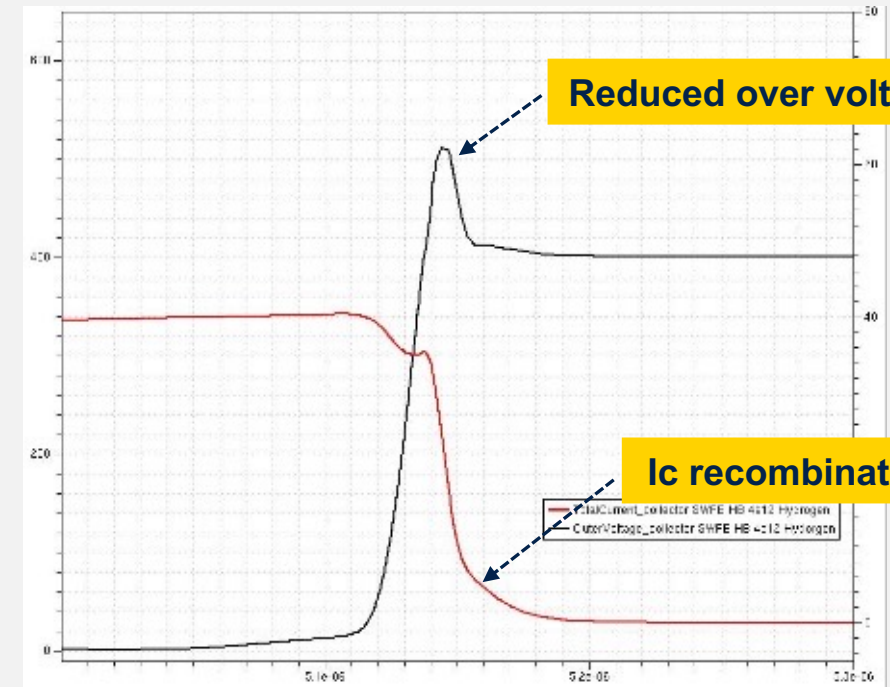
Abrupt  $I_c$  fall due to carrier wipe-out by very high bulk electric field



### Multiple field stop profile

Reduced over voltage

$I_c$  recombination tail



Multiple field stop design profile technique is used to control the carrier's lifetime improving performance by reducing overvoltage during switching events



# Takeaways

- **Silicon technologies** span an extensive market, from industrial to automotive sectors
- The **wide product portfolio** targets from low to high power range and from low to high frequency operation
- **New structures** and concepts allow to take up new challenges
- New technologies are one of the key contributors for the **green economy**

# Our technology starts with You

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