ANGELTECH CS INTERNATIONAL CONFERENCE

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Unspoken Impacts of SiC Power Packaging

MICROCHIP

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

Dr. Kevin Speer | *Technology Director, SiC Business*

16 April 2024

SMART | CONNECTED | SECURE

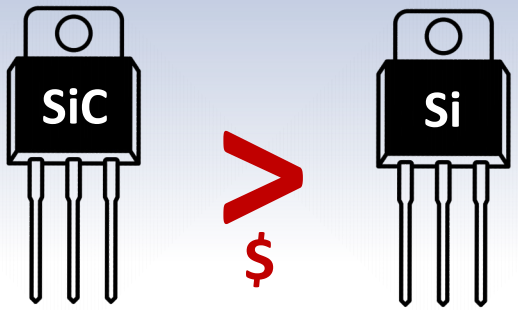
Outline

- SiC Packaging: Why must it be different?
- Power loops and parasitic inductance
- Optimizing SiC performance with low inductance
- Layout possibilities of the SP6LI power package
- Summary

SiC Packaging: Why must it be different?

Narrow view

SiC more expensive than silicon



Big picture view

SiC systems can be less expensive than silicon, PLUS…

In addition to cutting their cost, SiC can make systems:

- More efficient
- Last longer
- More rugged
- Smaller and lighter

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SiC Packaging: Why must it be different?

Customer Wishes = Packaging Requirements

More efficient, lower cost of use

- Lower parasitic inductance for faster switching and minimal switching losses

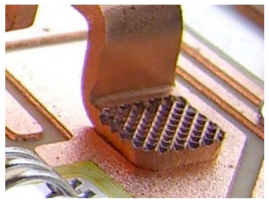
Smaller and lighter

- Enhanced heat removal for increased power density
- Lower parasitic inductance for smaller passive components

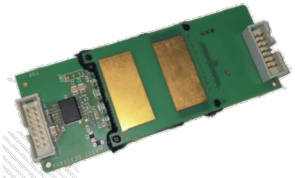
NEW PACKAGING REQUIRED

Longer lasting, more resilient

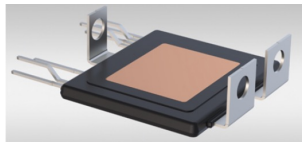
- Better materials for die attach and interconnect to extend cycling lifetimes
- Robust technologies for harsh environments
- Suitability for high voltages and currents



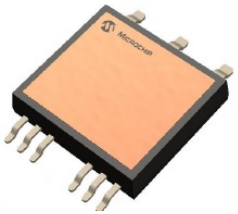
Terminal Welding



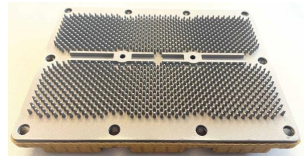
PCB Embedding



Double-Sided Cooling



Molding



Integrated Cooling

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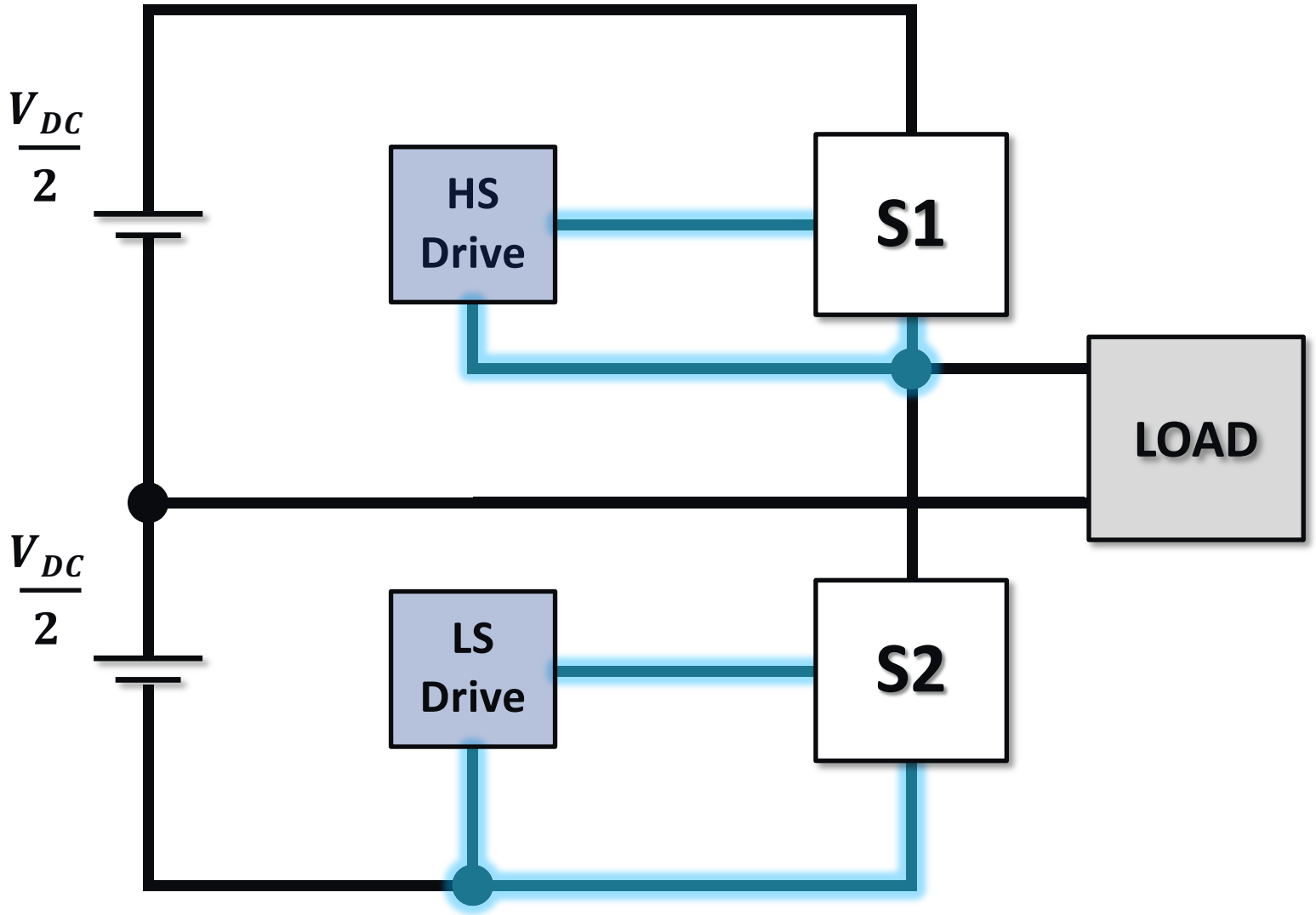
Performance Car With a 30 mph Speed Limit

- SiC is special because it can block high voltage AND switch at high frequency
- “Si-based packaging” limits the user’s ability to unleash the full advantage of SiC
- Room for packaging improvements in thermals, cycling reliability, and inductance

Today we focus on inductance:

1. Overview of inductances in a power circuit
2. Demonstration of enhanced performance in SP6LI

Overview of Power System Loops

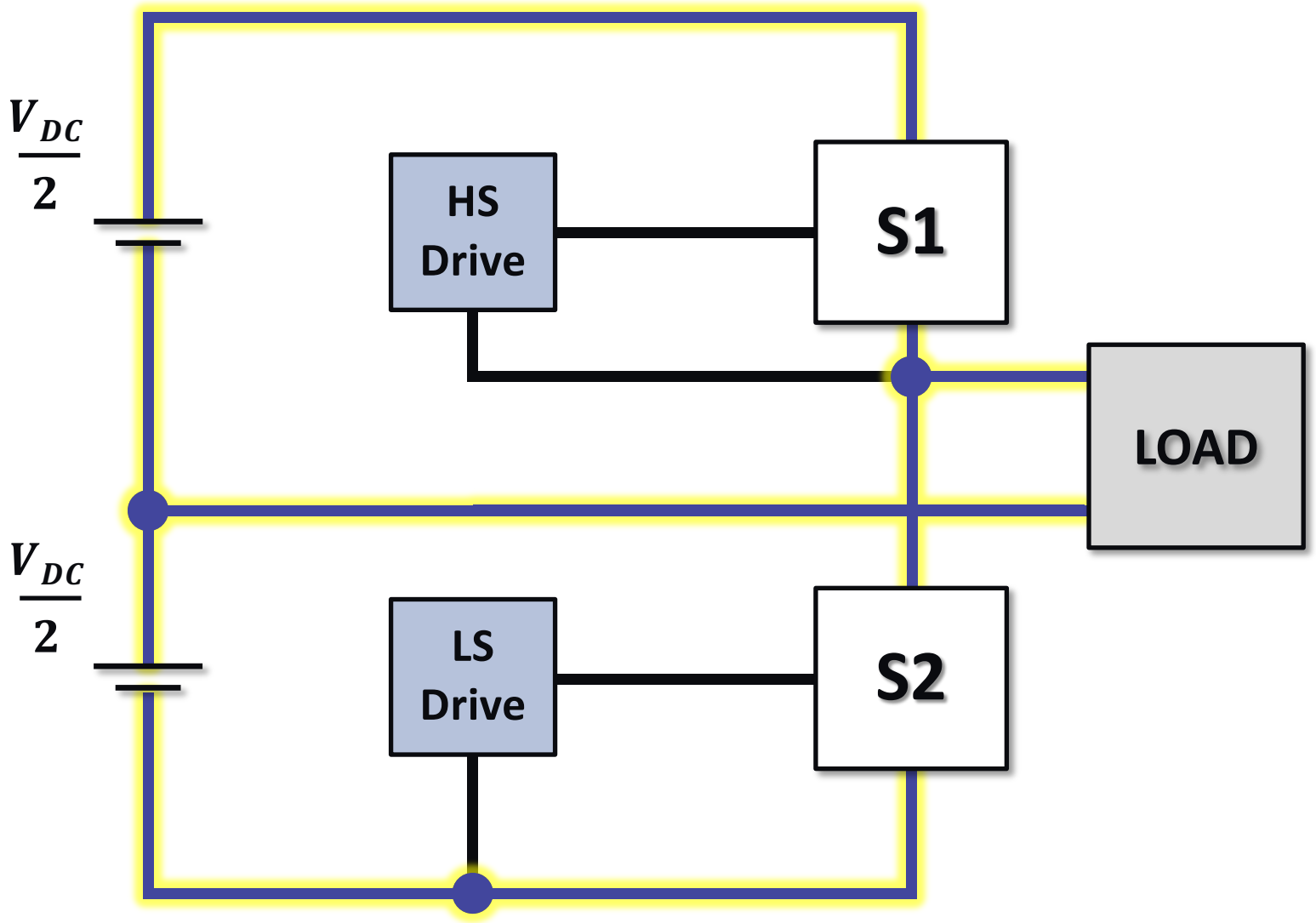


Consider…

At a high level, the power system has two major loops…

Gate-source loops

Overview of Power System Loops



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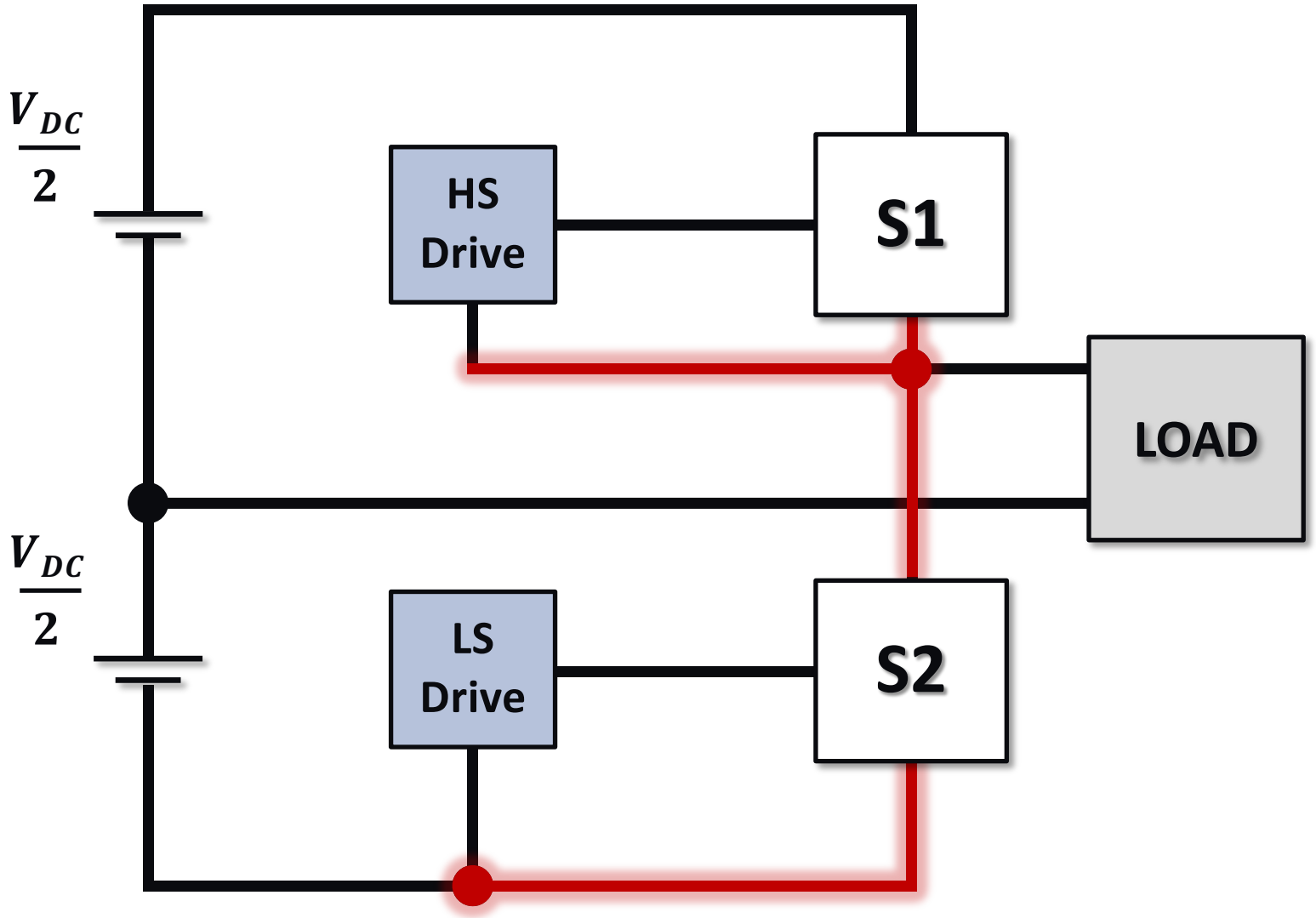
Gate-source loops

Power loops

Overview of Power System Loops



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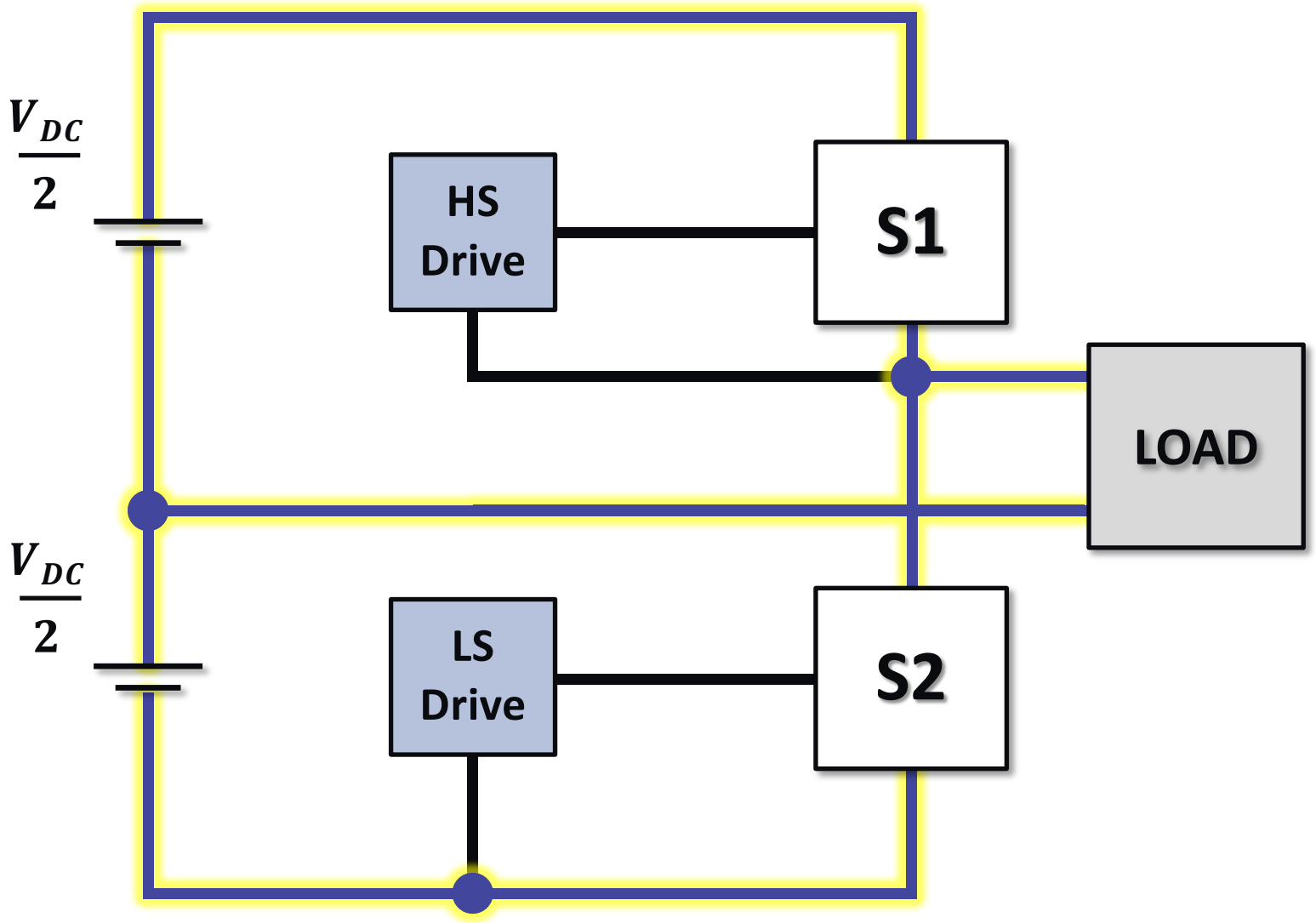
At a high level, the power system has two major loops…

Gate-source loops

Power loops

Common paths

Power Loop



Power loops

Components

L_{pwr} can include:

- the package (L_D and L_S)
- the overall parasitic inductance of the remaining power loop

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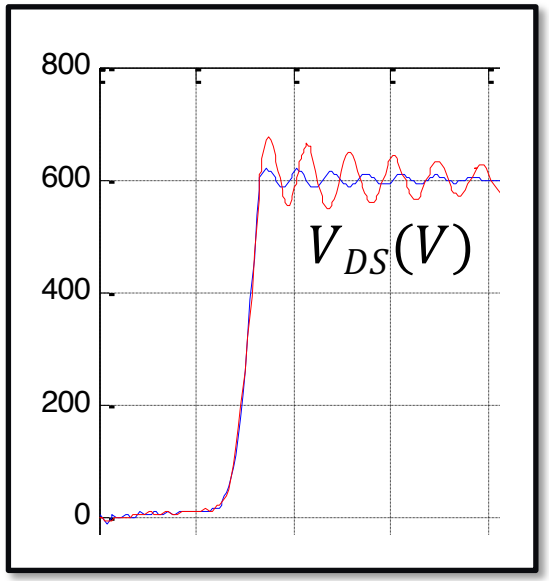
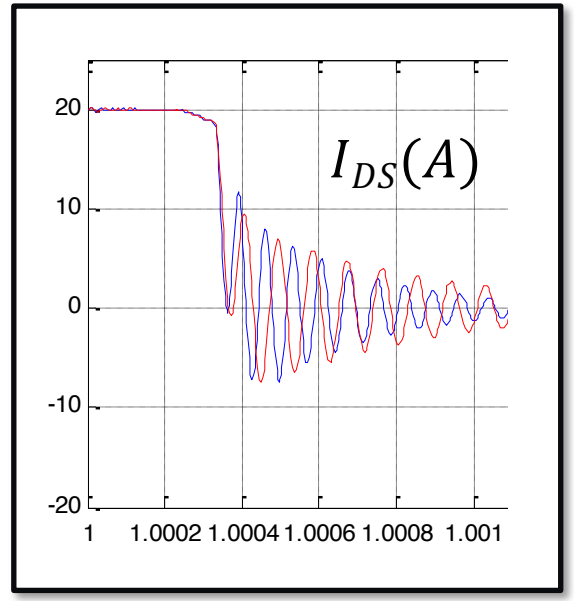
Problems with Power Loop Inductance



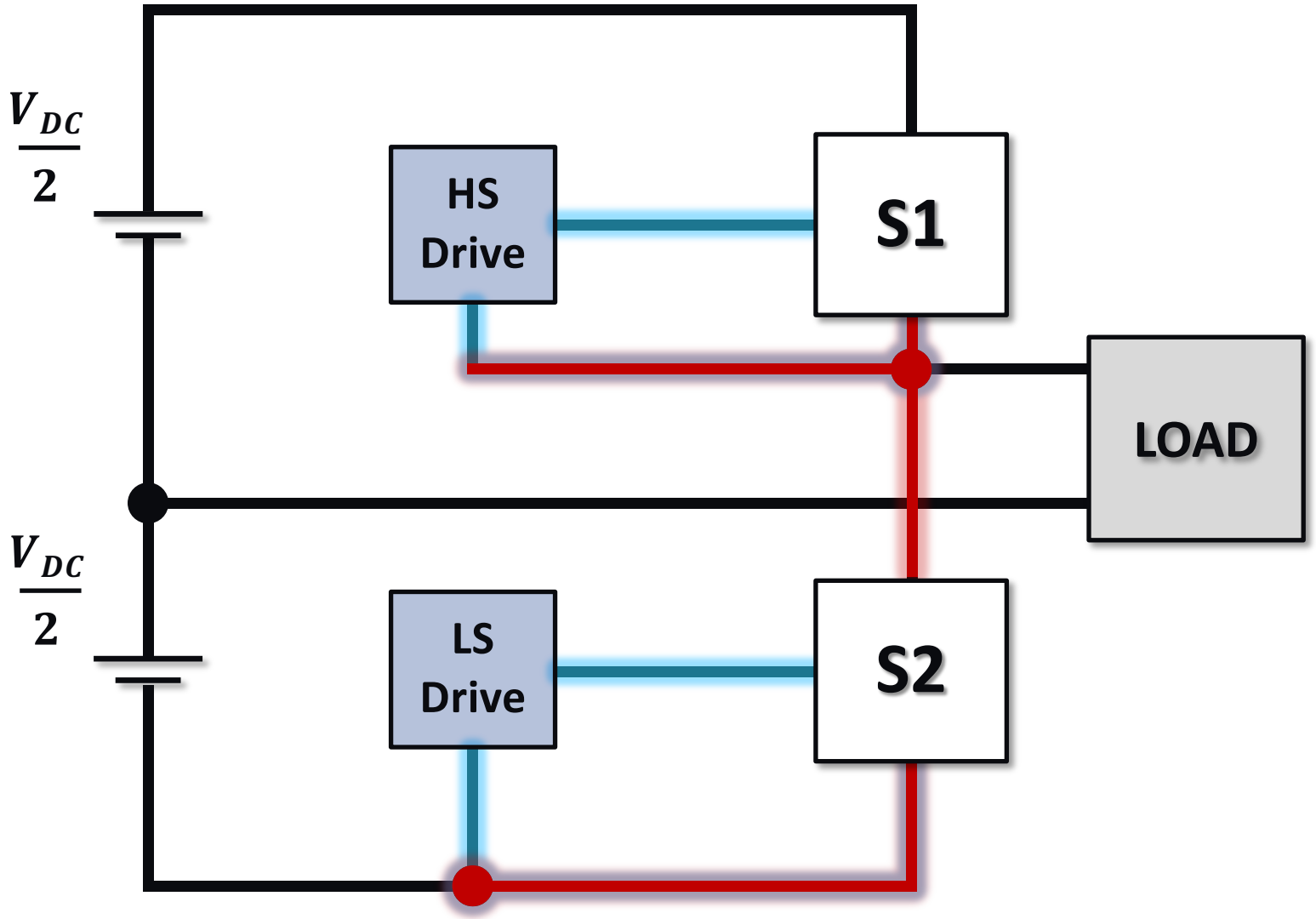
$L_{pwr} = 2$ nH
$L_{pwr} = 10$ nH

Problem 1 **Voltage overshoot**	Problem 2 **Switching oscillations**
Caused by combination of parasitic inductance and fast switching speeds (di/dt)	Caused by a resonant circuit that includes L_{pwr}
Even small values of L_{pwr} can cause V_{DS} to exceed design margins	Higher-order harmonics of the fundamental switching frequency
User must slow down switching speed, increasing losses; or…	Leads to higher switching losses
…select higher-voltage components (higher cost); or…	Can couple into nearby circuits radiatively or conductively, leading to malfunctions
…resort to more complicated, multi-level topologies (higher cost)	Users must incorporate filters to mitigate issues (higher cost, less power dense)



$L_{pwr} = 2$ nH
$L_{pwr} = 10$ nH

Gate Loop



Gate-source loops

Common paths

Components can include:

- the package (L_G and L_S)
- the overall parasitic inductance of the remaining gate-source loop
- Also introduced is the common source inductance, L_{csi}

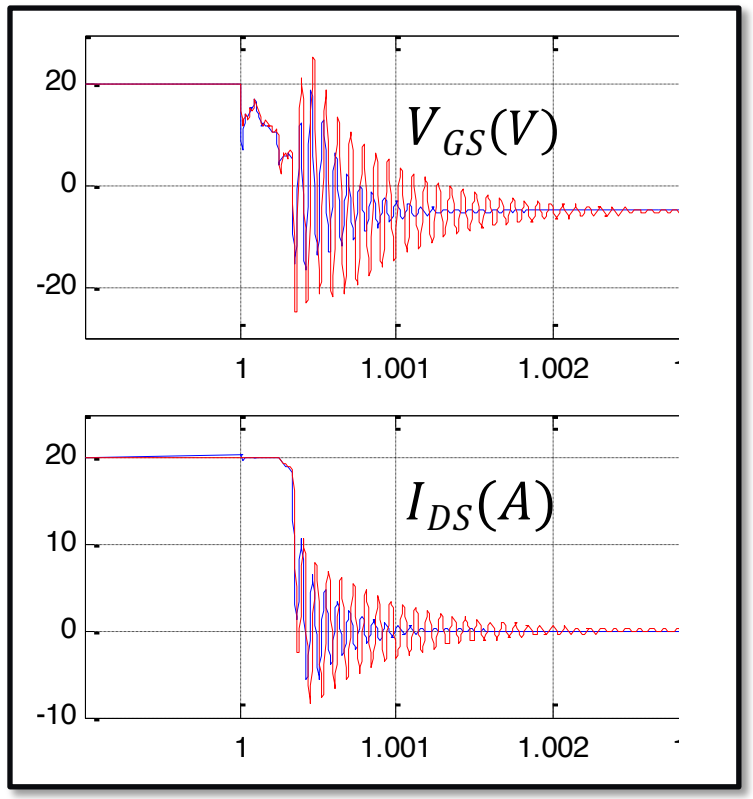
Problems with Gate Loop Inductance

Problem 1
V_G overshoot (high L_G, L_S)

Caused by combination of parasitic inductance and fast switching speeds (di/dt)

Can lead to inadvertent turn-on and catastrophic shoot-through

Excessive oxide fields can also induce device damage and limit lifetime

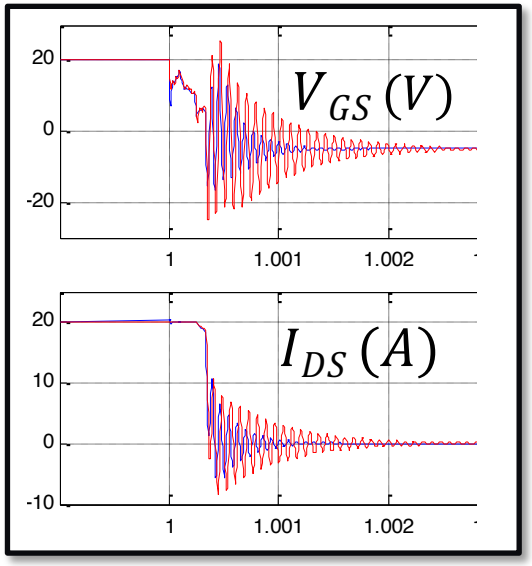


$L_G = 2\,nH, L_G = 10\,nH$

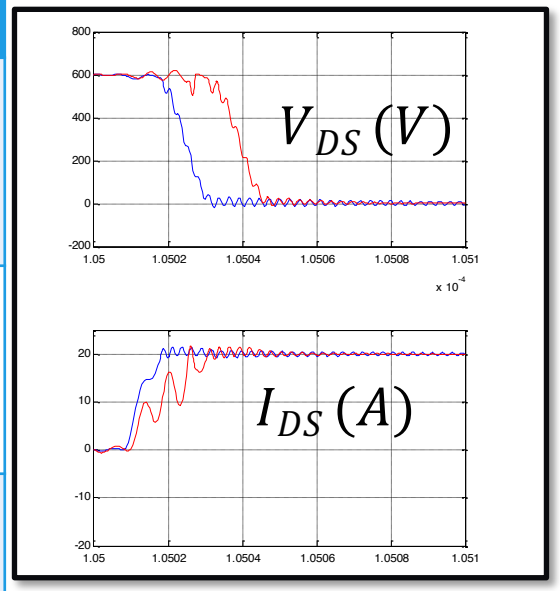
- Even low values of L_G result in V_{GS} oscillations well above V_{th}
- Oscillations in V_{GS} naturally lead to ringing in I_{DS}, which can give rise to EMC issues

Simulations using $V_{DC} = 60V,\ IL = 20A,\ di/dt = 2.5\ A/ns$, and $R_G = 5\Omega$.
1200V, 80 mΩ in TO-247-3L

More Problems: Common Source

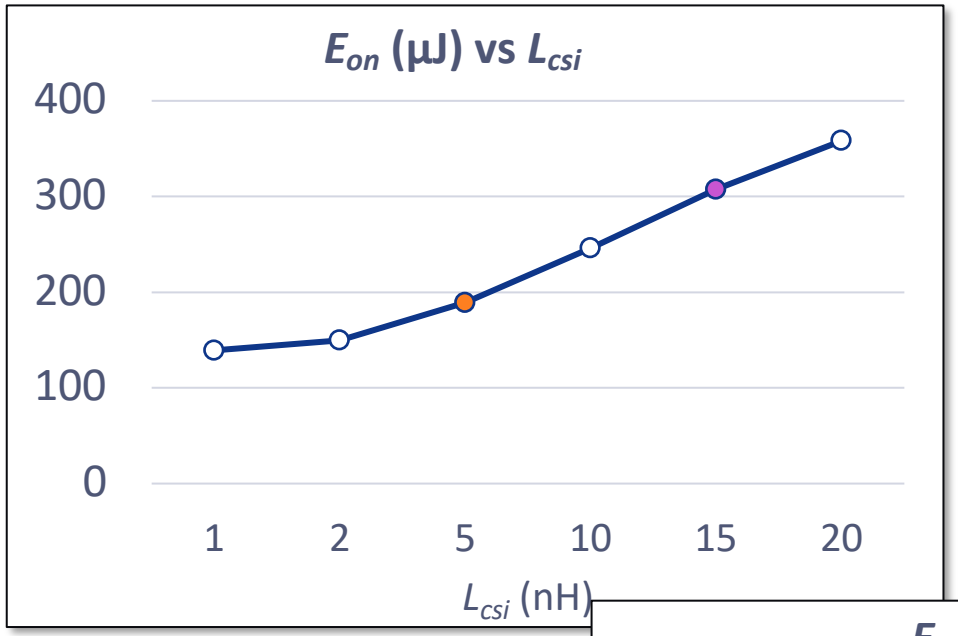


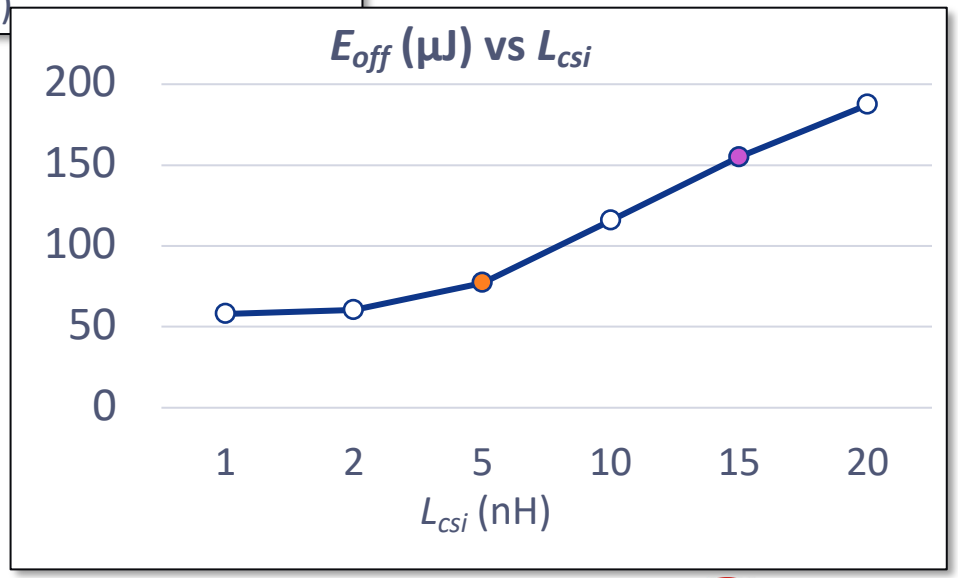
Problem 1 V_G **overshoot** (high L_G, L_S)	Problem 2 **High** L_{csi}
Caused by combination of parasitic inductance and fast switching speeds (di/dt)	Caused by high coupling of the gate-source loop with the power loop
Can lead to inadvertent turn-on and catastrophic shoot-through	Resists fast changes in current and slows down switching speed
Excessive oxide fields can also induce device damage and limit lifetime	Unnecessarily increases switching losses



Common Source Inductance, L_{csi}

Problem 2 **High L_{csi}**
Resists fast changes in current and slows down switching speed
Unnecessarily increases switching losses



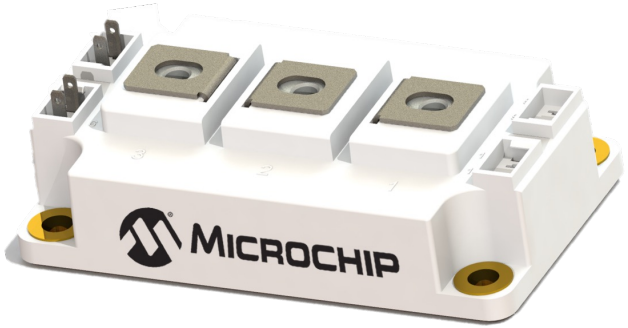


High values of L_{csi} increase switching losses and undercut a key benefit of SiC

	5 nH	20 nH
E_{tot}	266 µJ	545 µJ

Benefits of Low Power Loop Inductance

- What can one achieve by changing the package to reduce power loop inductance?



62 mm

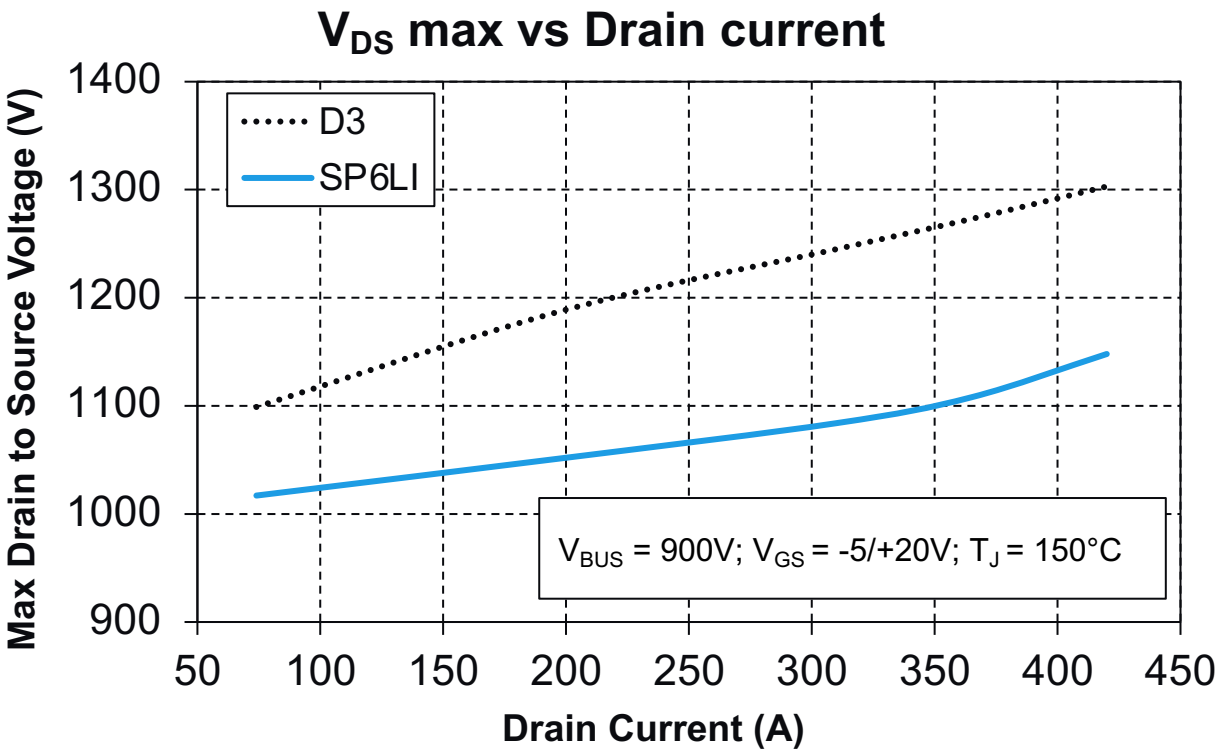
15-20 nH

SP6LI

3 nH

Benefits Over a Lifetime

1. Reduced voltage overshoot

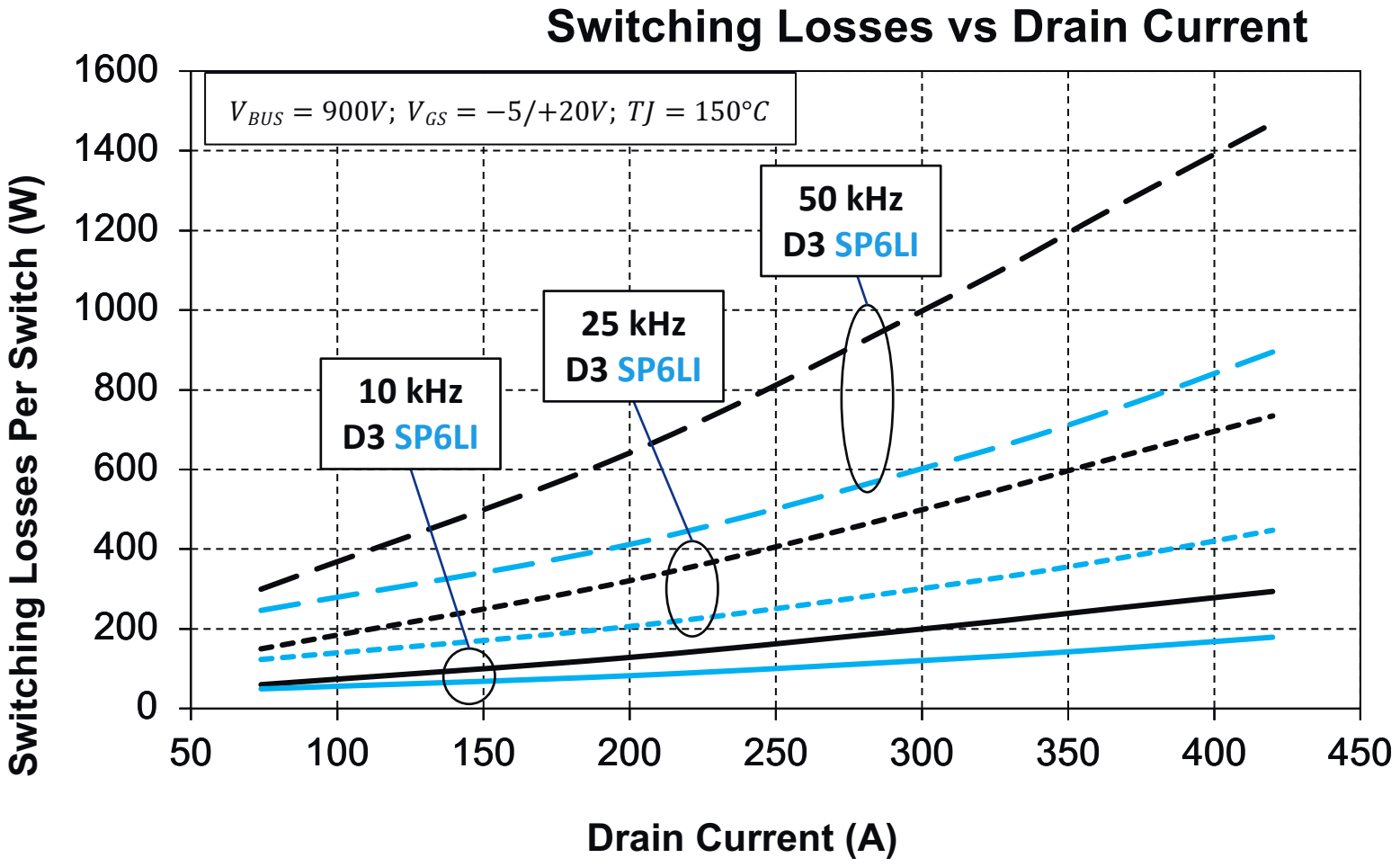


Designers can use lower rated devices and still have margin against overshoot

- Lower device cost
- Greater system efficiency

Benefits Over a Lifetime

2. Greater efficiency across wide working conditions

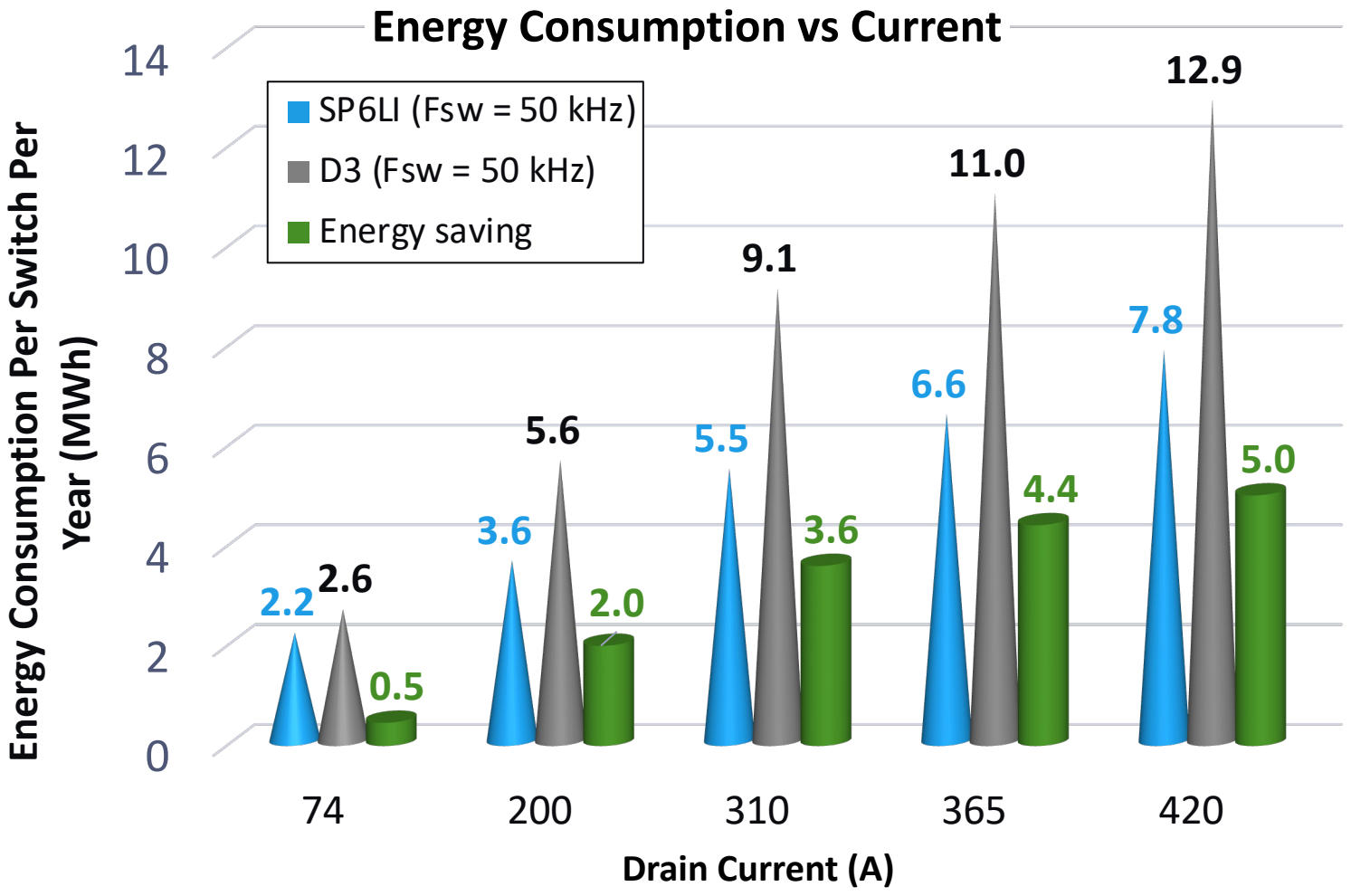


Total switching losses are 20-40% lower

Effects more pronounced at higher switching frequency and drain current

Benefits Over a Lifetime

3. Reduced cost of ownership



Each module used can save the end user more than $2000 per year*

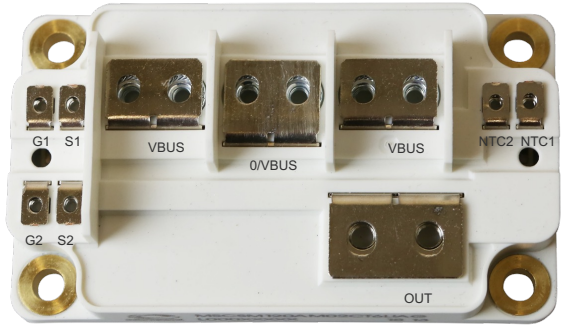
Total switching losses per switch per year at 420A, in units of megawatts

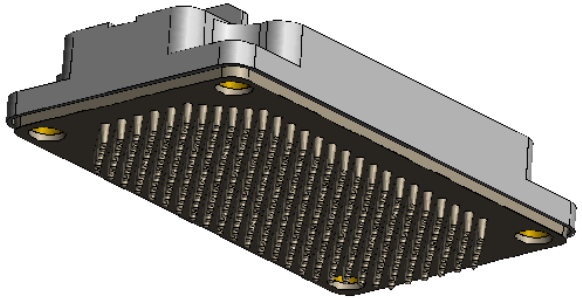
	10 kHz	25 kHz	50 kHz
D3	2.6	6.4	12.9
SP6LI	1.6	3.9	7.8

*Assumes energy cost of 23 cents/kWh, 50 kHz, 420 A

SP6LI: Voltage and Current Options

Part Number	Voltage	Current T_c = 80°C	$R_{DS(on)}$ Typ. T_j = 25°C	$R_{DS(on)}$ Max. T_j = 25°C	SiC parallel diode ratings
MSCSM70AM025CT6LIAG	700V	**538A**	2.5 mΩ	3.2 mΩ	300A
MSCSM120AM02CT6LIAG	1200V	**754A**	2.1 mΩ	2.6 mΩ	300A
MSCSM120AM03CT6LIAG	1200V	**641A**	2.5 mΩ	3.1 mΩ	250A
MSCSM120AM042CT6LIAG	1200V	**394A**	4.2 mΩ	5.2 mΩ	180A
MSCSM170AM029CT6LIAG	1700V	**530A**	2.9 mΩ	3.8 mΩ	300A
MSCSM170AM058CT6LIAG	1700V	**277A**	5.8 mΩ	7.5 mΩ	180A





Pinfin copper baseplate available

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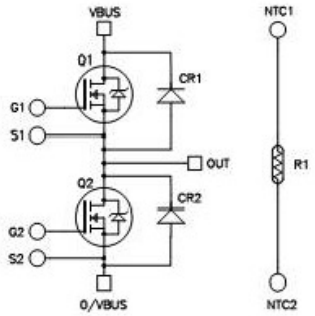
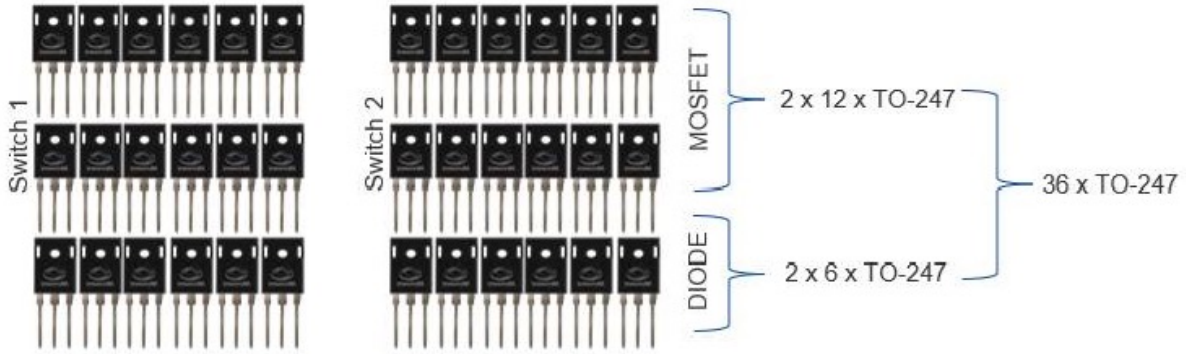
SP6LI vs. TO-247



MSCSM120AM02CT6LIAG

Or…

24 x MSC025SMA120B + 12 x MSC050SDA120B



	SP6LI power module	TO-247 discrete package	Power module benefits
MOSFET Electrical ratings	1200 V – 754 A @ Tc=80°C per switch	1200 V – 73 A @ Tc=100°C (non isolated) each	Higher power density ✓ ✓ ✓
Size	62 mm x 108 mm / 2.44" x 4.25"	36 x (15.87 mm x 21.13 mm / 0.625" x 0.832")	Easier mounting ✓ ✓
Mounting pcb area	6'696 mm2 / 10.37 sq. in.	Min. 13'950 mm2 / 21.62 sq. in. (mounting dependant)	Smaller system size ✓ ✓
Weight	320 g w/ Cu baseplate – 220 g w/ AlSiC	36 x 6.2 g = 223.2 g (no isolation)	More compact design ✓ ✓
Stray inductance	3 nH	20 nH	Higher efficiency ✓ ✓ ✓
Isolation	4 kV AC, 1mn - per design	None, to be added during assemlby	Higher reliability ✓ ✓ ✓
Thermal Management	Very good and repeatable	Complicated	Better thermal performance ✓ ✓ ✓
Temperature sensor	Yes, NTC	No, to be added externally	More accurate protection ✓ ✓ ✓
Assembly time	4 mounting holes + 14 electrical screws	36 mounting holes + 108 solder pins (additional labor)	Faster assembly time ✓ ✓ ✓
Cost (1 k pieces price basis)	$ 926.62 + minimum labor cost	$ 911.88 + high labor cost	Lower system cost ✓ ✓

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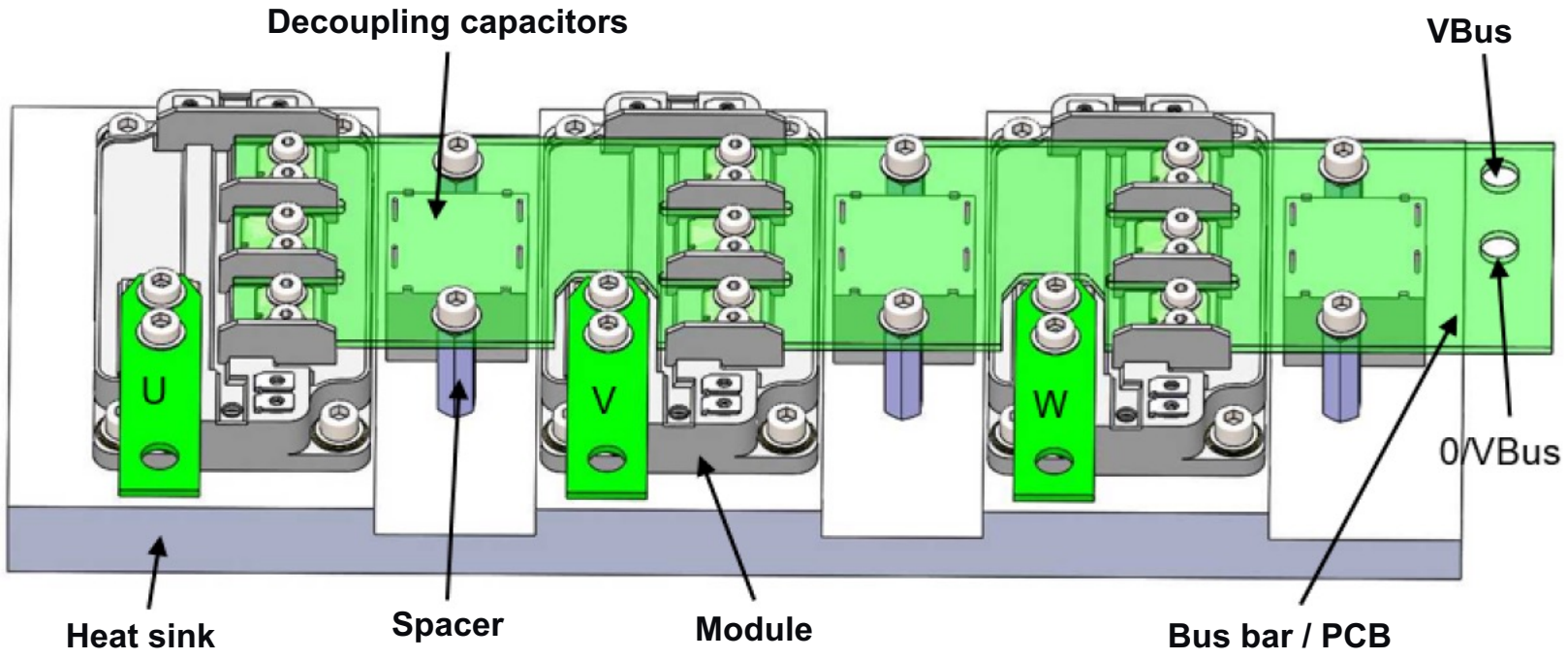
SP6LI: Megawatt-Scale Power

Option 1: Width-wise paralleling

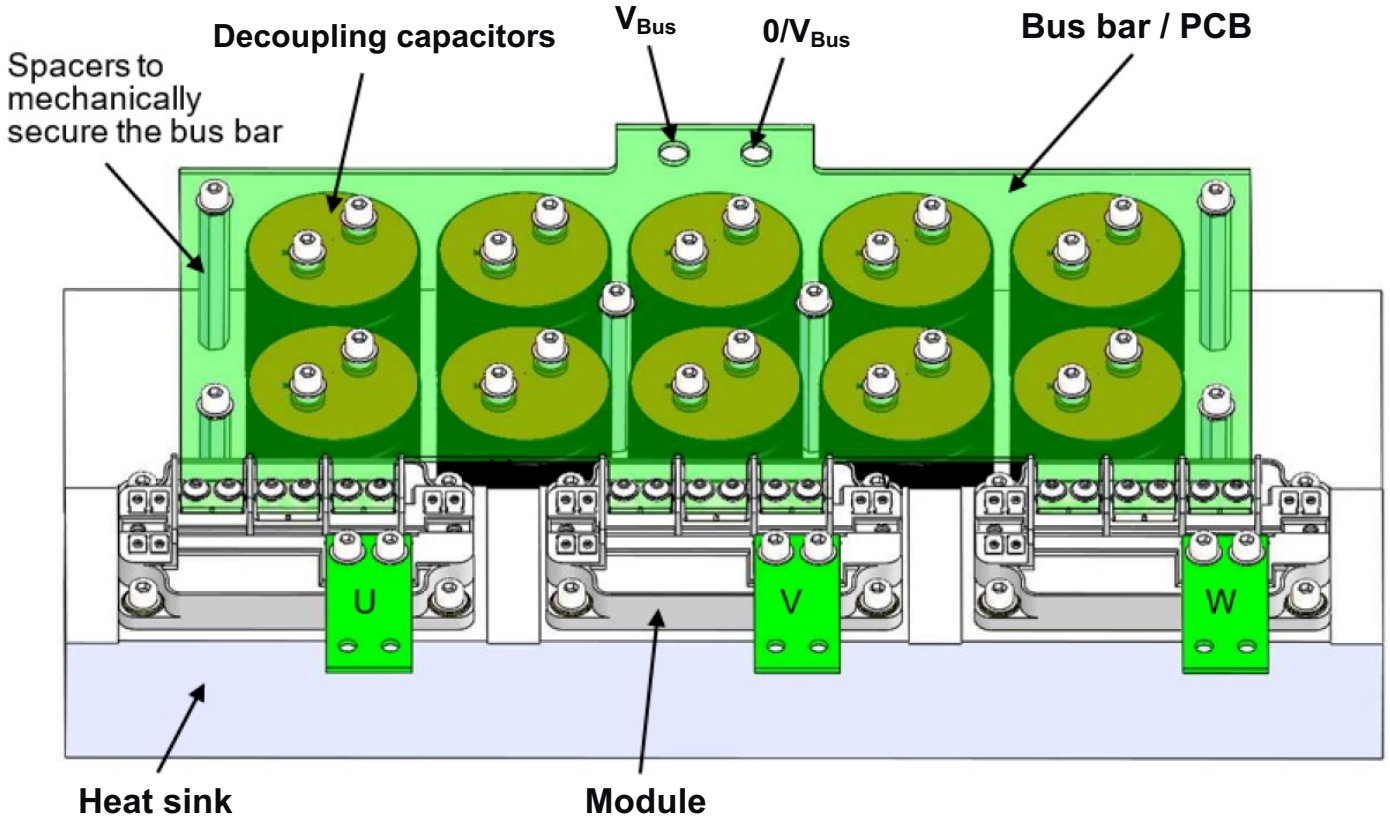
- DC link distributed via bus bars or PCB in a strip line
- Capacitors may be added between power modules



SP6LI: Megawatt-Scale Power

Option 2: Length-wise paralleling

- DC link distributed via bus bars or PCB in a strip line that includes capacitor bank
- Symmetrical DC link distribution, better module decoupling, lowest parasitic inductance



Summary

- Broad Market Acceptance that SiC saves cost at the system level
- To get even more out of SiC, new packaging is required to make systems more efficient, compact, and longer-lasting
- Today we have looked at the impact of parasitic inductance
- Comparing the SP6LI to the common 62 mm package, the end user can save thousands of dollars per module per year
- SP6LI solution is superior to discretes and suitable up to megawatt-scale power levels

Thank you for your attention!

Learn more: microchip.com/SiC