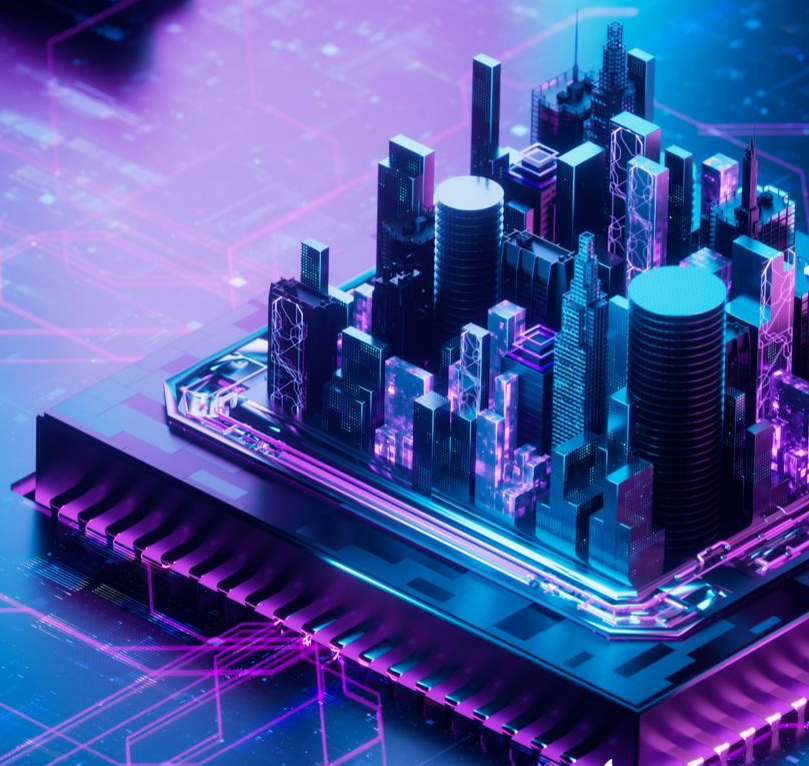
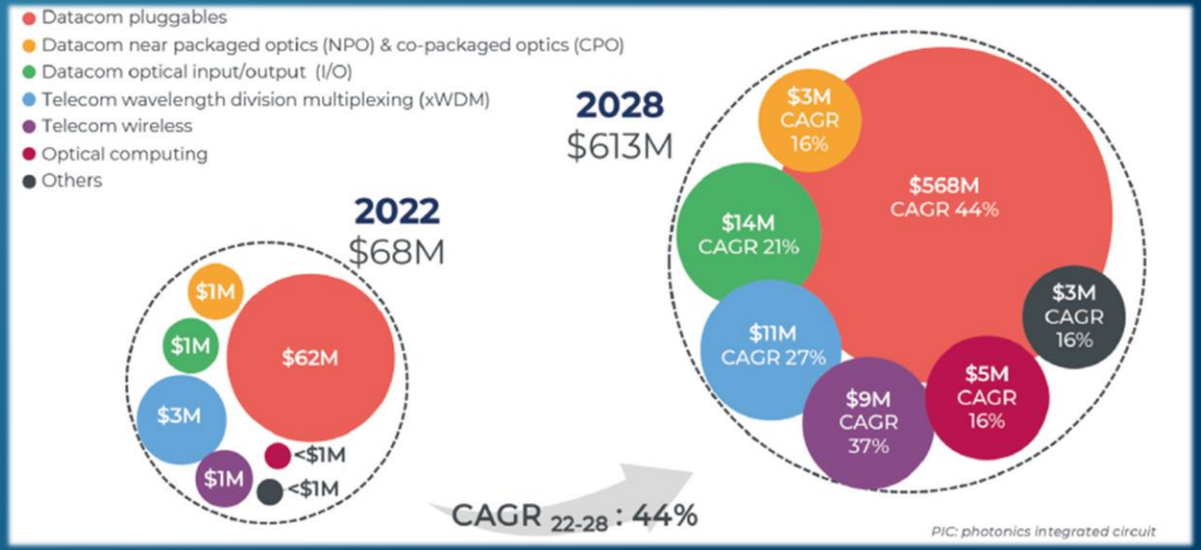
Silicon Photonics For AI/HPC Optical Interconnects

Philippe Absil, Vice President



What is driving the silicon photonics market ?



Yole Développment Report November 2023, PIC dies revenue growth

- Other applications may emerge and drive the technology but …
- …today, Datacom / Telecom drives wafer demand towards 2028
- …tomorrow, AI-driven Datacom I/O & CPO will emerge and drive by 2030-2032

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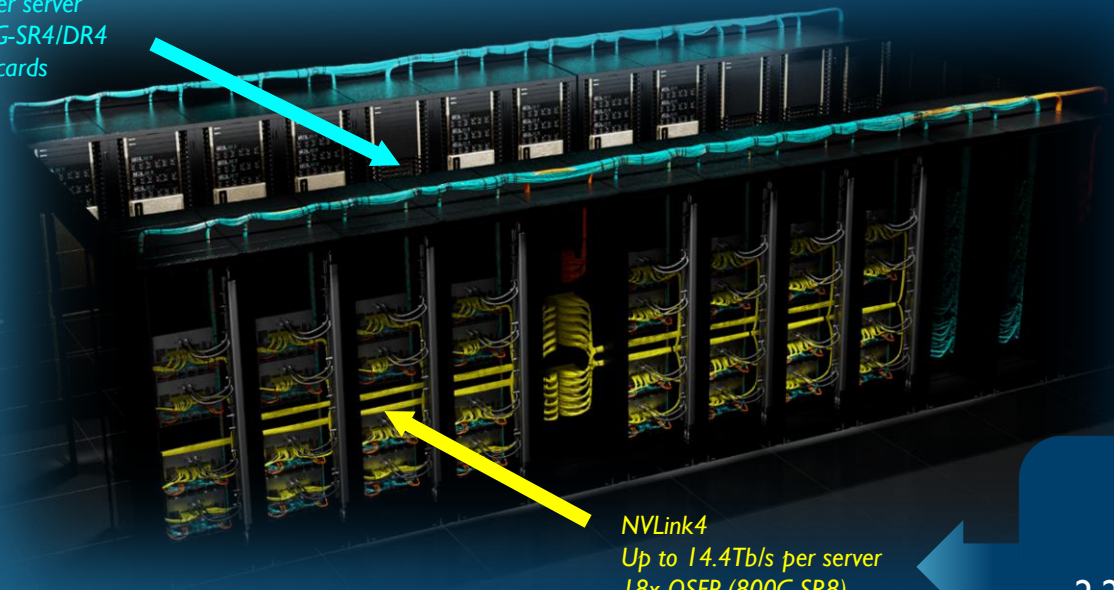
Optical interconnects in AI/ML compute clusters

NDR IB or 400GbE
4Tb/s per server
8x 400G-SR4/DR4
+ DPU cards



NVLink4
Up to 14.4Tb/s per server
18x OSFP (800G-SR8)
256 GPUs

OCP Global Summit 2022 - Nvidia

Anatomy of an H100 AI/ML Cluster

- *1 Exaflp AI perf*
- *>20TB HBM3 memory*
- *70TB/s bi-sectional BW*

[2023] 256 GPU Cluster:
24Tbps HBM bandwidth &
2.2Tbps compute + datacom network bandwidth per GPU

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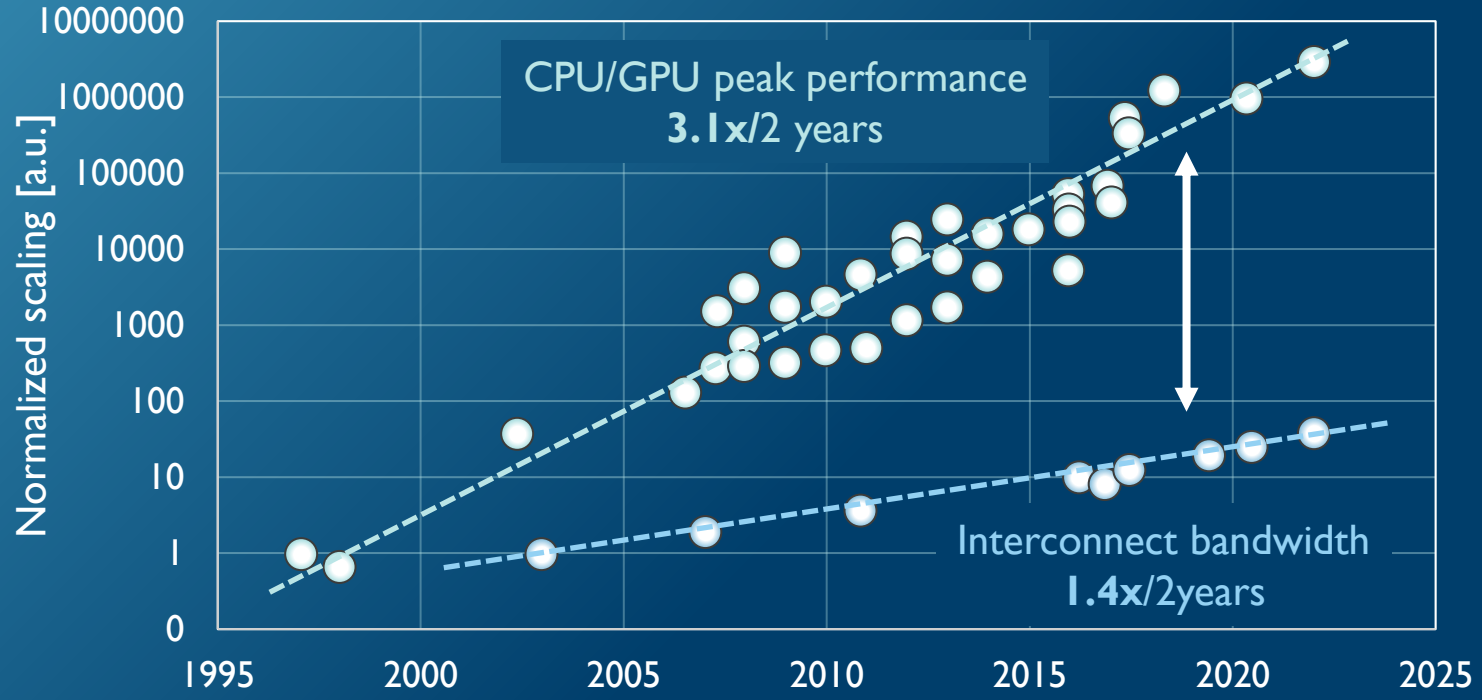
More info: https://developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth/

Interconnect Bandwidth lagging behind **Compute Capability**



Amir Gholami, et. Al. "AI and Memory Wall", https://medium.com/riselab/ai-and-memory-wall-2cb4265cb0b8

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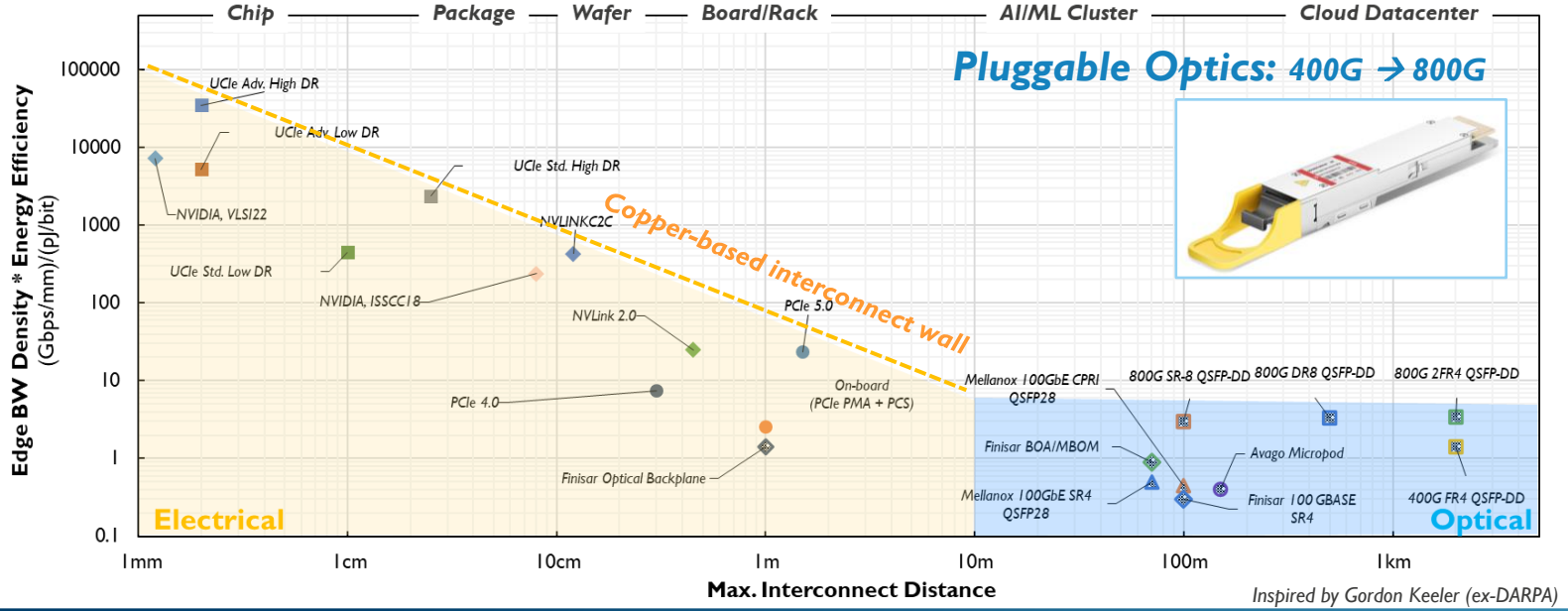
Interconnect Landscape: Copper vs. Optical



Pluggable Optics are the only option for **interconnects beyond 1m,**
but have **2-4x orders worse interconnect performance** than board- or chip-level **Copper**

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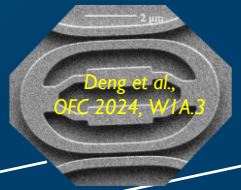
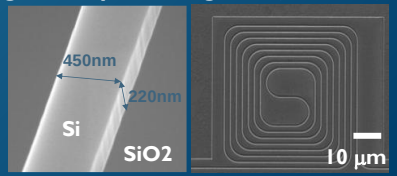
iSiPP: imec's Silicon Photonics Technology up to **200Gbps/lane**

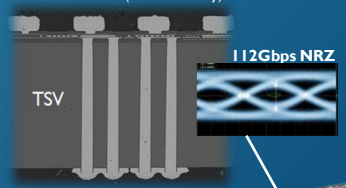
Ultra-Compact Si WDM filters *(193nm immersion) with high thermal tuning efficiency (→1mW / P_π)*



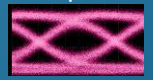
High-density Si Waveguides *(0.5-2dB/cm)*

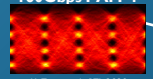


High-Speed TSV *(300mm only)*

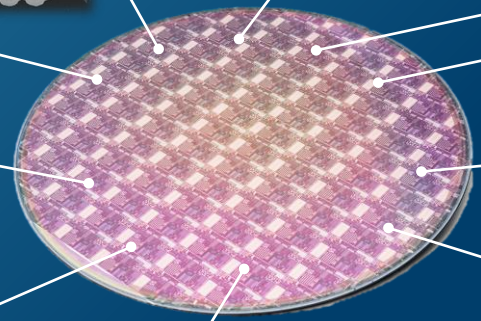


Silicon Ring Modulator

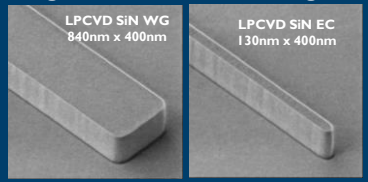




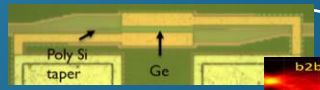
Y. Tong et al., PTL 2020

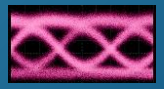


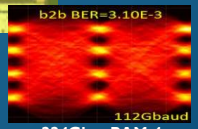
Integrated LPCVD SiN Waveguides



GeSi Electro-Absorption Modulator

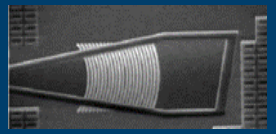






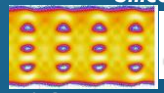
224Gbps PAM-4
D. Chan et al., JLT 2022

SMF Grating Coupler *(<2dB)*



High-NA *(<2dB) &* ***SMF Edge Couplers*** *(~2dB)*

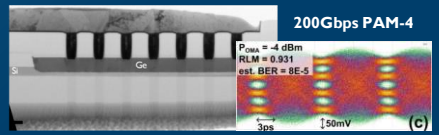
Silicon Mach-Zehnder Modulator



106Gbps PAM-4

56Gbps NRZ

Ge Photodetector



State-of-the-Art Silicon Photonics Platform

enabling next-generation **800G** and **1.6T Pluggable Optics**

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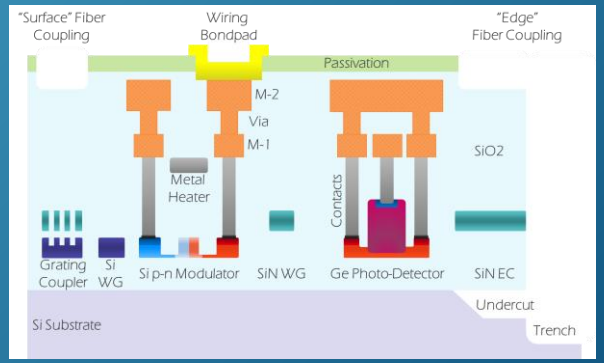
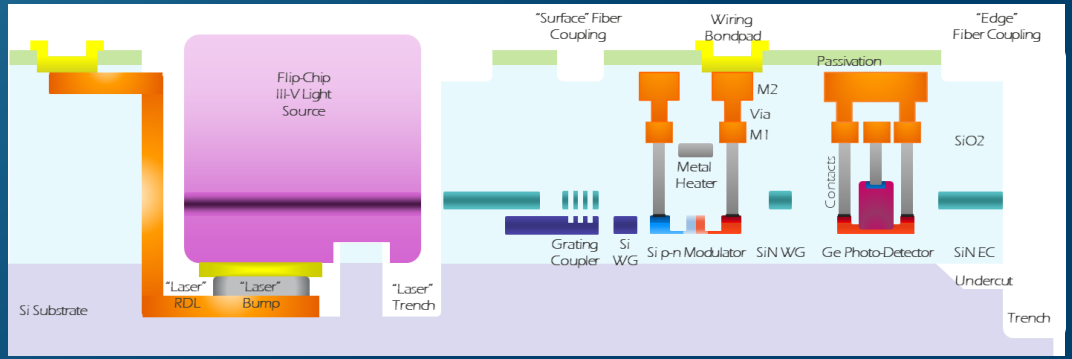
Extending iSiPP: Example #1 - Integrating Light Sources

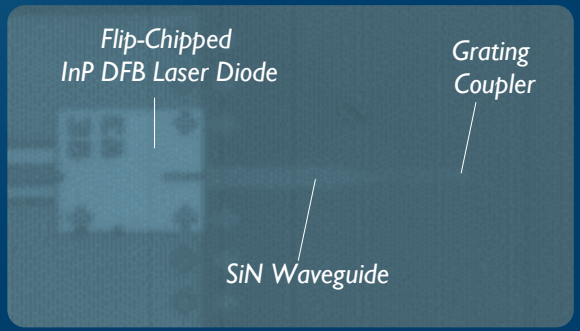
Standard iSiPP



iSiPP with flip-chip bonded III-V laser



Flip-Chip Bonding (FC)
Sequential bonding of III-V Lasers or Amplifiers with <500nm alignment accuracy



Joint Development partners

ASM AMICRA

sivers PHOTONICS

https://ieeexplore.ieee.org/abstract/document/9956863

Adding **High-Power, Flip-Chipped III-V Lasers** to the **Si Photonics toolbox**

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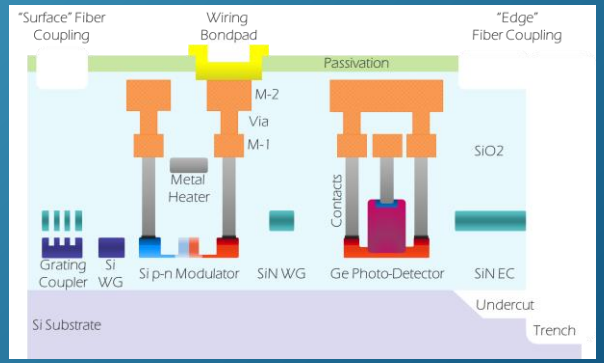
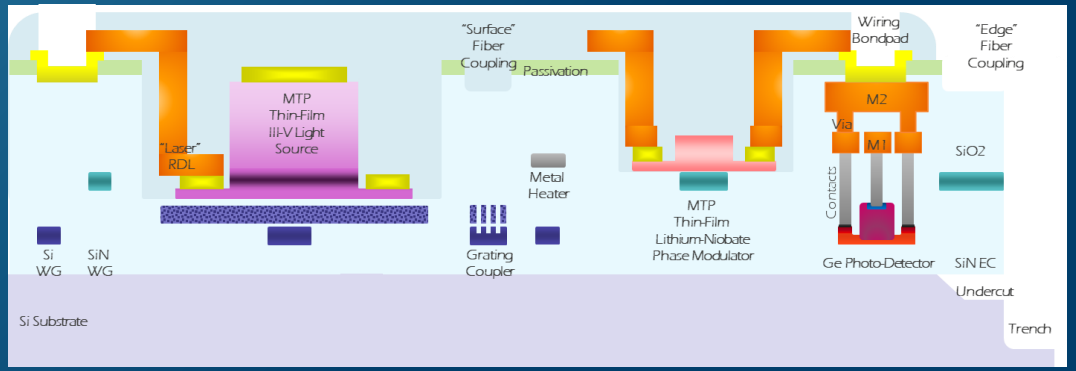
Extending iSiPP: Example #2 – scaling towards **400Gbps/lane**

Standard iSiPP

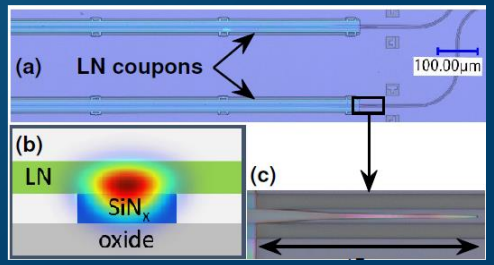


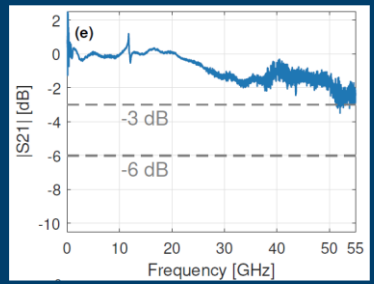
iSiPP with Micro-Transfer Printing



Micro-Transfer Printing (MTP)

Semi-collective bonding of non-Si thin-film devices with <500nm alignment accuracy





T. Vanackere, et al., CLEO 2023

***MTP'ed LNTF** modulators. Early prototype with >55GHz bandwidth*

Adding **100GHz Lithium-Niobate Modulators** to the **Si Photonics toolbox**

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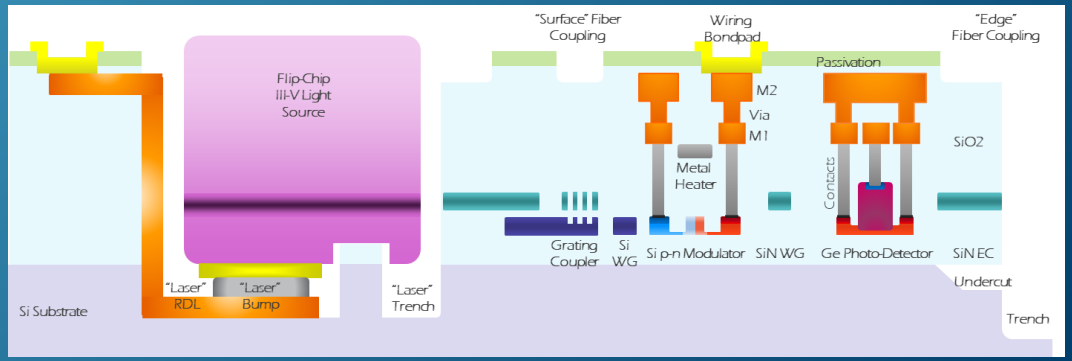
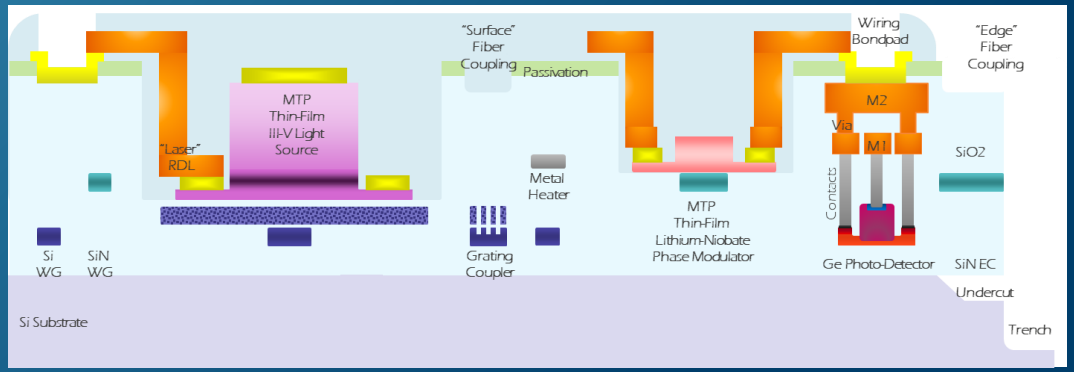
European Consortia Driving Silicon Photonics Hybridization **Supply Chain**



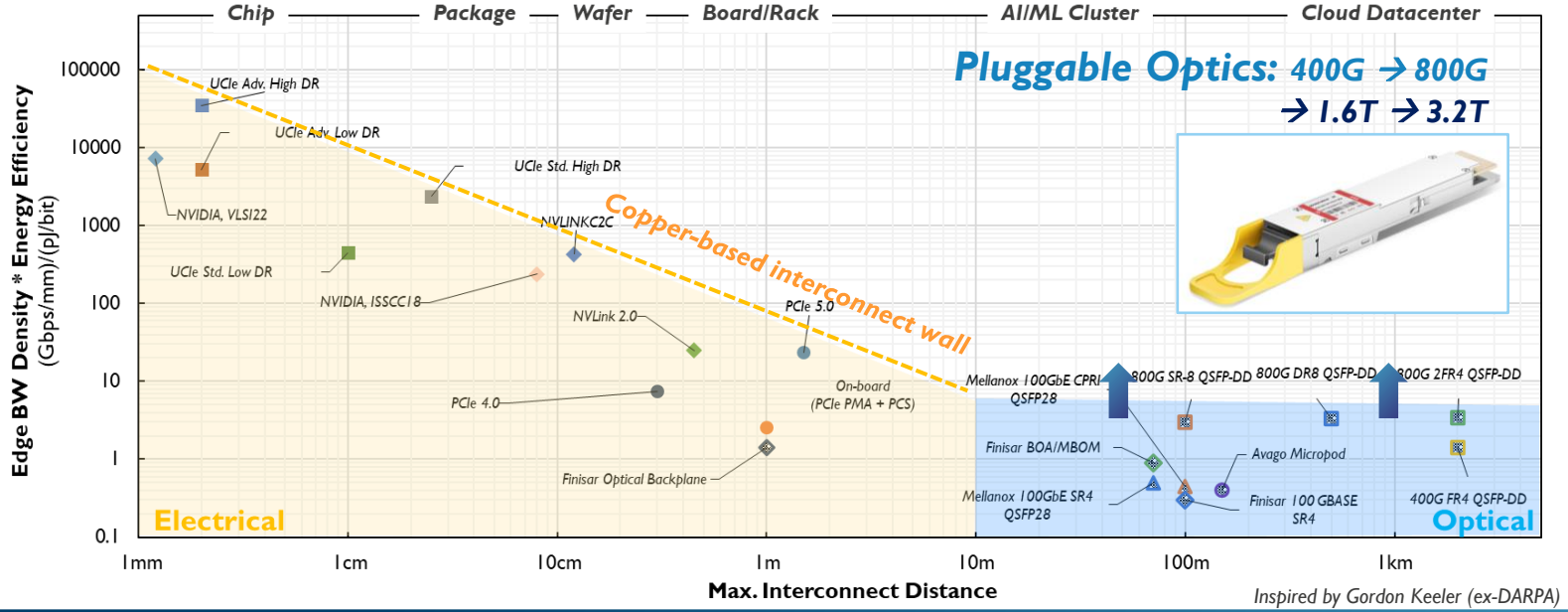


PhotonDelta

photonixFAB

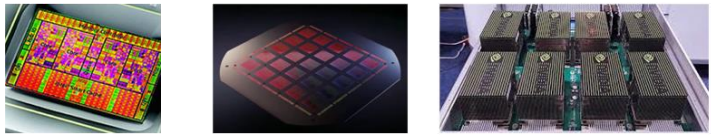
aryballe imec LUMEDA NOKIA xfab

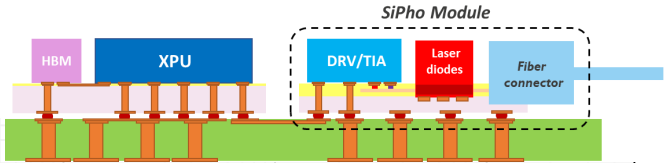
Scaling Pluggable Optics

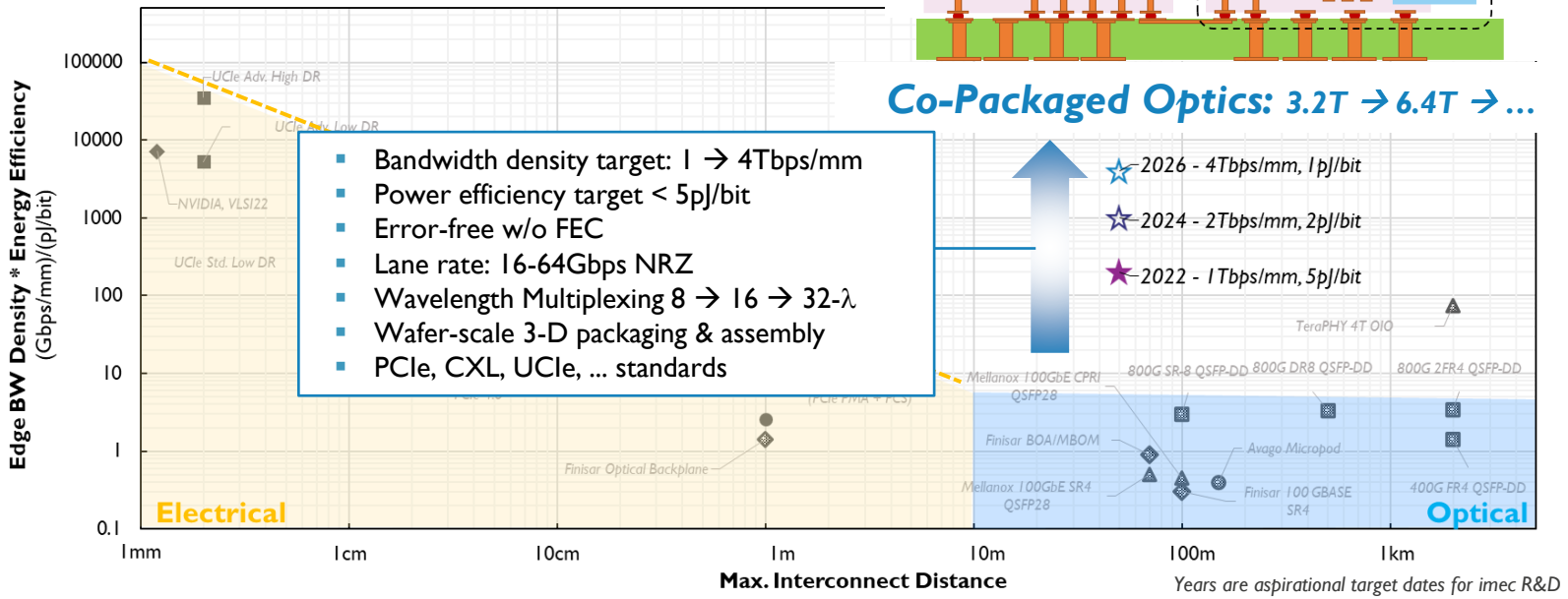


Hybridized SiPho technology will enable **Pluggable Optics** at **1.6T** and **3.2T**

Great, but what's next? Enter **Co-Packaged Optics**

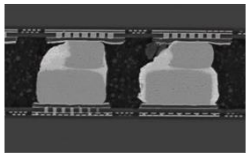
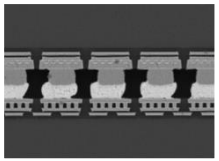
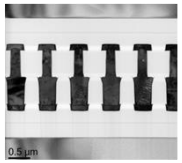


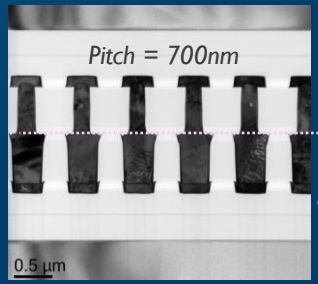




Co-Packaged Optics is needed for **Disruptive Scaling** beyond Pluggable Optics

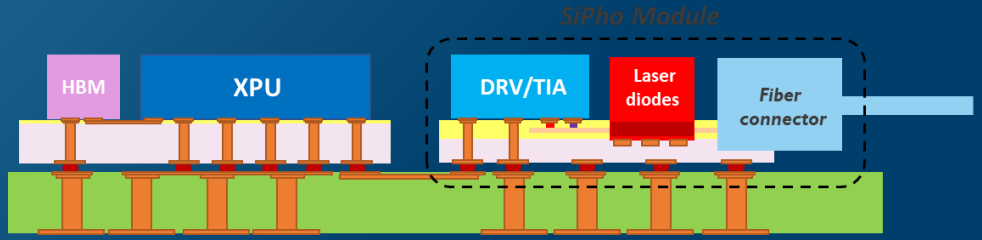
3D-enabled co-packaged optics

	Scaled µbumps (WLUF)	Embedded µbumps	Die-to-Wafer Hybrid Bonding	Wafer-to-Wafer Hybrid bonding
Pitch	50µm → 20µm	40µm → 5µm (3µm)	20µm → 3µm (2µm)	3µm → 0.5µm (0.4µm)
Die-to-die gap	12µm	4µm	~0µm	~0µm
Cross-section				
Interface parasitic Capacitance	~60fF → ~15fF	~40fF → ~2fF	~10fF → ~1fF	~2fF → <1fF



Top Wafer/Die (EIC)

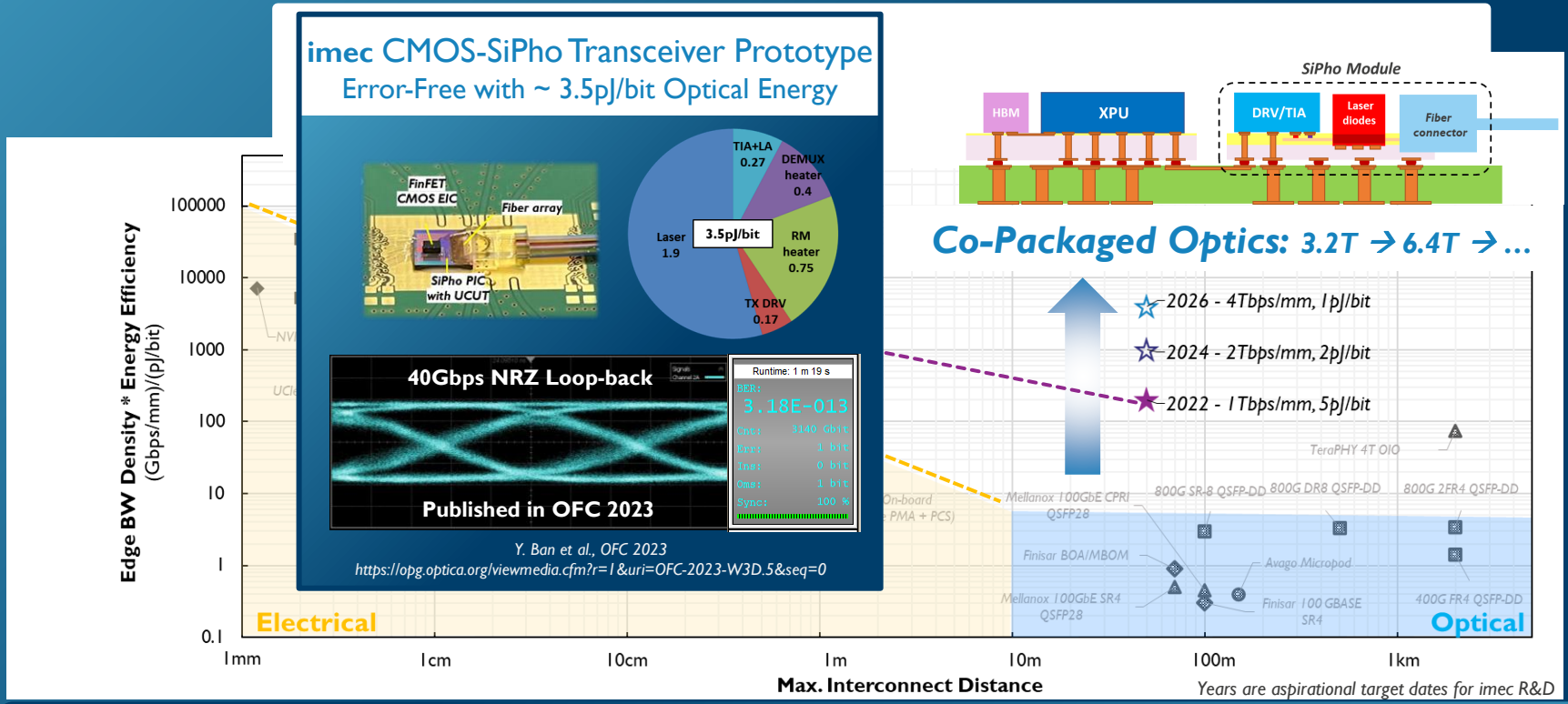
Bottom Wafer/Die (PIC)



3D/TSV enabled Co-Packaged Optics

Energy efficiency scaling with 3D bonding technology scaling with low capacitance

Co-Packaged Optics for **ultra-low Power** and **Latency**

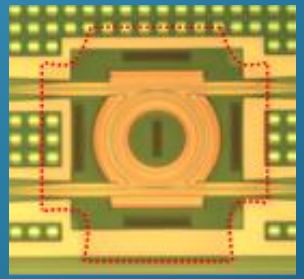


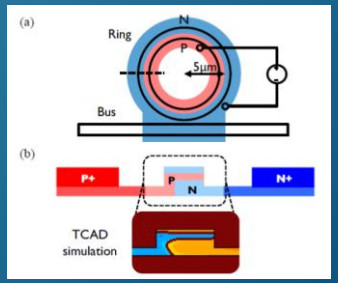
Co-Packaged Optics is needed for **Disruptive Scaling** beyond Pluggable Optics

What **Modulator** For CPO & Interposer ?

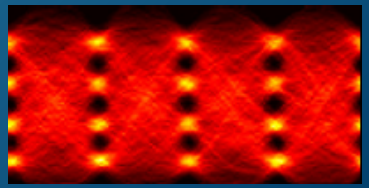
Established Si-based Options

Micro Ring/Disk Modulator



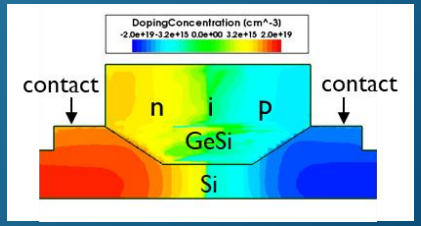


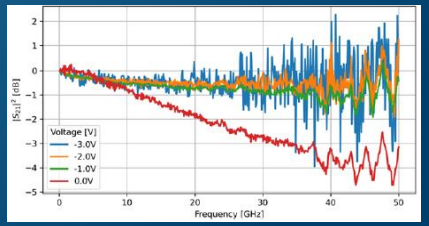
160Gbps



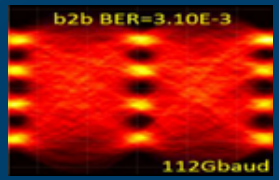
Y. Tong et al., PTL 2020

Ge/Si Electro-Absorption Modulator





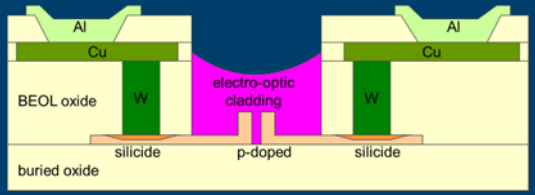
224Gbps



D. Chan et al., JLT 2022

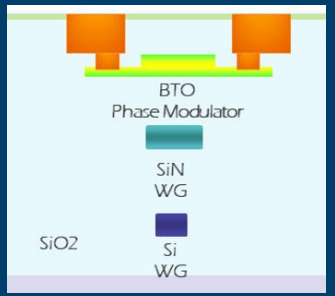
Alternative Materials Options

Silicon-Organic



Courtesy W. Bogaerts

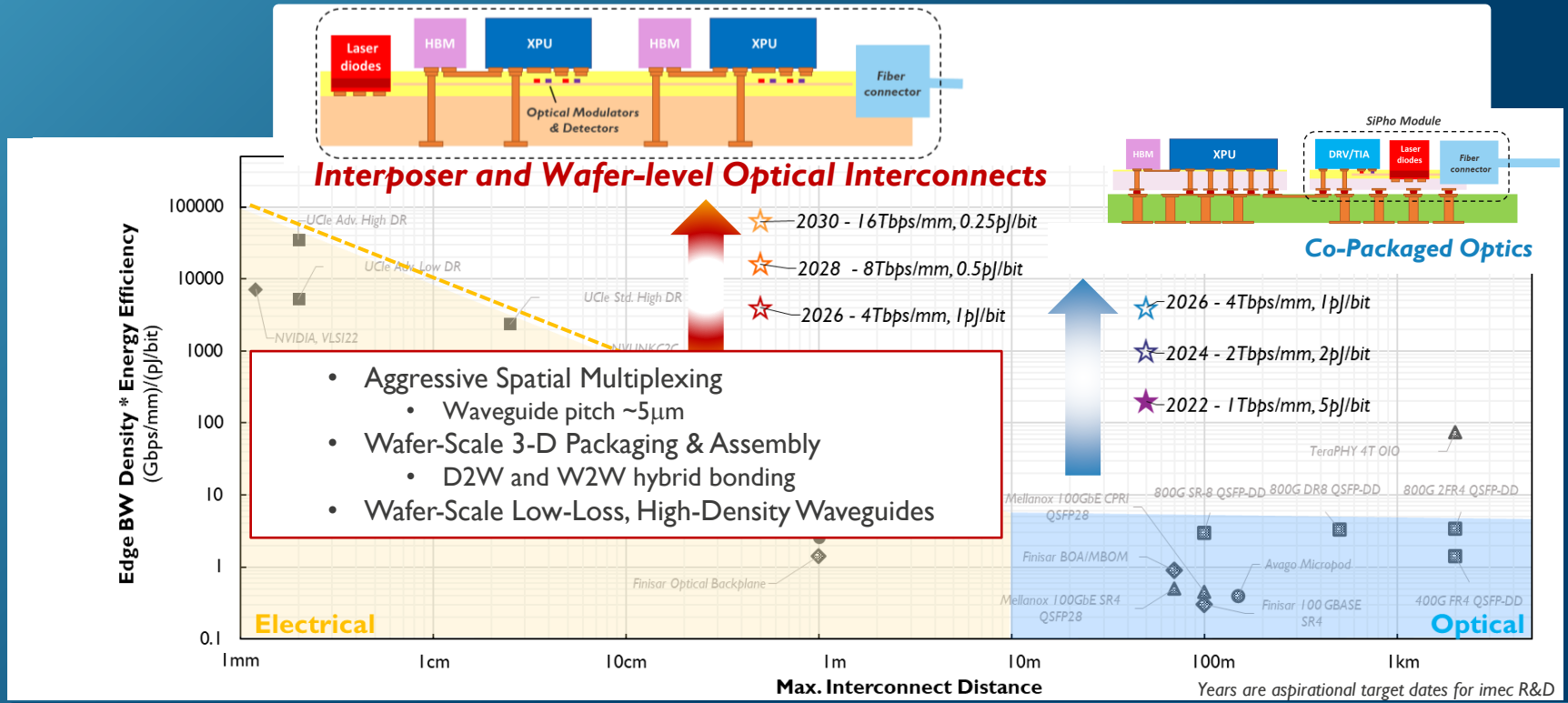
Pockels



Courtesy F. Ferraro

imec

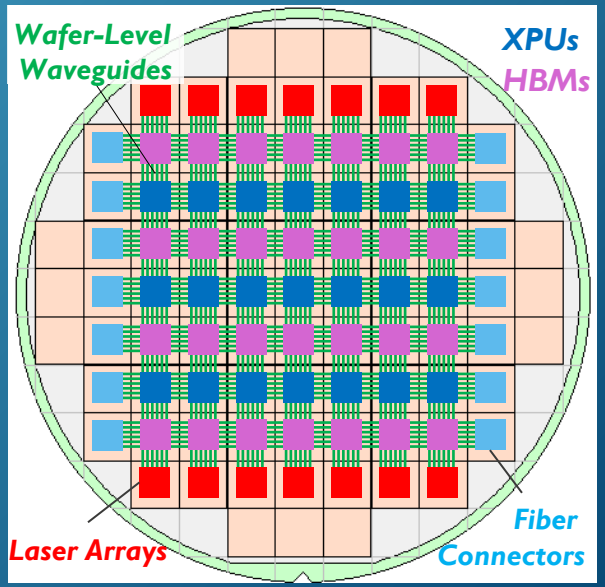
Optical Interconnects on the **Interposer** and **Wafer**

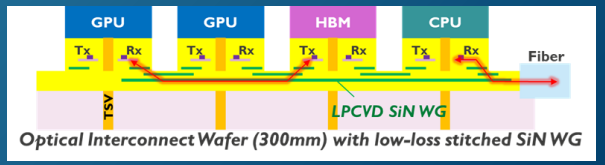


Optical Interposers for **Chip-to-chip** and **Off-Package Interconnects**
with the performance of **short-reach Copper,** at **100x Reach**

Vision: **Towards Optically Interconnected Systems-on-Wafer**

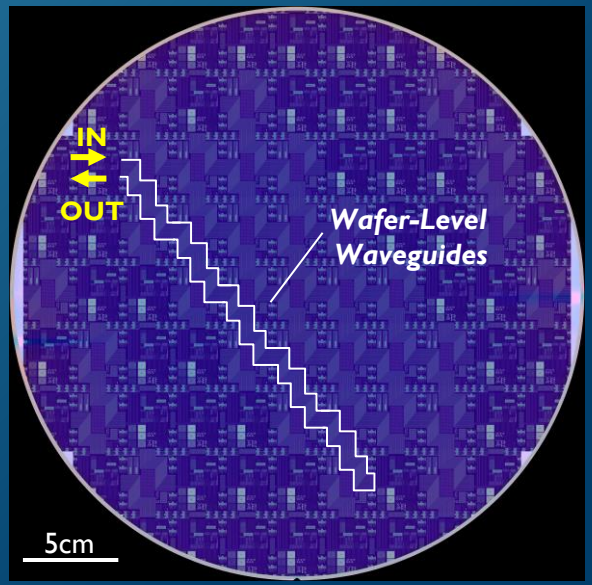
Optically Interconnected System-on-Wafer



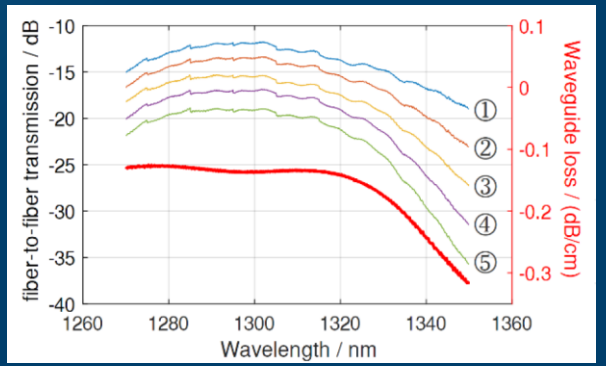


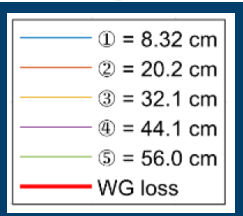
Optical Interconnect Wafer (300mm) with low-loss stitched SiN WG

First 300mm wafer-level reticle-stitched interconnect waveguides (imec)



Measured Wafer-level Loop-back SiN Waveguides





300-mm wafer-level waveguides up to **56cm long,** with **low all-in propagation loss (0.15dB/cm)**

Xu et al., OFC 2024, M4A.3

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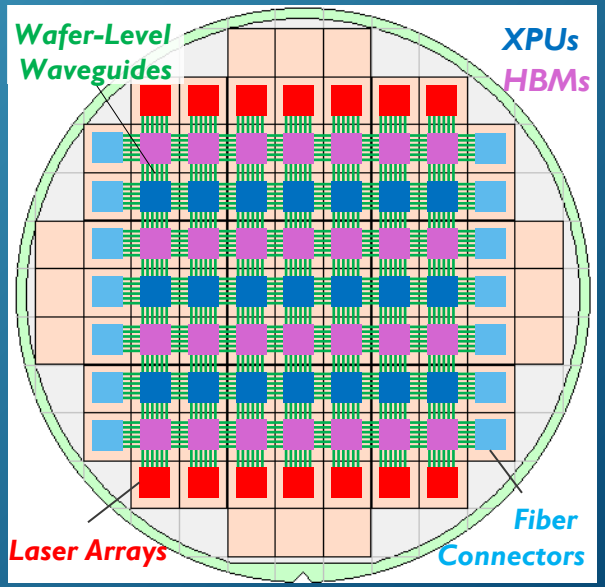
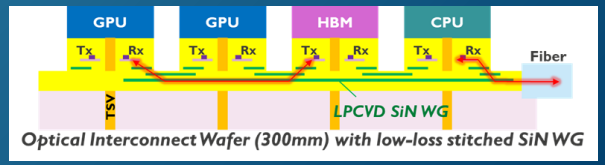
Vision: **Towards Optically Interconnected Systems-on-Wafer**

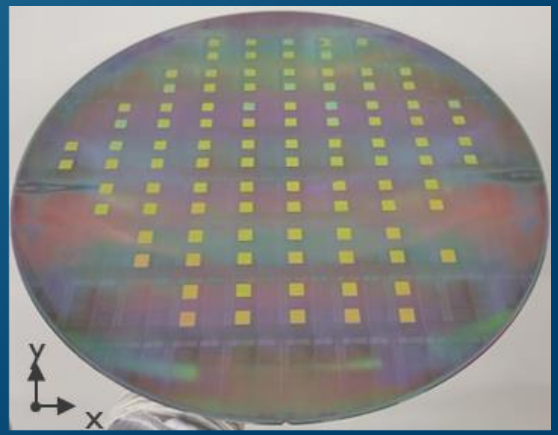
Optically Interconnected System-on-Wafer



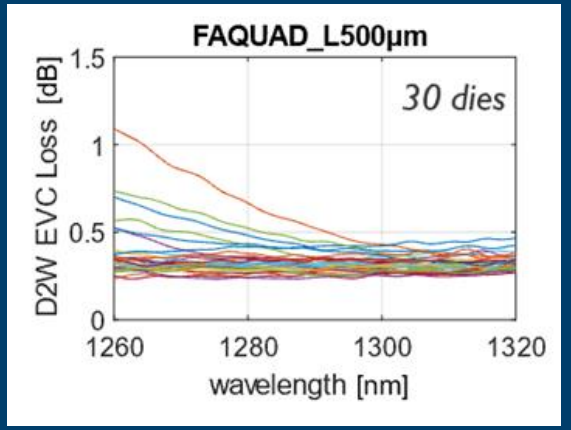


Optical Interconnect Wafer (300mm) with low-loss stitched SiN WG

300mm wafer populated with Collective Die-To-Wafer Cu-Dielectric Hybrid Bonding With Electrical & Optical Interfaces



Measured Wafer-level Distribution of Die-To-wafer Transition Loss



Die-to-Wafer Transition Loss <0.5dB

Xu et al., OFC 2024, Tu3A.3

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Takeaways

- AI/ML and HPC Systems are driving aggressive growth in optical networking
- State-of-the-Art Silicon Photonics enables 800G and first-gen 1.6T pluggable optics
  - Upcoming Hybridized Silicon Photonics platforms will enable pluggable modules up to 3.2T
- Co-Packaged Optics aims at a further 100x scaling of optical interconnect performance
  - Highly efficient and compact modulators will be required
- Optical Interconnects are likely to replace long-range Cu interconnects at the Interposer and Wafer level, Leveraging 3D-enabled Silicon Photonics


Thank You
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40 YEARS
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