CENTER OF EXPERTISE

ADVANCED X-RAY TOPOGRAPHY

SPEEDING UP XRT DEFECT RECOGNITION FOR SIC

FROM TSD DETECTION TO FASTBPD

C. Kranert[1], C. Reimann[1], S. Kobayashi[2], Y. Ueji[2], K. Shimamoto[2], K. Omote[2]

[1]Fraunhofer IISB, Erlangen, Germany

[2]Rigaku Corp, Tokyo, Japan

Rigaku

Fraunhofer
IISB

Center of Expertise for X-Ray-Topography

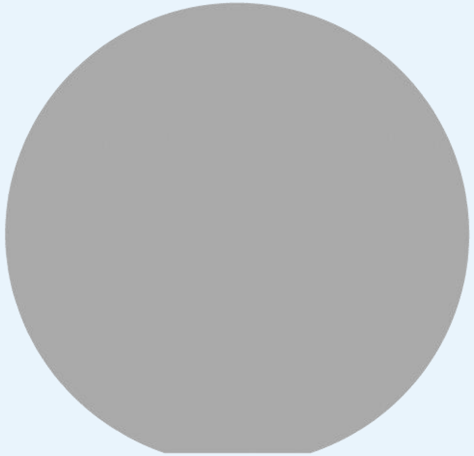
- founded in 2021
- joint undertaking of Rigaku Corporation and Fraunhofer IISB to develop:
  - X-ray topography tools
  - measurement procedures
  - defect recognition and counting algorithms

for production, quality assurance and R&D application

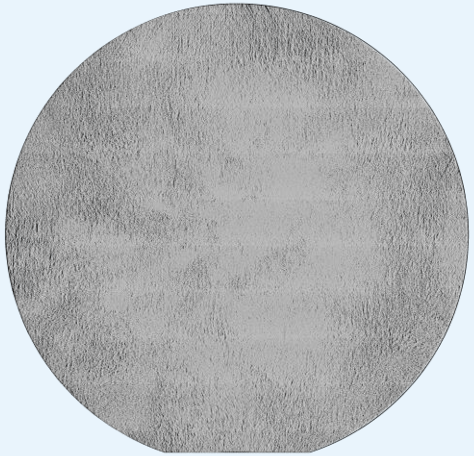
Taking away the power from silicon…

- … means leaving behind dislocation-free material!
- Dislocations can have an impact on device yield and reliability
- Every substrate is different

Silicon



Silicon carbide



Industry requires reliable, high-throughput, non-destructive substrate characterization

Defects in silicon carbide

Threading Screw Dislocations (TSD)

- Increase leakage current of diodes
- Detrimental to gate oxide lifetime
- Can result in growth pits causing problems during device processing

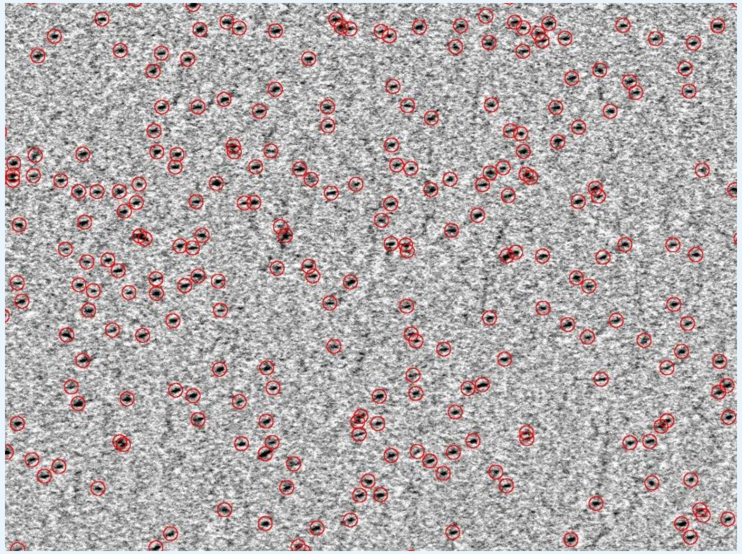
Basal Plane Dislocations (BPD)

- Result in stacking faults under stress
- Reduce lifetime of
  - MOSFETs
  - Bipolar devices

TSD Detection

TSD detection

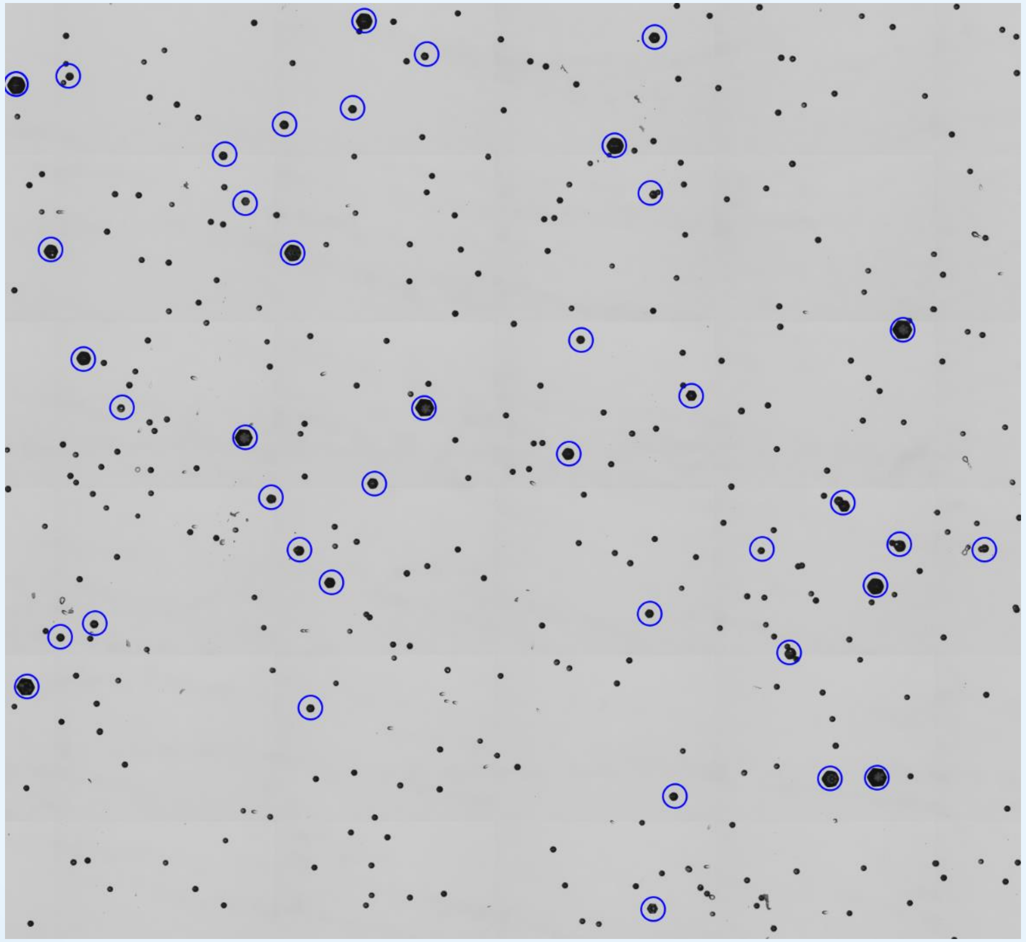
- TSD detection using chemical etching highly challenging
  - TED and TSD cannot be distinguished for standard KOH etching
  - Other alternative approaches come with different problems
- Use of (0008) reflex
  - TSD/TMD appear as small, dark spots
  - Almost no other features visible (on today‘s production grade SiC)
  - Simple to classify and count → enables reliable and robust dislocation counting



TSD detection

Accuracy

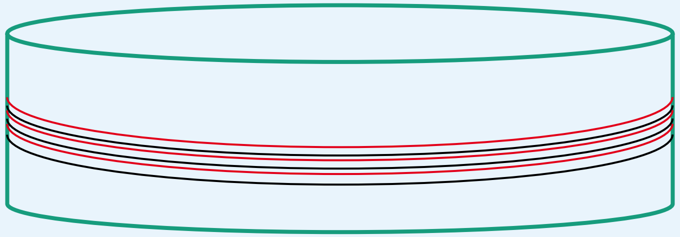
- Verification of TSD detection against other established methods
  - KOH etching after epitaxy
  - **KOH+Na$_2$O$_2$ etching**
  - C-face etching
  - Synchrotron XRT
  - Pit features after epitaxy

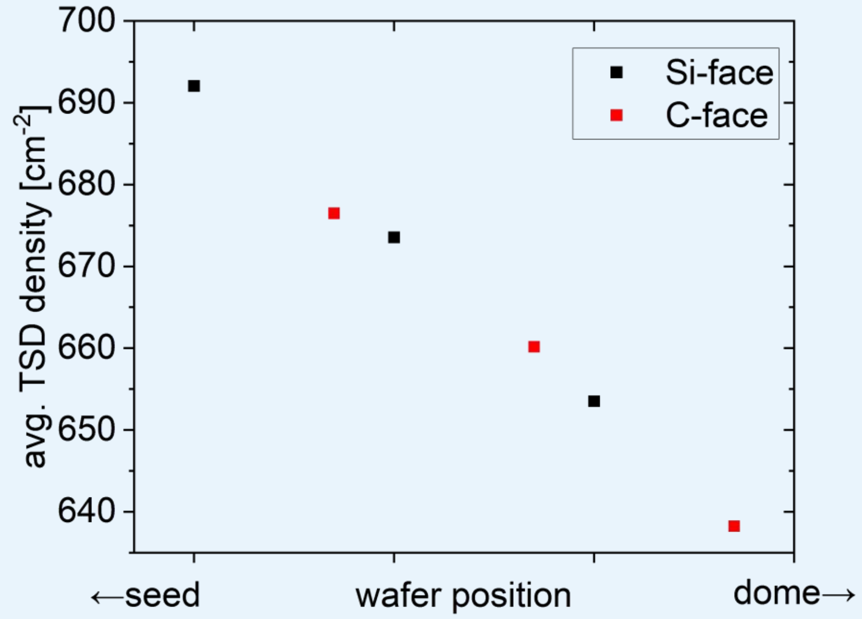


TSD detection

Reproducibility

- Measurement of three neighboring wafers on both sides
(Si-face and C-face)
- Differences between individual wafers can be resolved
- Differences between front and back side of wafer can be resolved
- From trend between data points, the distance between wafers can be estimated!

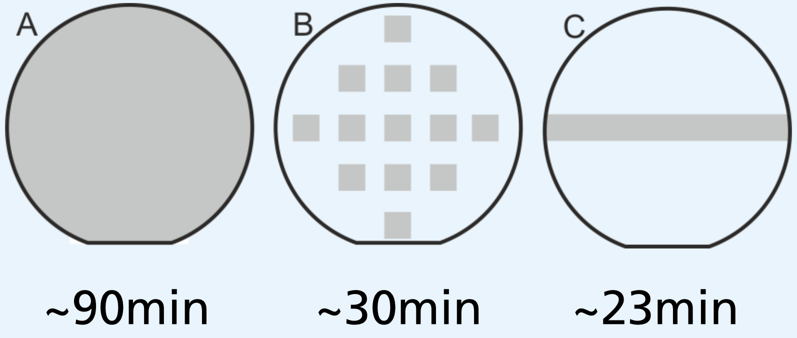


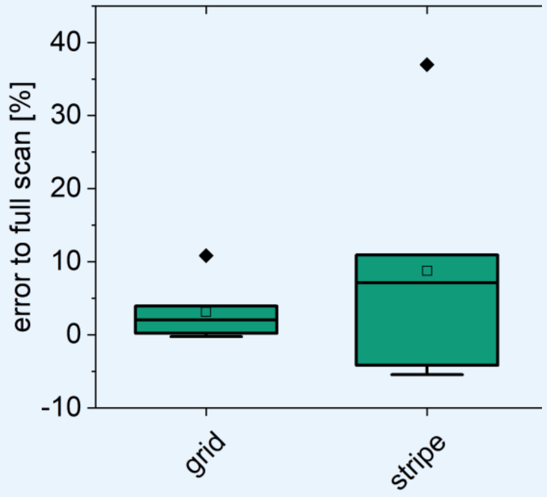


TSD detection

Measurement times

- Industrial application:
  - Perfect accuracy usually not required
  - **High throughput essential**
- TSD detection requires minimum image quality → Throughput on full wafer scale is limited
- Use of local measurement to increase throughput
  - Grid measurement (B) → only very small error at 3x throughput
  - Stripe measurement (C) → critically increased error at 4x throughput





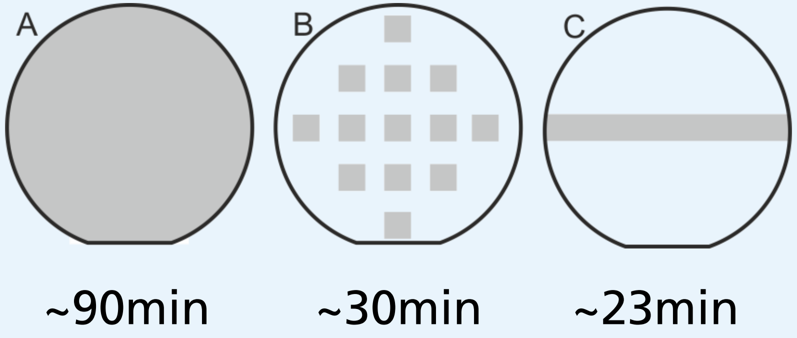
TSD detection

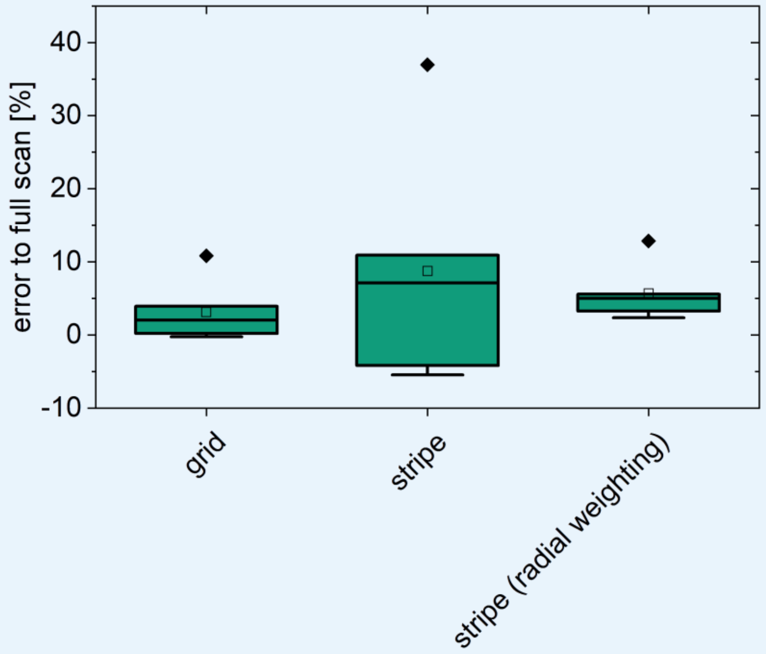
Measurement times

- Large error for strip measurement results from different contributions from center and edge parts
- Use of radially weighted average:

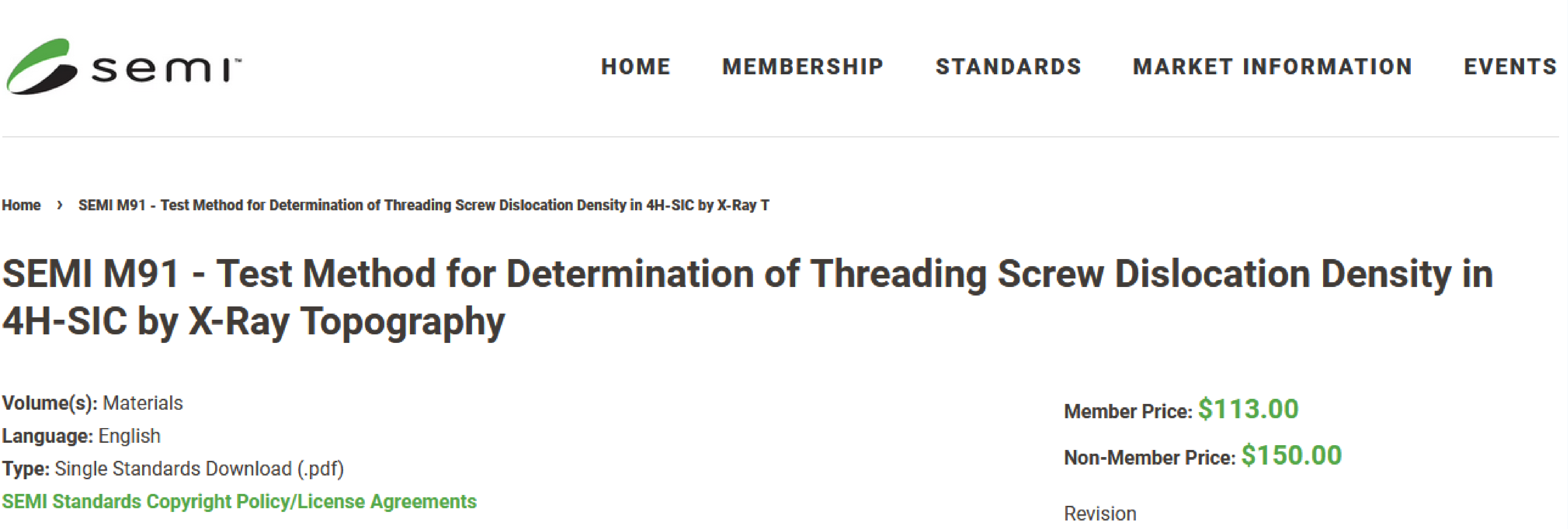
$$\rho_{TSD} = \frac{\sum r_i \rho_i}{\sum r_i}$$

- Strongly reduced error with much narrower distribution





TSD detection
SEMI Standard



SEMI M91 - Test Method for Determination of Threading Screw Dislocation Density in 4H-SIC by X-Ray Topography

Volume(s): Materials
Language: English
Type: Single Standards Download (.pdf)
SEMI Standards Copyright Policy/License Agreements

Member Price: $113.00
Non-Member Price: $150.00
Revision

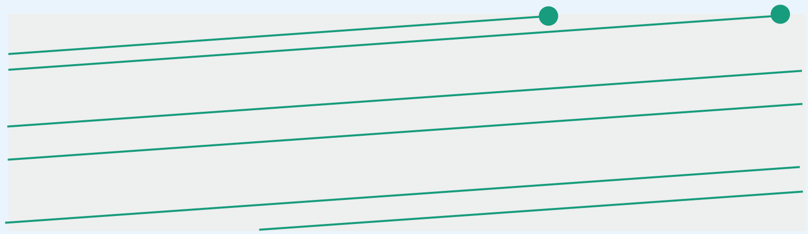
BPD Quantification

BPD quantification

Principle

- BPDs give only weak contrast in reflection geometry due to in-plane Burgers vector → usually measured by XRT in transmission geometry
- Which properties to investigate?
  - BPD count?
  - BPD length?
- Volumetric density (cm/cm^3) differs strongly (factor of 14 at 4° offcut) from etch pit density (cm^{-2})

XRT measurement must reproduce EPD values from KOH etching!

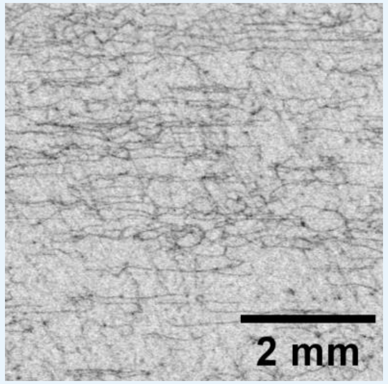


BPD quantification

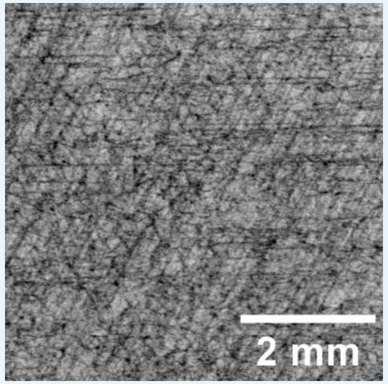
Principle

- Linear appearance of BPD pose challenges to counting
  - Detection of start and end of dislocation already challenging for low densities
  - At higher densities → strong overlapping hinders differentiation between dislocations
  - Discrete counting (as for BPD) not possible

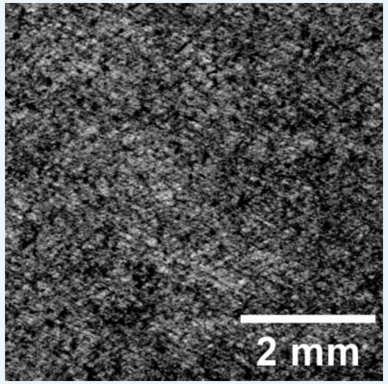
low density



medium density



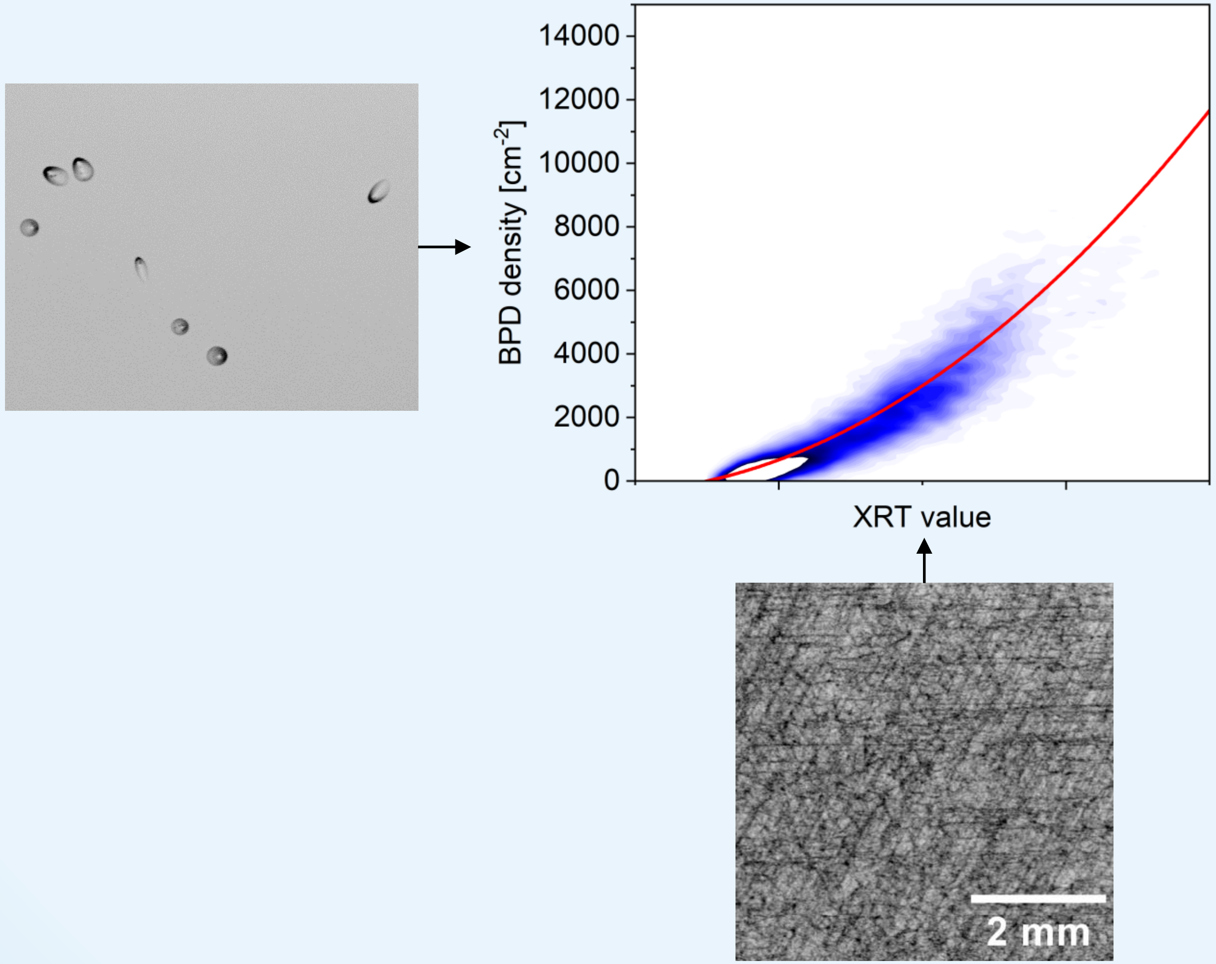
high density



BPD quantification

Principle

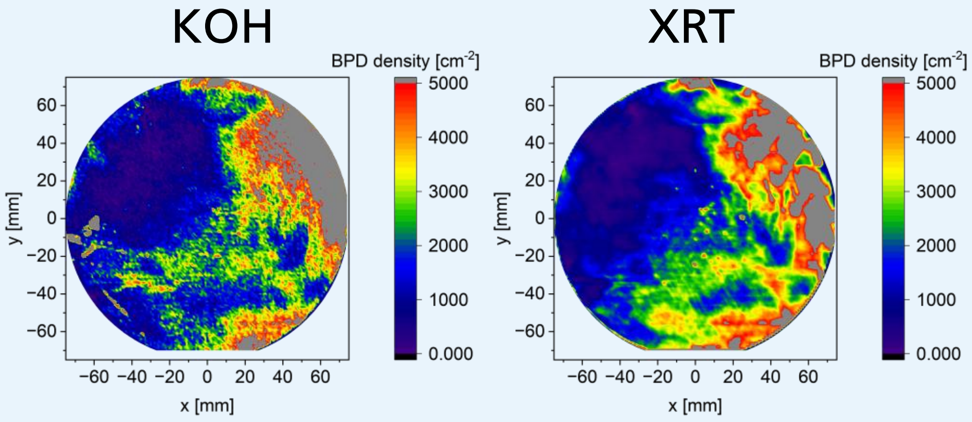
- Use of a calibrated approach to obtain results consistent to KOH results
  - Divide topogram into tiles (typically 1x1mm²)
  - Analyze topogram to obtain a numeric value
  - Etch wafer by KOH and obtain etch pit density for the same tiles
  - Calibration curve obtained by correlating both data sets



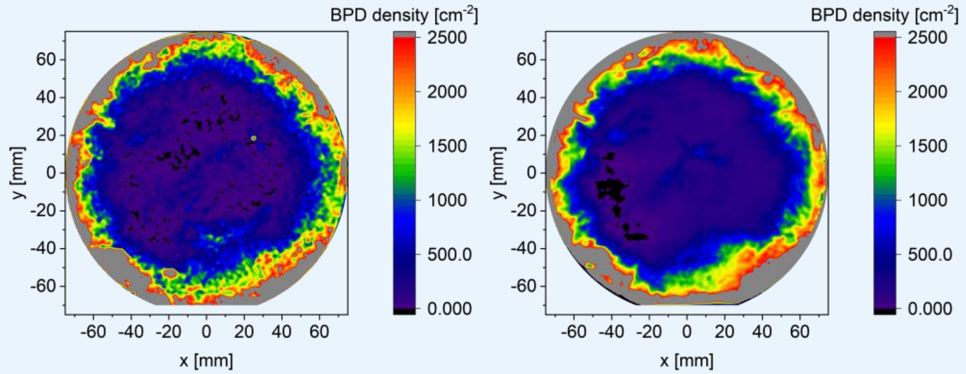
BPD quantification

Verification

- Calibration tests using wafers from 5+ leading manufacturers
- Very good agreement with the same set of calibration data for all manufacturers
  - Independent of material properties (except thickness and offcut angle)
  - Recalibration / system check can be done based on XRT measurements, i.e., without additional KOH etching



Kranert et al., poster presentation @ECSCRM 2021



Kranert et al., poster presentation @ICSCRM 2022

BPD quantification

Advantages and disadvantages of regular XRT

Advantages

- Non-destructive
- Possible to exchange wafers to check inter-lab accuracy
- Not affected by things like stains/residues which may occur when etching
- Insensitive to overlapping (depending on evaluation algorithm)
- Easier to keep stable and to validate than the properties of a KOH melt

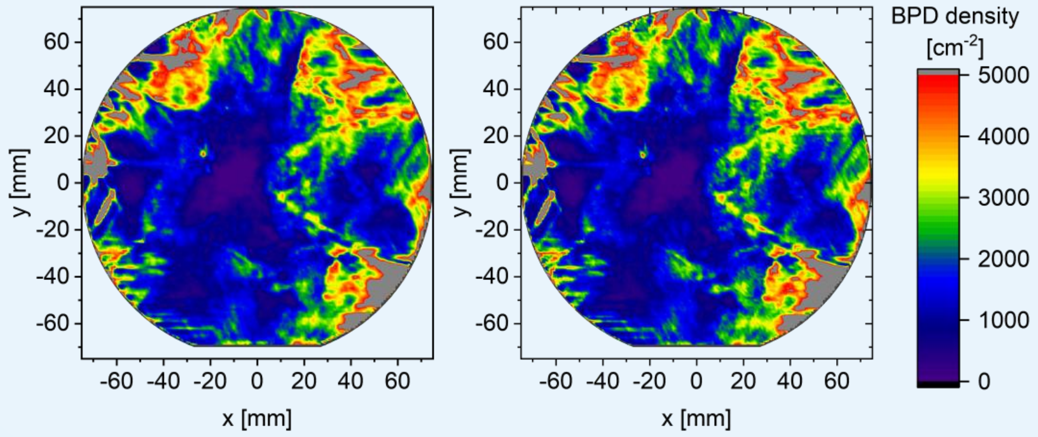
Challenges

- Rather time-consuming (~1h per 150 mm wafer)
- Sensitive to lattice curvature causing measurement artifacts
- Careful alignment is required (can be automated though)

BPD quantification

FastBPD approach

- New version of XRTmicron available on request
  - Measurement times of ~5min per 150mm wafer
  - Identical results as for standard measurement
  - Insensitive to lattice curvature → wafers that fail on standard system can be measured
  - Very simple and fast alignment
  - For sufficiently tight specs → no alignment at all



Summary

- XRT has become a mature technique ready for application in industry
  - **High accuracy, high reproducibility**
  - **SEMI-standardized procedures**
  - **High throughput**