CS International 2023

Plasma Dicing of GaAs VCSELs

18th – 19th April 2022, Brussels, Belgium

Panasonic Connect Europe GmbH, Germany*1
Panasonic Connect Co., Ltd., Japan*2

James Weber*1, Toshiyuki Takasaki*2

Panasonic CONNECT

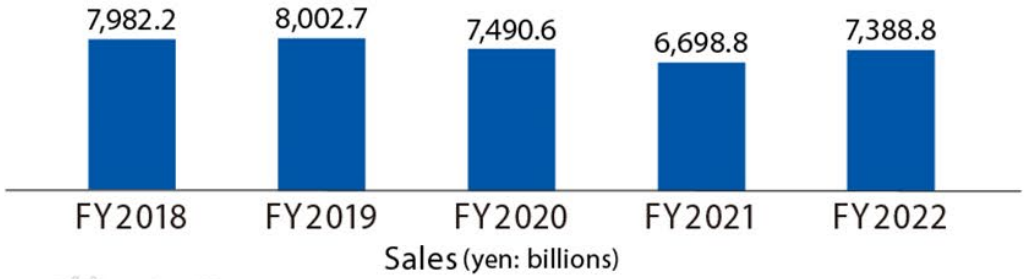
angel tech CS INTERNATIONAL CONFERENCE

Panasonic Corporation

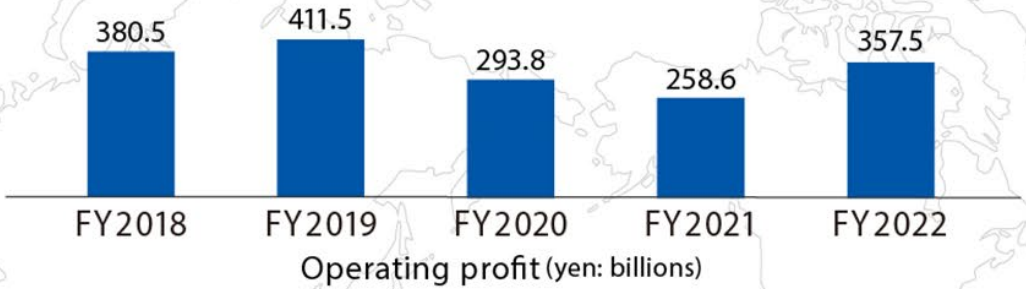
Yuki Kusumi
Group CEO

Head Office	Kadoma City, Osaka, Japan
Sales	¥ 7,388.8 billion
Employees	approximately 240,000
Group Companies	532

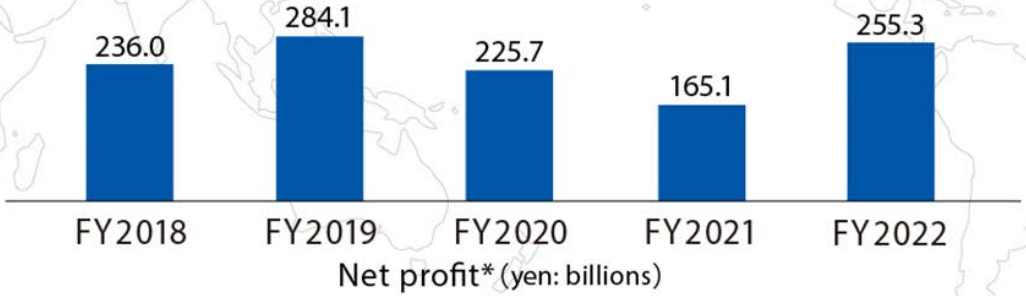
*As of March 31, 2022



Sales (yen: billions)



Operating profit (yen: billions)



Net profit* (yen: billions)

*attributable to Panasonic Corporation stockholders

FY2022 : Fiscal year ended March 2022

Panasonic Group Structure

Up to March 2022

Panasonic Corporation

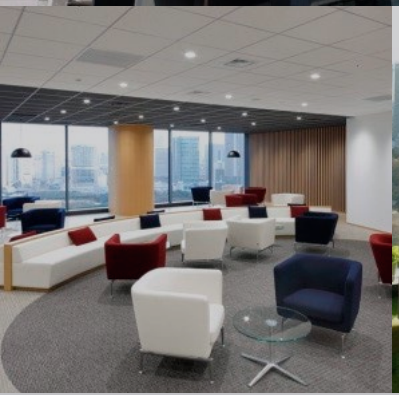
- Corporate Strategy & Technology Sector
- Lifestyle Updates Business Division
- Automotive Company
- Entertainment & Communication Business Division
- Housing Systems Business Division
- **Connected Solutions Company**
- Industry Company
- Energy Company
- Operational Excellence Company

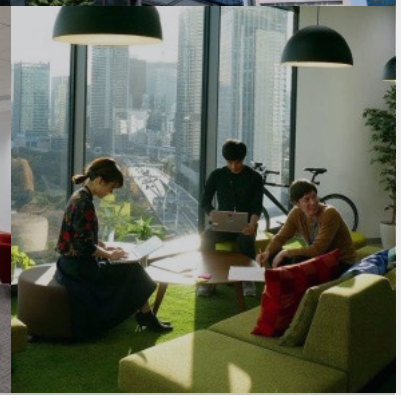
From April 2022

Panasonic Holdings Corporation

- Panasonic Corporation
  - China and Northeast Asia Company
  - Living Appliances and Solutions Company
  - Heating & Ventilation A/C Company
  - Cold Chain Solutions Company
  - Electric Works Company
- Panasonic Automotive Systems Co., Ltd.
- Panasonic Entertainment & Communication Co., Ltd
- Panasonic Housing Solutions Co., Ltd.
- **Panasonic Connect Co., Ltd.**
- Panasonic Industry Co., Ltd.
- Panasonic Energy Co., Ltd.
- Panasonic Operational Excellence Co., Ltd.

Company Overview





Company Name	**Panasonic Connect Co., Ltd.**
Head Office Location	Sumitomo Fudosan Shiodome Hamarikyu Bldg., 8-21-1 Ginza, Chuo-ku, Tokyo 104-0061, Japan
Tel	+81-3-5565-8700
Web	https://connect.panasonic.com/en
Foundation	April 1, 2022
CEO	Yasu Higuchi
Business	Development, manufacture and sale of devices, and provision of solutions, including system integration, installation, maintenance and repair services for the supply chain, public service, infrastructure, and entertainment sectors.
Employees	Approx. 28,500 (Japan: 12,500; Overseas: 16,000) (as of April 1, 2022)
Annual Sales	JPY924.9 billion (FY2022)
Business Sites	Japan: 13 (incl. 4 factories), affiliated companies: 11; overseas: 24 (as of April 1, 2023)

Panasonic Connect Europe – Business Areas

Panasonic Connect Europe GmbH

Managing Director Hiroyuki Nishiuma

MSBD – Mobile Solutions BD

Head: Daichi Kato

MEBD – Broadcast & ProAV BD

Head: Jan Markus Jahn / André Meterian

MEBD – Visual System BD

Head: Jan Markus Jahn / David Sempere

PFSE – Smart Factory Solutions

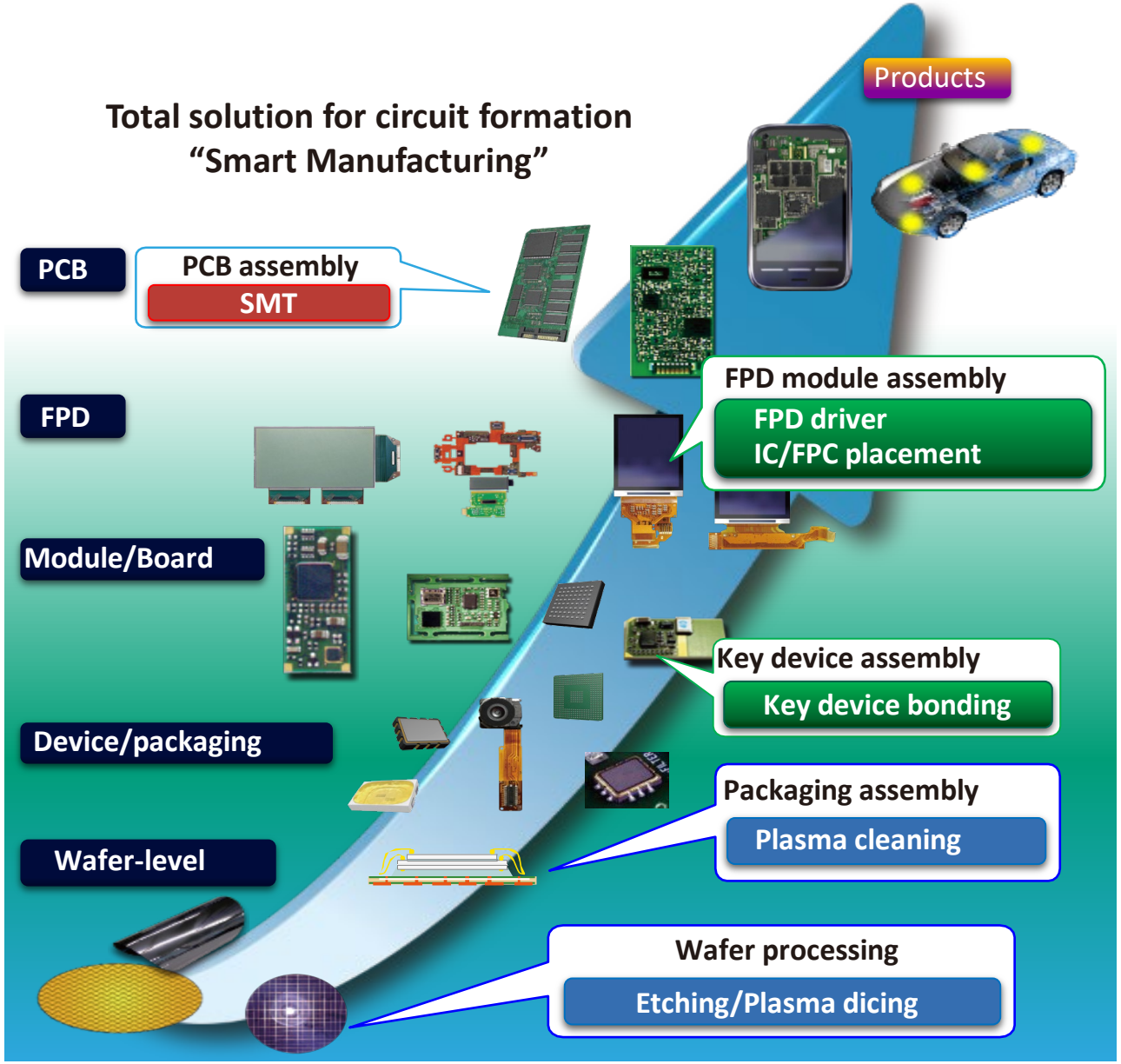
Head: Akira Yamashita

B&I – Business & Industry BU

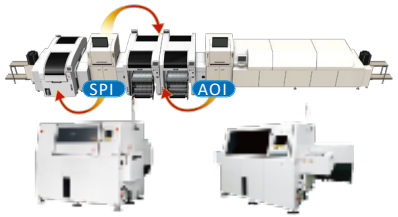
Head: Shawn Aoki

Process Automation Business Division

Total solution for circuit formation
"Smart Manufacturing"



Surface mounting



Surface mounting for electronic circuit board

- Chip mounter
- Screen printer
- Insertion machine for lead component
- Insertion machine for odd-shape component

High-precision bonding

FPD Driver IC/FPC placement

- COG bonder/FOG bonder

Key device placement

- Die bonder/Flip chip bonder

High-precision processing

In this presentation

Etching and dicing

- **Dry etcher**
- **Plasma dicer**

Cleaning

- Plasma cleaner

Dry Etching

Device/Technology trends to support 5G, IoT, AI

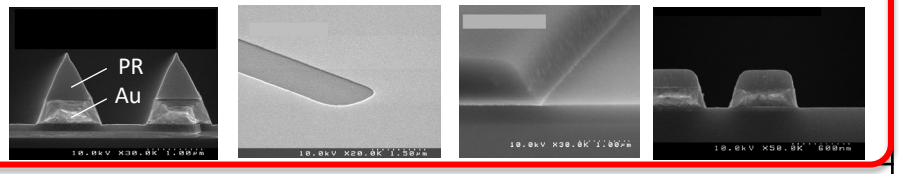
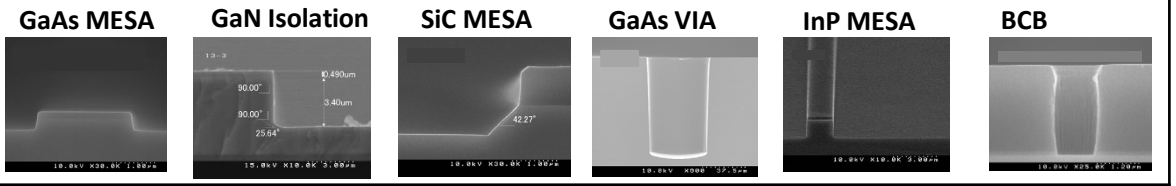
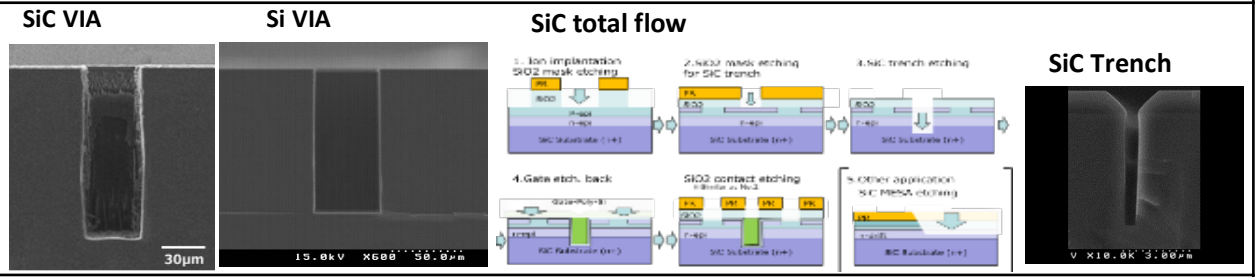
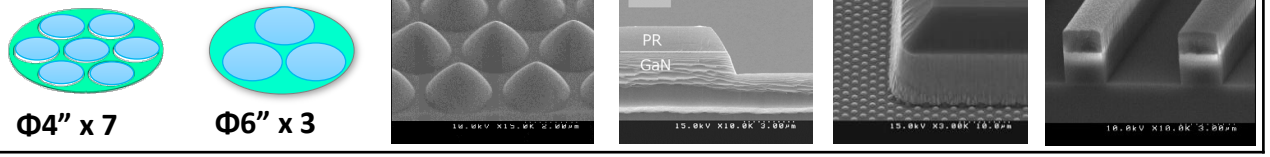
Market trends	5G, IoT, AI ～Data center, IoT device, AI chip～					
Device	CPU・GPU/Memory/ Image sensor	**Power semiconductor**	**Optical communication**	**High frequency communication**	**RF module** Filter+Switch+Amplifier	**MEMS**
Technology trend	○Broadband in chips・Low energy consumption・High speed signal transmission ○Mixture of different chips	○**Use new material** High power：**SiC** High speed：**GaN**	○Increase of communication capacity/speed, achieve low energy consumption and machine enlargement. ○Larger data center、Long distance and large capacity communication **（Surface emission laser）** ○5G frequency band、antenna with multiple elements **（GaN HEMT、InP）**		○Mixture of 4G/5G, increase frequency band ○**SAW：HAL structure** （Hetero Acoustic Layer） ○**BAW：New piezo MEMS structure**	○Rapidly increase **RF MEMS** market with 5G ○Expend use of sensor for IOT **（angular velocity sensor, gyro sensor）**
Market size/growth rate From Yole Development	2019:29M wafers 2025:43M wafers CAGR 7% 2019-2025	SiC/GaN 2019:$630M 2025:$3950M CAGR **35.8%** 2019-2025	2020:$1.1B 2025:$2.7B CAGR **18.4%** 2020-2025	2019:$740M 2025:$2B CAGR **12%** 2019-2025	2020:$15,215M 2025:$25,398M CAGR **11%** 2019-2025	2019:$11.5B 2025:$17.7B CAGR **7.4%** 2019-2025
Advanced-PKG technology	Plasma dicing for 3D stacked device		Plasma dicing for compound		Plasma dicing for Wafer-on-Wafer structure	

Panasonic equipment introduction

Dry Etching

Plasma Dicing

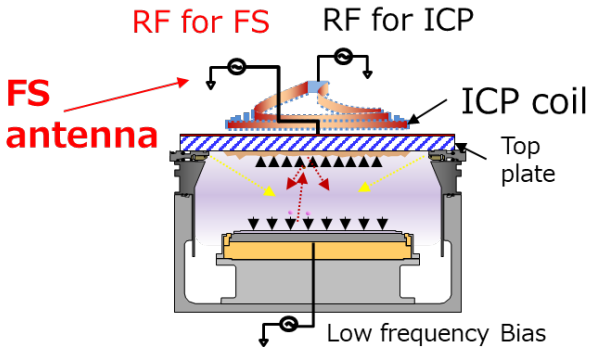
Dry Etching Solutions for Compound Semiconductors

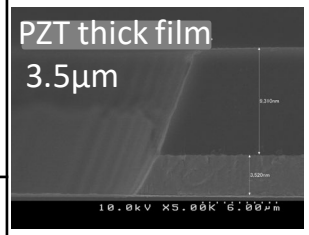
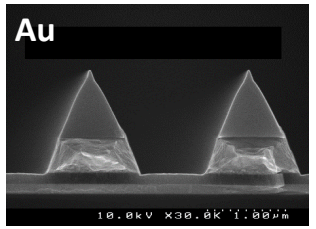
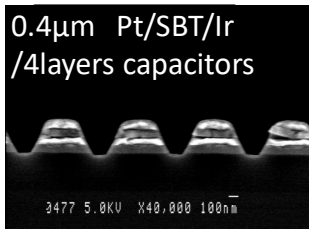
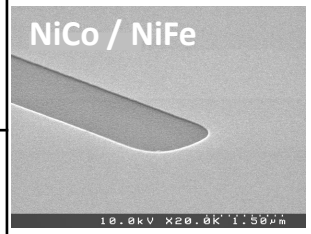
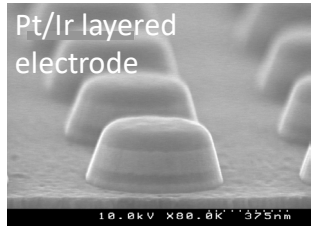
Machine/Specifications	Applicable Devices
 New APX300-S **FS-ICP**	**Long MTBC*1 ICP Process for Non-volatile materials** *1 MTBC : mean-time-between-clean Au / PZT / Pt for Piezo MEMS Magnetic film, Metal wiring for MEMS and Magnetic sensor Capacitor for compound 
 APX300-S **MSC-ICP**	**High Precision Multi-Spiral-Coil ICP Process** GaAs High Frequency / Optronics (Recess, GaAs MESA, VIA) GaN High Frequency / Optronics (Recess, MESA, Isolation) InP Optronics (MESA, VIA) SiC Power (MESA, Trench, Etch. Back) Passivation (SiO2, SiN, BCB, PI, etc.) 
 APX300-S **BM-ICP**	**High Density Plasma Process** Si / SiC VIA for GaN HEMT All SiC trench process (SiO2 mask, Trench, Etch-Back) 
 APX300 Batch processing	**Batch Processing for Mass-production** LED (PSS, GaN MESA, GaN Isolation, SiO2, etc.) SiO2 mask etching, etc. 

APX300-S FS-ICP / Ashing & Rinse Chamber Specification

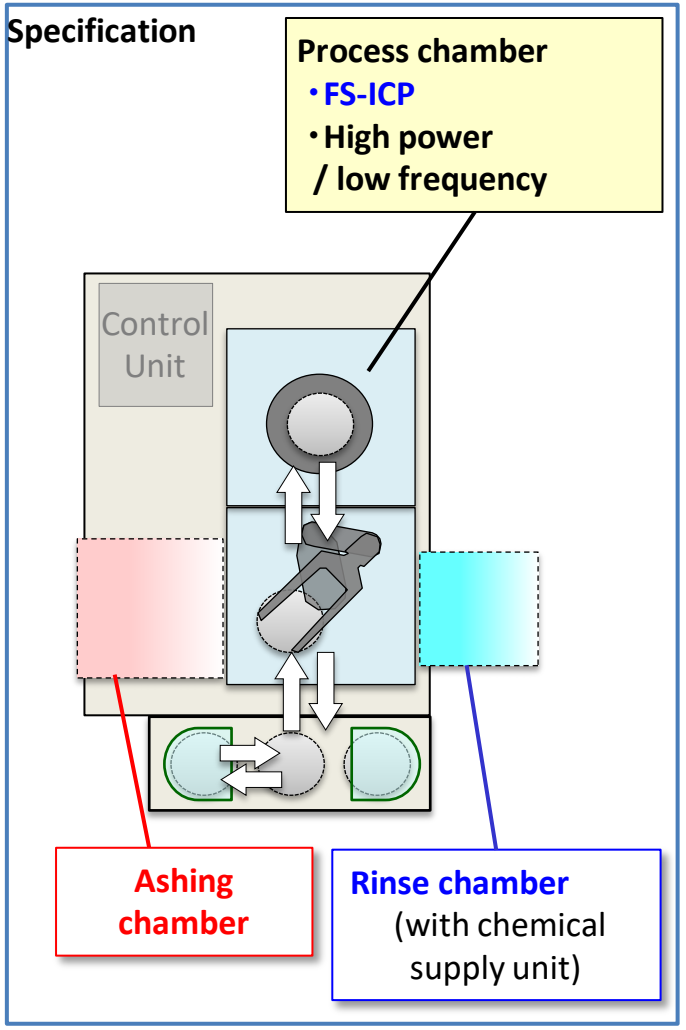
Characteristic

- FS-ICP plasma source:
  - Remove deposition at top plate by FS antenna
    Achieve long MTBC for non-volatile materials
  - Applying RF power to ICP and FS antenna
  - Achieve wide process window and stability
- Ashinig / Rinse chamber:
  Remove resist and prevent Cl・F corrosion by in-line ashing/rinse



Device	Application	Example of processing
Piezo MEMS	**Au/PZT/Pt Piezo element,** Insulation film	  
MEMS Magnetic sensor	**Magnetic film, Metal wiring,** Insulation film	  Etching rate Au ≧400nm/min. Pt ≧200nm/min. PZT ≧180nm/min. Uniformity within wafer ≦±5% wafer to wafer ≦ ±1%
Si、Compound semiconductor	Capacitor	

Specification



Stable Process can be achieved by using FS-ICP to remove deposition at top plate

APX300-S/APX300 Applications

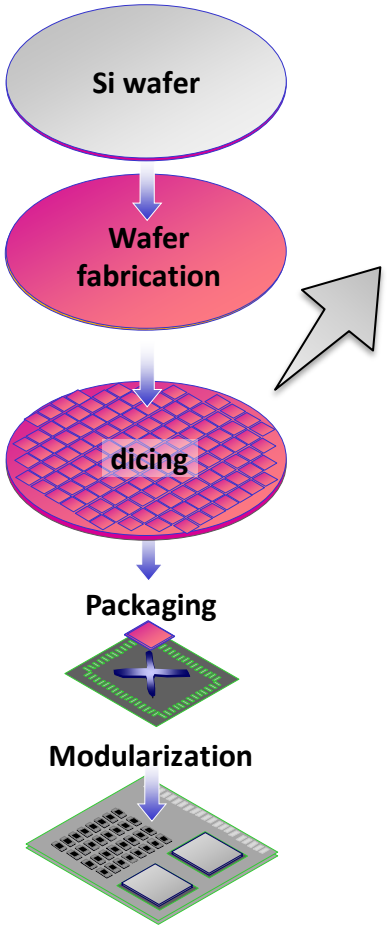
Dry Etching Material		Device		
		Compound Semiconductor	Electric device	Silicon semiconductor
		Communication device, Optical device, LED	MEMS, sensor, Automotive device, SAW	Power device CMOS, FeRAM
Silicon	Deep-Si	-	●	●
Wiring material	Poly-Si, WSi, Diamond	●	-	●
Insulation film	SiO2, SiN, SiON	●	●	●
Protection film, resin	Polyimide, BCB	●	●	●
Compound	SiC	●	-	-
	GaAs, AlGaAs, InP, InSb, GaP	●	-	-
	GaN, AlGaN, InGaN	●	-	-
Metal	Al, AlSi, AlCu, AlSiCu, AlN, Ti, TiN, TiO2, W, Mo, Ru, Cr, Ta, ITO, HfO2, Ta2O5	●	●	●
	Au, Pt, Ir, Cu	●	●	●
Substrate・ferroelectrics・Magnetics	Sapphire（Al2O3), LiTaO3, LiNbO3	●	●	-
	PZT, SBT, STO, NiCo, NiFe	●	●	●

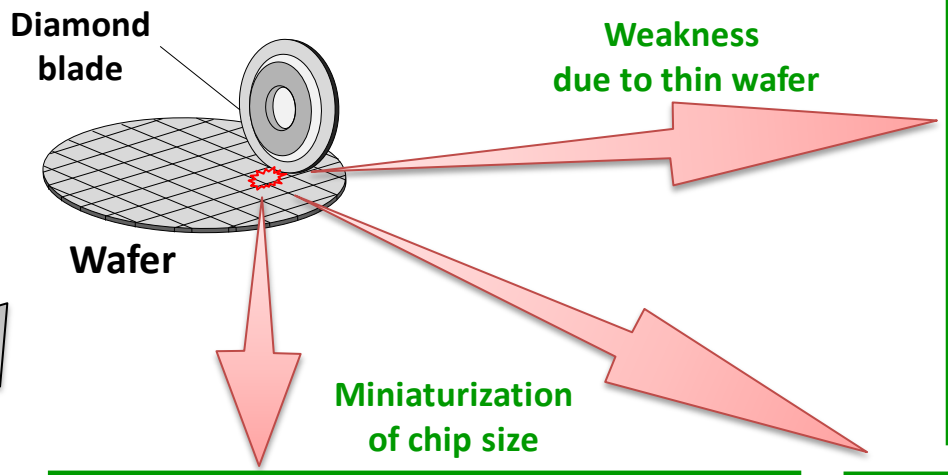
● ：Experienced with APX300S／APX300

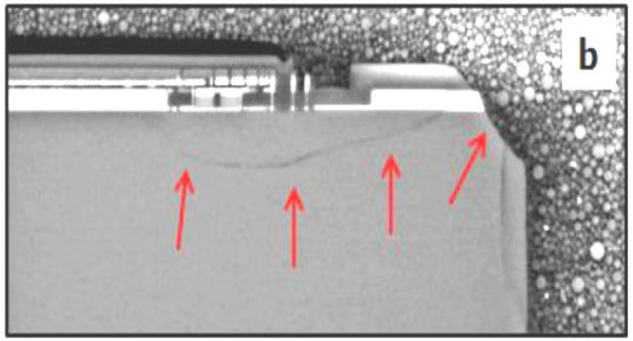
● ：Experienced with APX300S

Plasma Dicing

Issues with Conventional Dicing Methods

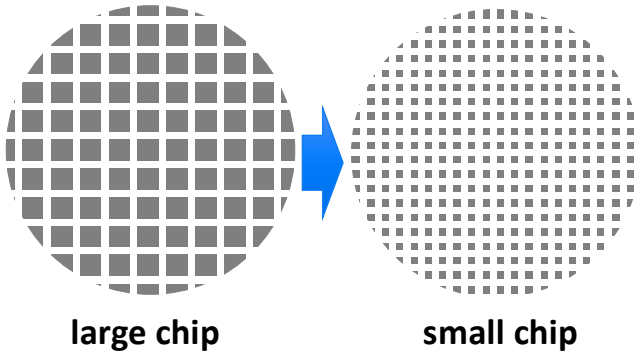






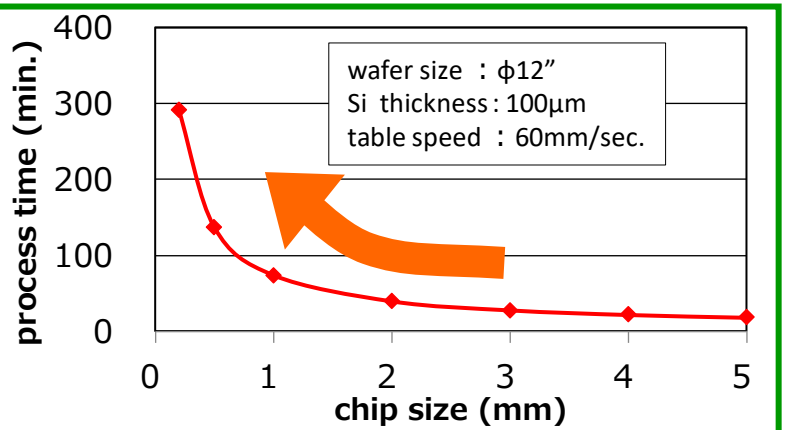
Chipping

Source) A.Hooper et al, ECTC2015



Increasing loss area

due to blade width

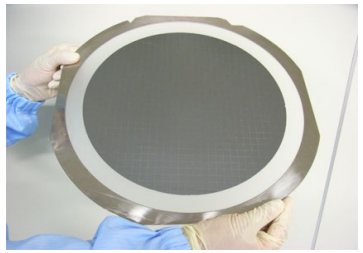


Increasing process time

due to increasing line amount

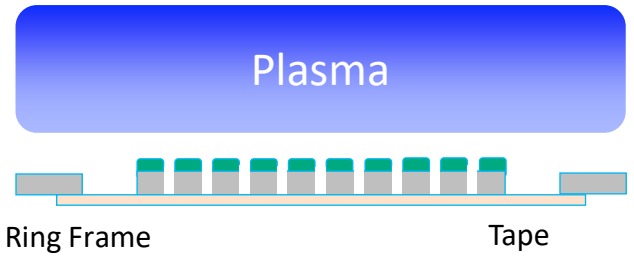
Principle of Plasma Dicing

■ Mounted on FFC, Patterned

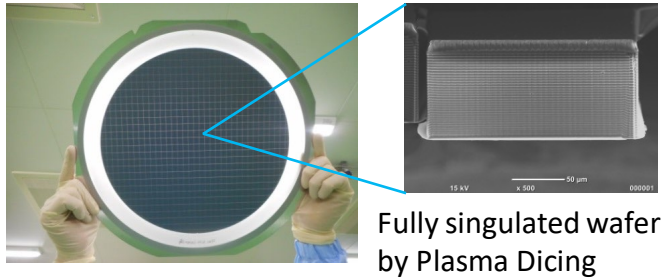


Wafer mounted on ring frame with tape

Transfer in Process Chamber

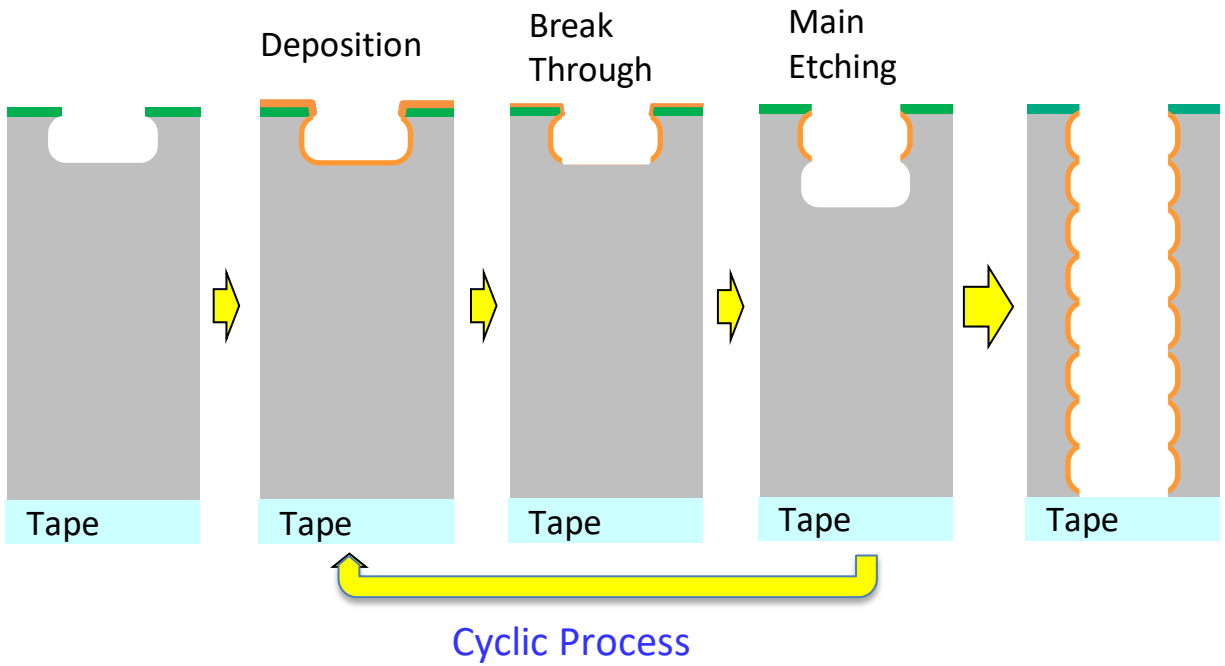


Transfer from Process Chamber



Fully singulated wafer by Plasma Dicing

■ Bosch Process (cycle etching)

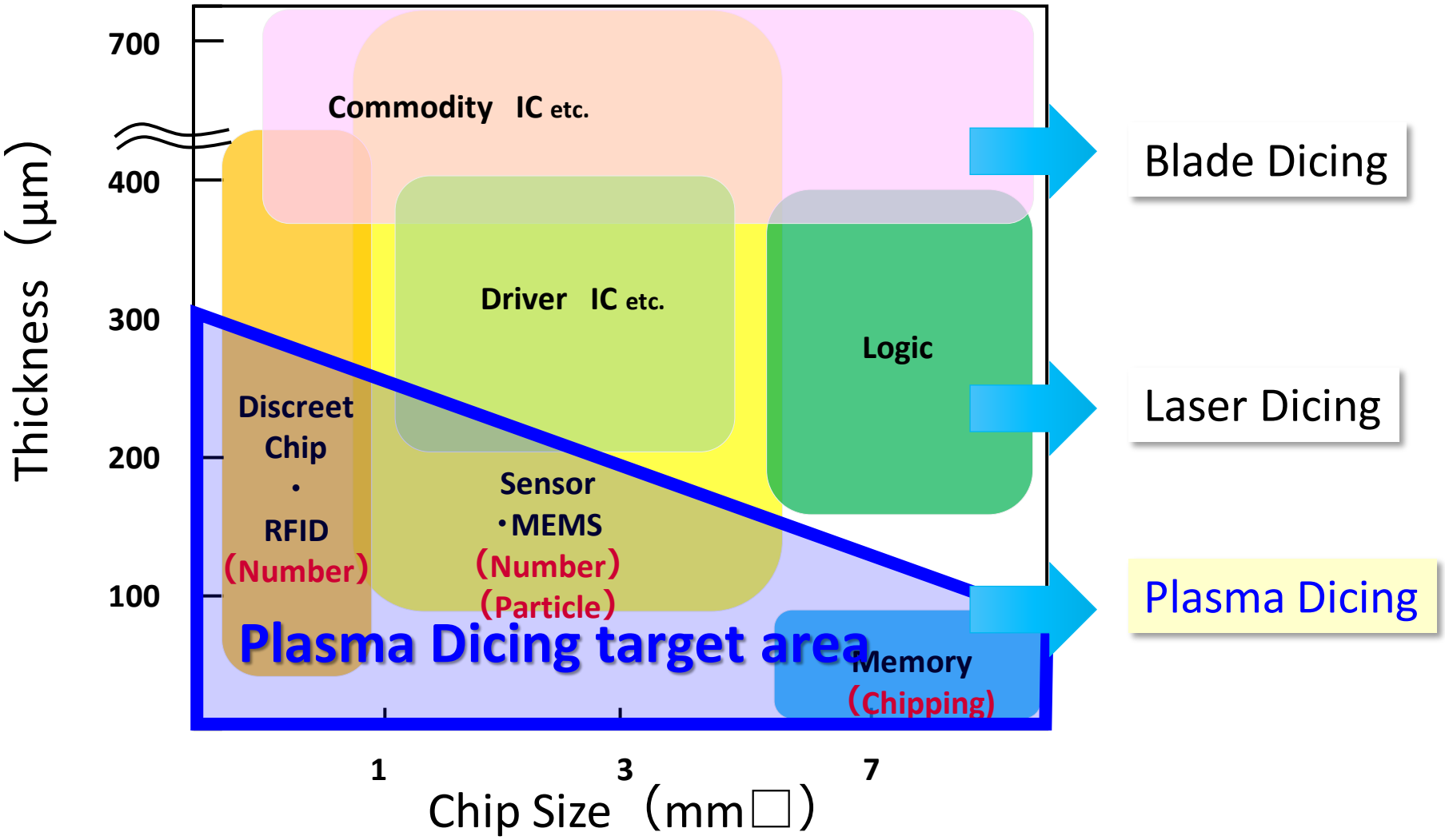


Wafers mounted on ring frame with tape are diced without damage.

Special hardware and processes are key technologies.

Plasma Dicing Target Market

Thin and small chips are the target market of plasma dicing

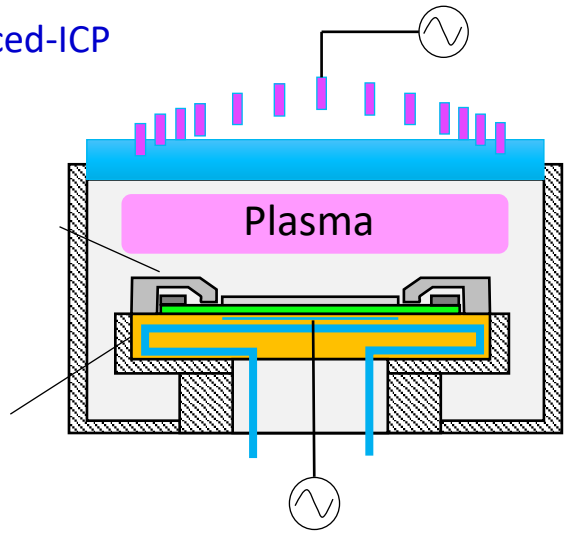


Plasma Dicer APX300-DM (Dicer Module)

Patented Enhanced-ICP

Patented Dicing Ring Cover

Patented Panasonic Original ESC Electrode

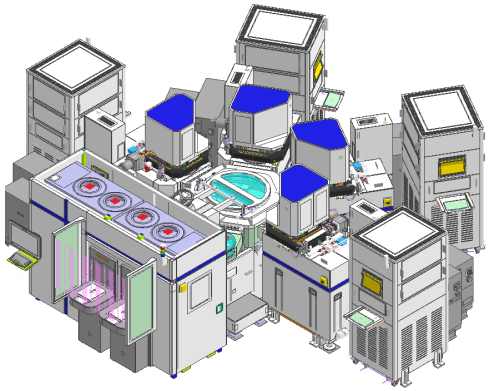


・Configuration of APX300-DM Process Chamber

・APX300-DM has optimized elemental technologies for Plasma Dicing

1. Enhanced ICP Plasma Source : High density and uniform plasma
2. Plasma Dicing ESC Electrode & Dicing Ring Cover
   ・Patented Panasonic design enables the Plasma Dicing process to be performed on wafers mounted on ring frame with tape
   ・Strong chucking force and cooling enables almost all dicing (DC) tape to be used.
   ・Eliminates exposure of the tape and frame to plasma
3. Etching performance
   ・Process chamber that can use both Fluorine-based and Chlorine-based etching gasses. Compound Semiconductor etching is possible
   ・Multi layer dicing (SiO2, SiN, DAF & Si) is possible
   ・Si etching rate up to 35µm/min. ≦±3%

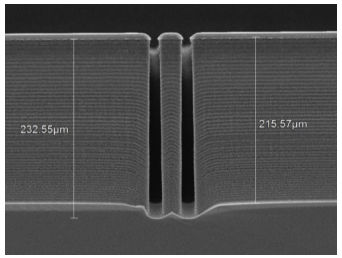
Plasma Dicing Solutions for Various Semiconductors

Machine/Specification	Applicable Devices
APX300-DM 	**Compound Semiconductor, Small Chips, MEMS and R&D** Material: Si / SiO2 / SiN / SiCN / GaAs / GaN etc., Wafer size: φ4 ~ 8inch wafer with frame for φ8inch φ12inch wafer with frame for φ12inch Max. chamber: 1ch (single chamber type)
New APX300-PD 	**Memory (DRAM, NAND), Image Sensor, Logic** Material: Si / SiO2 / SiN / SiCN etc., Wafer size: φ8~12inch wafer with frame for φ12inch Max. chamber : 4ch (multi chamber type)

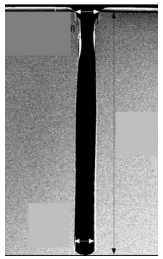
■ **Narrow street etching**

Si dicing 5um X 175um

Si double line 10um X 220um

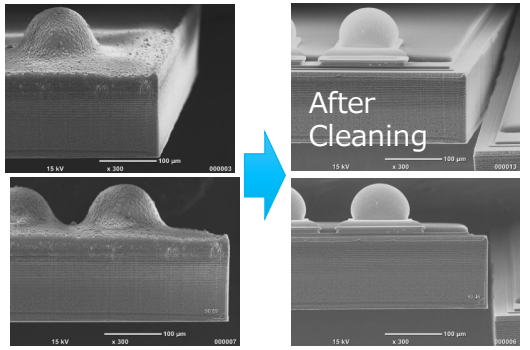


GaAs Plasma dicing 15um X 160um



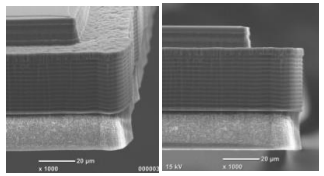
■ **Characteristic plasma etching**

Ball bump/Device-layer/Si

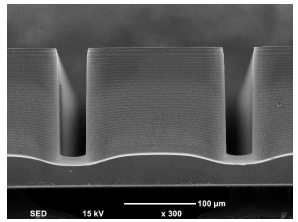


After Plasma dicing **After Washing**

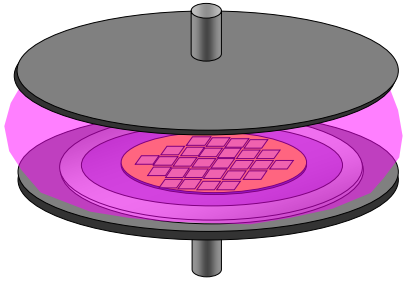
Si with DAF



GaAs smooth sidewall



Benefits of Plasma Dicing



No Damage & No Chipping

- Dicing of thin & fragile wafers w/o damage
- Possible to reduce the kerf margin
- Possible to dice with low device damage

High Productivity & Low CoO

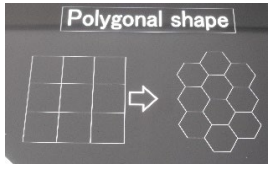
- Parallel processing
- Narrow dicing width and kerf margin by elimination cracks increases the amount of dies

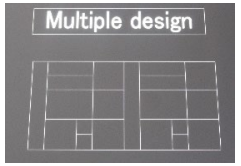
No Dust & No Particle

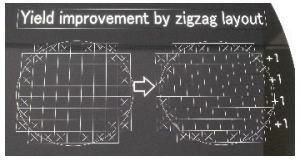
- Clean chemical etching process
- No mechanical dust, debris, vibrations, water pressure etc.
- Potential to reduce inspections

Variant Chip Shape & Layout

- Flexible die shapes and non-orthogonal layouts

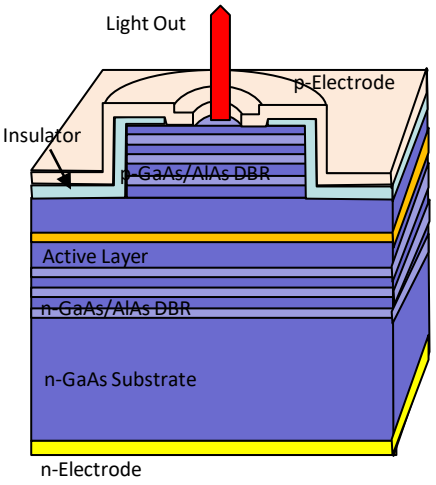






Trends of VCSEL Market and Technology

VCSEL Structure

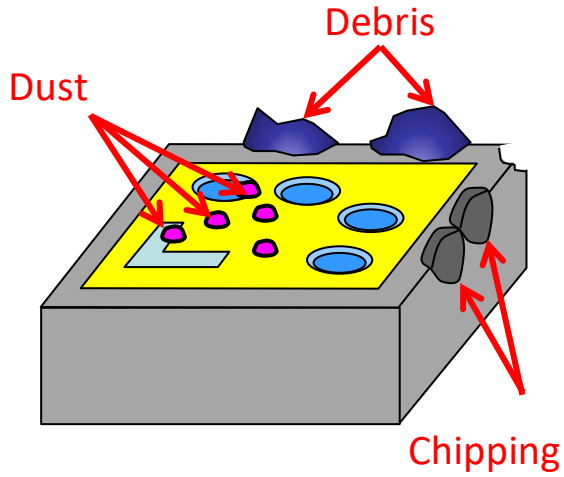


VCSEL: Vertical Cavity Surface Emitting LASER

- Densely-packed laser 2D-array structure
- Low power operation due to small size
- Applications :
  - Laser Mouse, Laser Printer
  - Optical Communication
  - Interconnection between data centers
  - Sensing (ToF, Gesture, etc.)

Application Expansion

VCSEL Dicing Issues



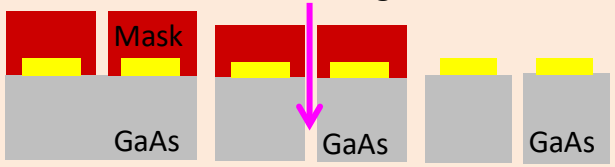
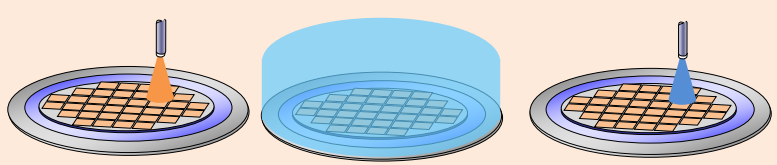
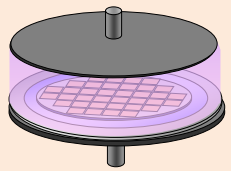
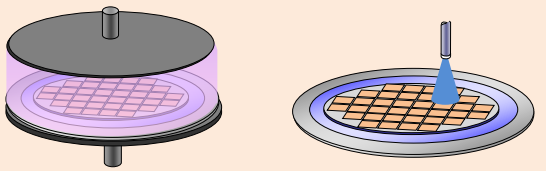
Conventional Methods (Blade or Laser Dicing)

- Physical & heat damage
- Dust on chip
- Wide dicing street width & kerf margin
- Arsenic compound contamination water

Market requirements : Damage free, No dust No debris, less contaminated water, Improved yield per wafer

Panasonic provides a new dicing technology “Plasma Dicing”

Plasma Dicing Process Flow for VCSEL

Cross-section of Wafer	Process		
	Mask Patterning	Plasma Dicing	Mask Stripping
			

-VCSEL Plasma Dicing Requirements

Mask Patterning

- Photo-lithography patterning on metal ring frame and tape
- Narrower street width (≦30μm) and narrower kerf margin

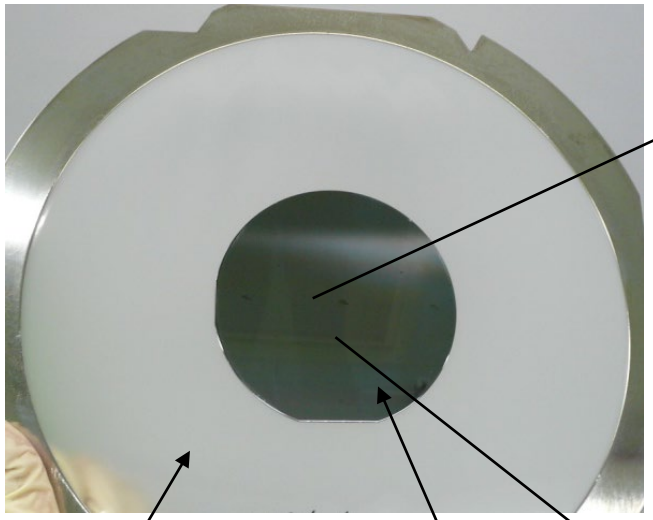
Plasma Dicing

- No physical/heat damage to chip
- Etching depth of GaAs ≧100μm

Panasonic proposes the use of photo-lithography and Plasma Dicing integration for small chip VCSEL dicing.

Photo-lithography on GaAs Wafers with Ring Frame and Tape

→ Panasonic tested the photo-lithography
Sample : Novolak Photo Resist (PR), GaAs substrate, Polyolefin Dicing tape, Φ200mm ring frame

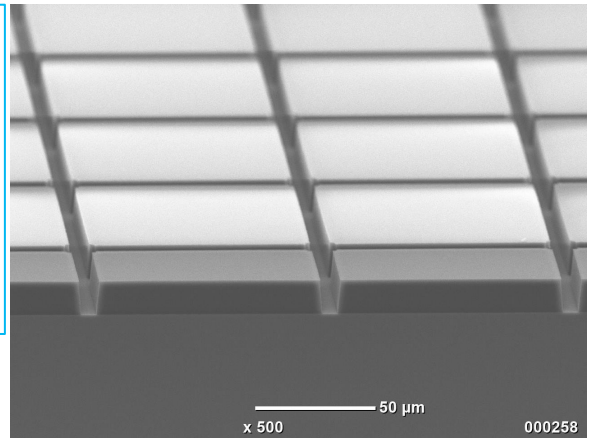


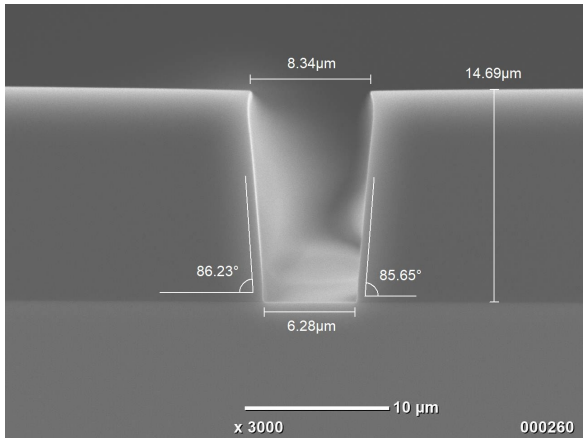
No tape damage

Thin GaAs substrate
Φ2” up to Φ8”

Thick PR
High Aspect Ratio (A/R) Exposure

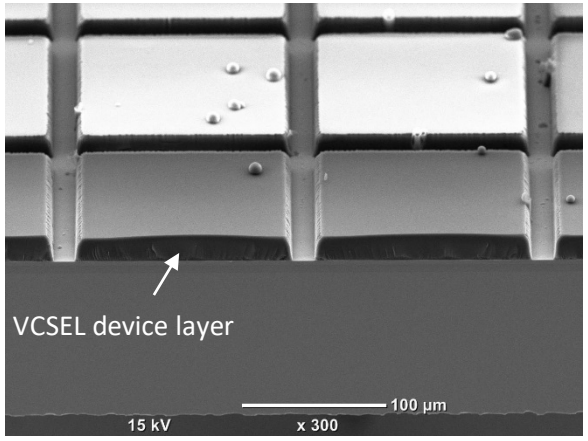
PR thickness =14.6µm
Dicing width = 6.3µm
A/R = 2.3

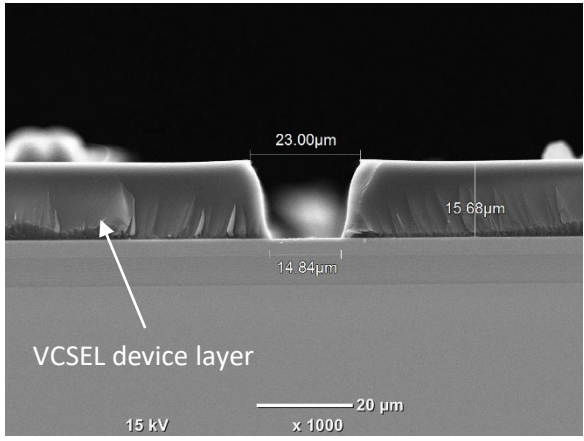




PR Mask on VCSEL

PR thickness = 15.7µm
Dicing width = 14.8µm
Completely covered on VCSEL device structure

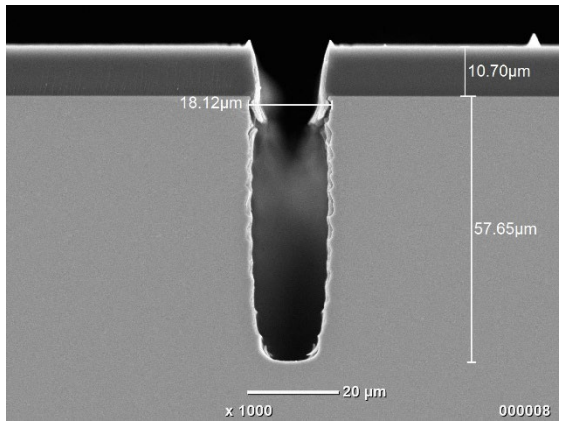




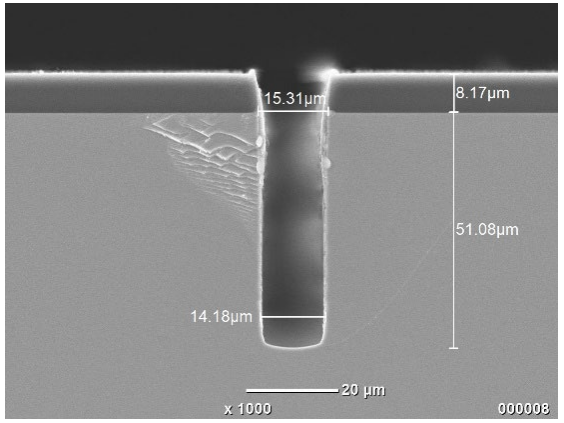
Panasonic can perform photo-lithography on metal frame and tape. Coating, Alignment & Exposure and Development with ring frame and tape enable this technology to be applied on wafers from Φ2” GaAs to Φ8” GaAs

Results of GaAs Plasma Dicing: “Etching Profile Control”

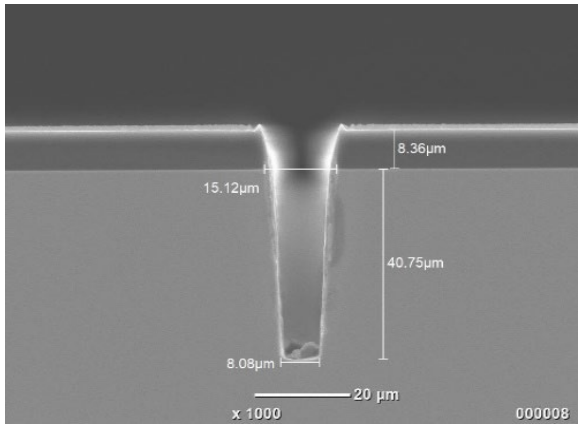
■ Profile Control



Bowing



Vertical

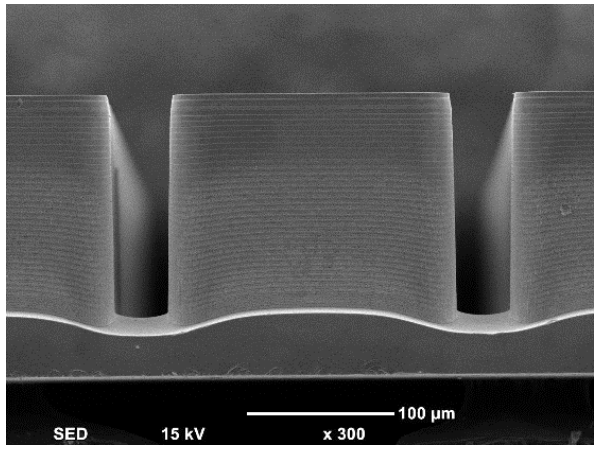


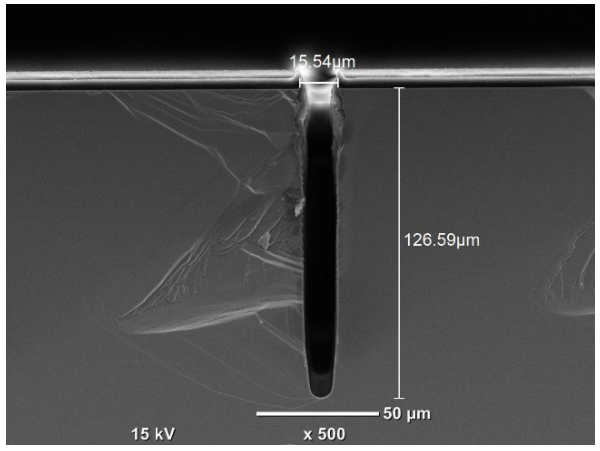
Taper

・Etching profile can be controlled

85 deg. ~ 90 deg.

■ High A/R GaAs Dicing



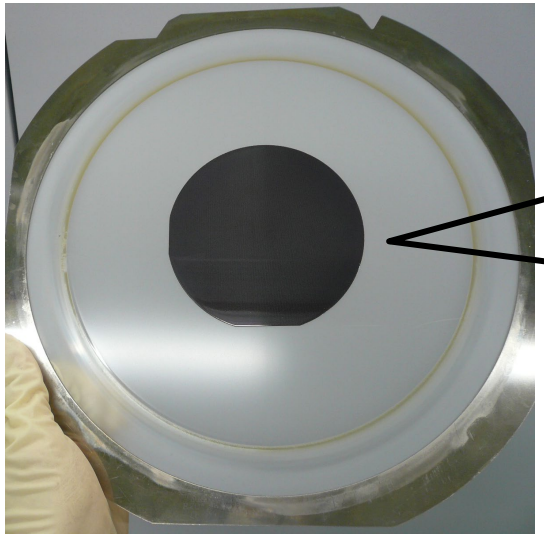


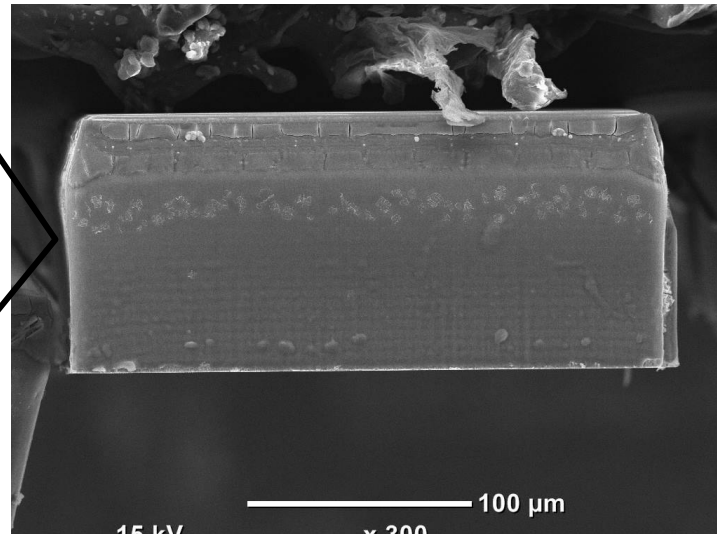
Etching Depth : 127µm
Dicing Width : 16µm
A/R : 8
Profile : Vertical

Very high A/R process can be applied to GaAs VCSEL Plasma Dicing.

Results of GaAs Plasma Dicing

→ Panasonic tested the photo-lithography and Plasma Dicing
Sample : Novolak PR, GaAs substrate, Polyolefin Dicing tape, Φ200mm metal ring frame
Condition : 1. Lithography (coat → pre-bake → exposure → develop →Post bake) to wafer with ring frame
2. Plasma Dicing





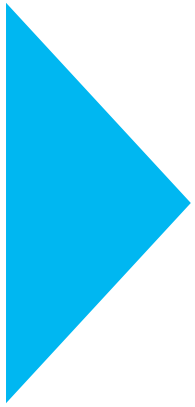
GaAs Etching Rate (E/R)	≧	8.0µm/min.
E/R Uniformity @ 6inch	≦	±3.0%
GaAs:PR Selectivity	≧	22
Etching profile		Vertical
Tape damage		None

- Possible to use Chlorine-based gas etching process without DC tape damage
- High GaAs etching rate and high PR selectivity was achieved
- Vertical etching profile was achieved

Typical Etching Speed of a GaAs Wafer

Example Parameters

4“ or 6“ wafer
150 µm thick
25 – 35 µm dicing streets
Au backside possible



~ 35 – 45 mins

Plasma Dicing time

Demo Centers in Osaka

■ Plasma Dicing Demo Center

Location: Osaka, Japan
Floor Space: 230m^2
Wafer size: Φ200mm up to Φ300mm
Equipment: Plasma Dicer, Plasma Cleaner, Back-grinder, Photo-lithography, Laser Patterning, Measurement tools, etc.

■ Dry Etching Demo Center

Location : Osaka, Japan
Floor Space : 275m^2
Wafer: Up to Φ200mm or 340mm tray
Equipment: Dry Etcher, Plasma Cleaner, Measurement tools, etc.

Panasonic provides and supports customers with the “Total Solutions Approach” for Plasma Dicing and Dry Etching, together with our partners.

Conclusions and Acknowledgments

Dry etching for compound materials

Panasonic can propose etching solutions for various compound semiconductors.

Non-volatile material such as LT, LN, Au, etc. can be etched by New FS-ICP plasma source.

Plasma dicing for compound materials

Panasonic can propose Plasma Dicing technology to singulate GaAs VCSEL wafers.

- Photo-lithography with metal ring and tape can be performed.
- GaAs substrate can be fully cut by using Chlorine-based gases.
- High-aspect-ratio GaAs Plasma Dicing process can be performed

Panasonic continues to improve Plasma Dicing technology for GaAs and we have expanded the application to other compound semiconductors such as GaN, etc.

Acknowledgments:

Thank you very much to EV Group for their ongoing support and cooperation.

Contact Information

Please visit us at our booth.

For more information in Europe, please contact our sales office:

Panasonic Connect Europe GmbH
Caroline-Herschel-Strasse 100
85521 Ottobrunn
Germany

(Near Munich)

James Weber
Senior Business Development Manager
Electronics Manufacturing Solutions

james.weber@eu.panasonic.com

Visit our website

Panasonic Microelectronics

Panasonic

CONNECT