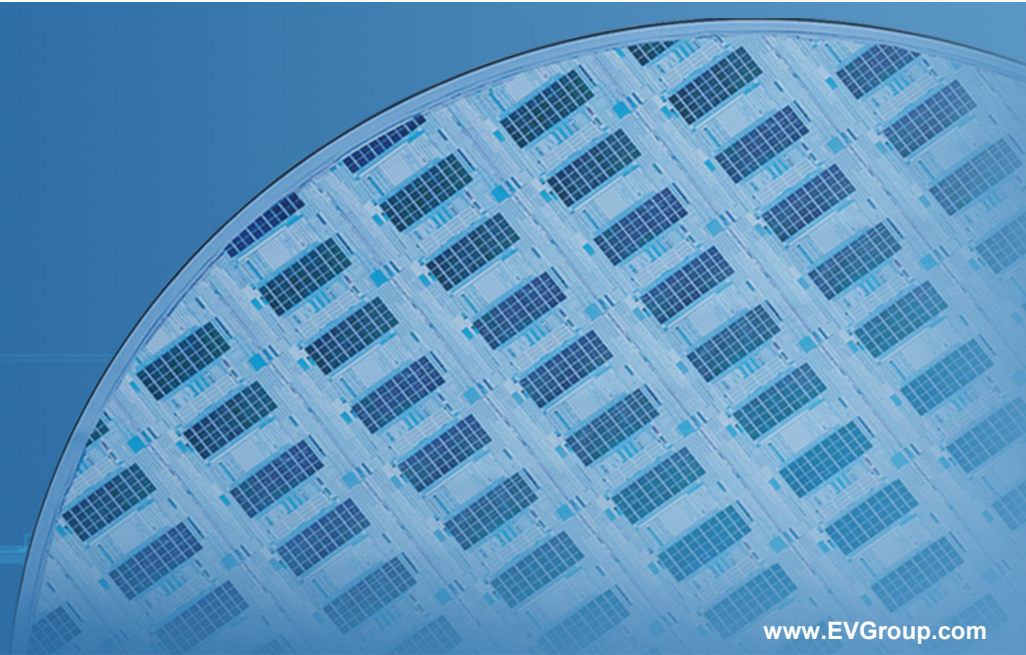
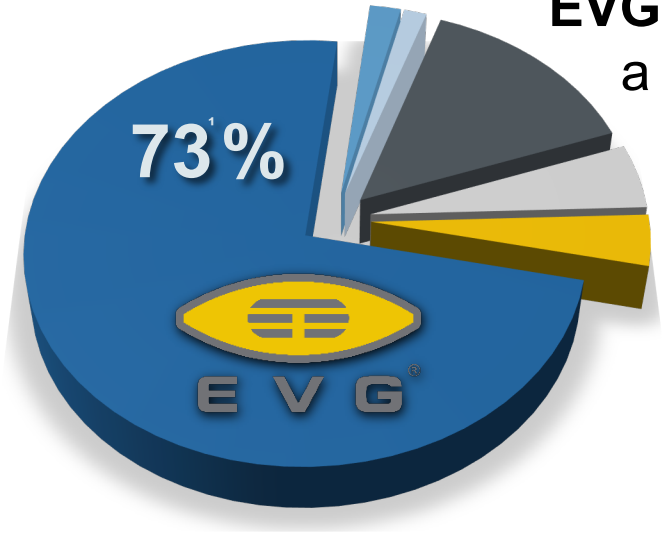
Wafer Bonding:
Technology That Enables µLED Microdisplays

Dr. Anton Alexeev, Business Development Manager



Executive Summary

Micro-Displays



EVG is an indisputable market leader in **wafer bonding**, a **key technology** for **µLED displays** manufacturing.

Our solutions go beyond bonding and enable many **µLED display** solutions for the industry leaders.

Process Development → **In-house Pilot Manufacturing** → **R&D and HVM Equipment**

Our Bonding Expertise

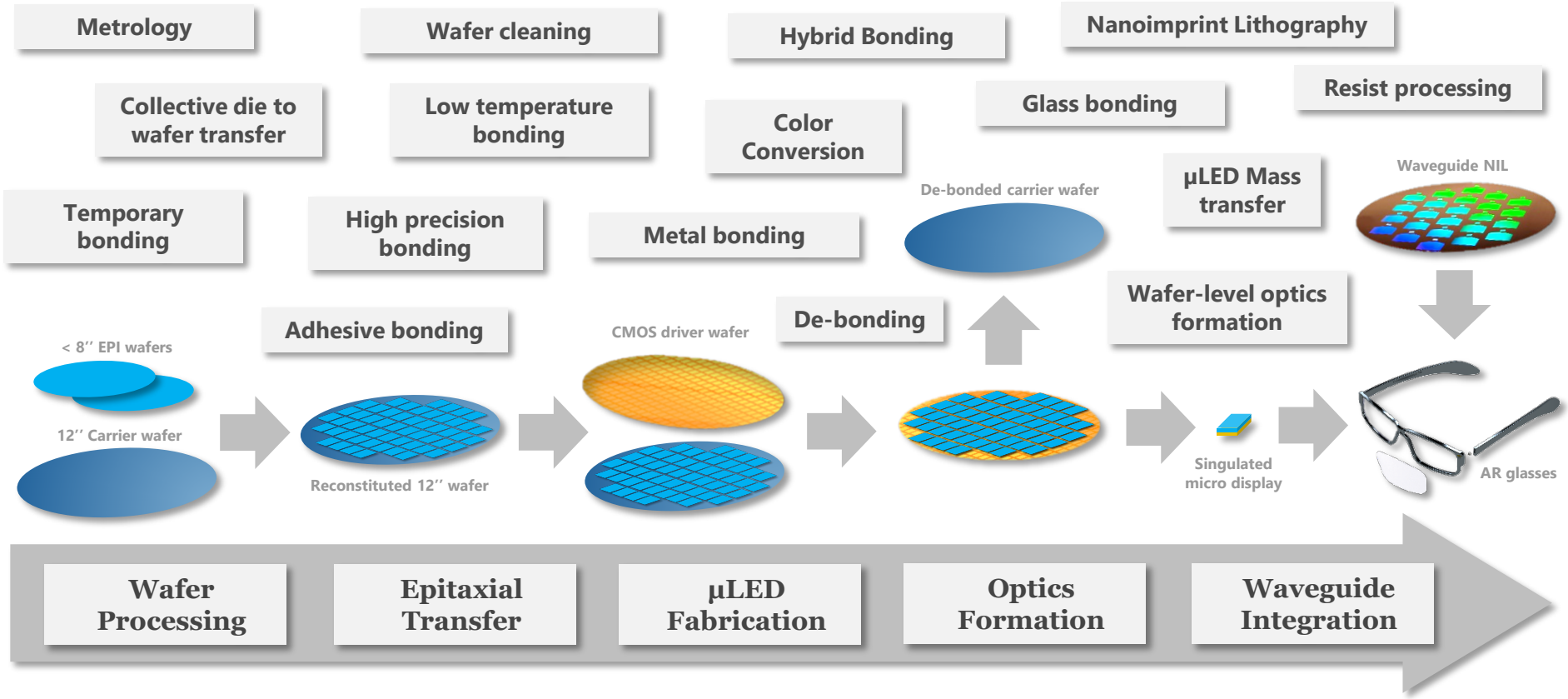
- Hybrid
- Fusion
- Plasma activated
- Adhesive
- Metal diffusion
- Wafer to wafer
- Die to wafer
- Temporary
- De-bonding

Other Technologies

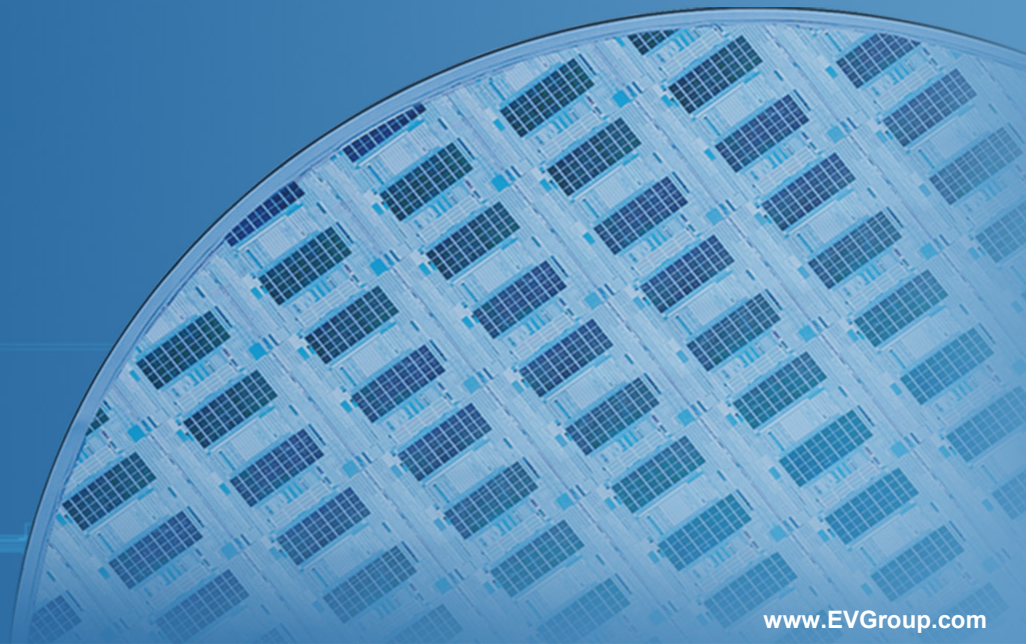
- Waveguides nanoimprint
- Wafer-level micro-optics
- Mass transfer

[1]Market report by Yole Développement 2021, permanent bonding market *"Bonding and Lithography Equipment market for more than Moore Devices"*

EVG Enables Full Process of µLED Displays Fabrication



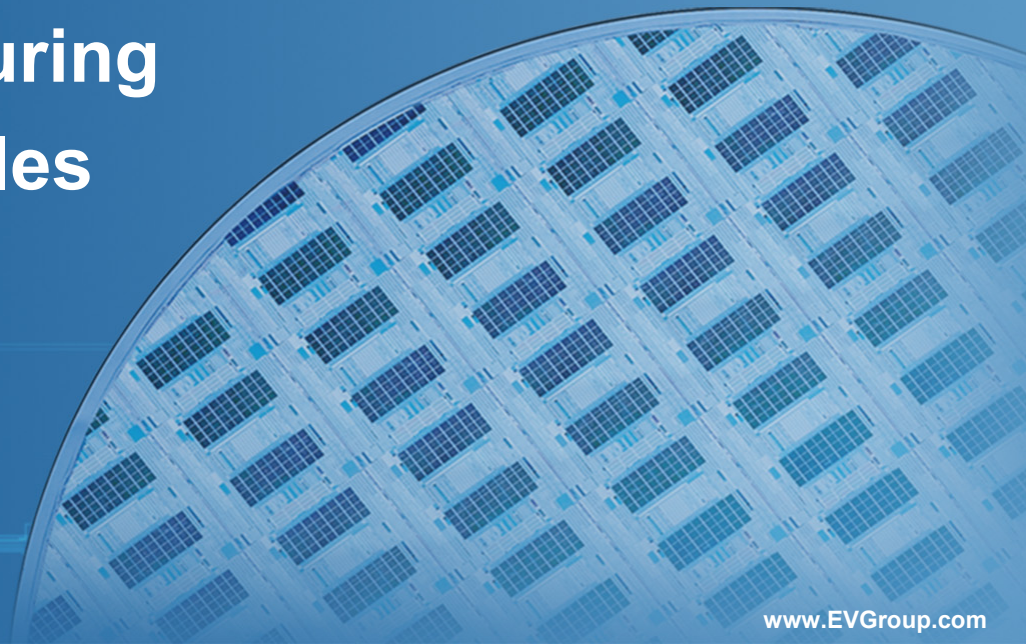
Outline



Outline

- Analysis of Micro-displays Manufacturing
  - Hybridization vs Monolithic Approach
  - Process flow examples
- Bonding Technology Demonstrators
  - No interlayer
  - Metal Interlayer
  - Insulating Interlayer
- EVG Unique Technologies
  - Substrates of Different Dimension
  - ComBond
  - Wafer Reconstitution
  - NanoCleave

Microdisplay Manufacturing & Process Flow Examples

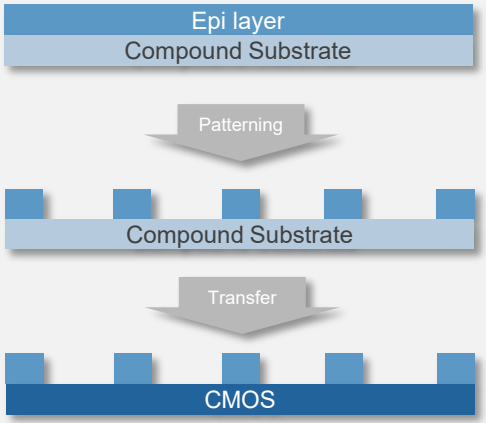


µLED Micro Display Manufacturing Process

10µm — Pixel pitch — 1µm

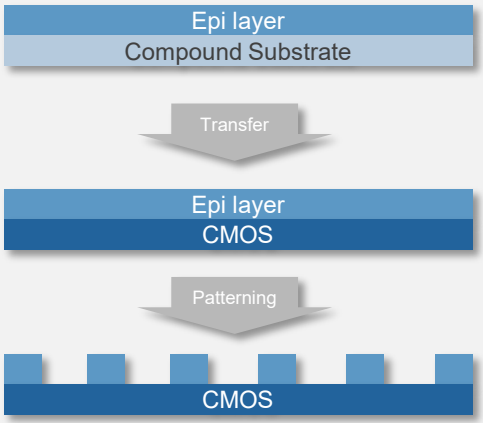
Hybridization ⟵ ⟶ **Monolithic**

Singulation First



Pitch <10µm is challenging

EPI Transfer First

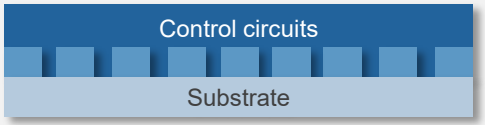


Commercialization is ongoing

EPI growth on the backplane

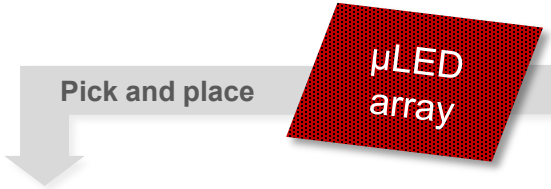
Challenging due to CMOS-EPI processing temperature mismatch

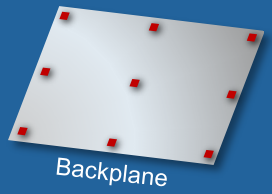
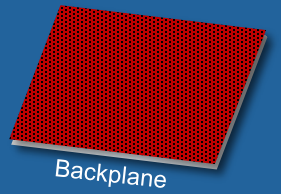
Control circuitry growth on top of a µLED array



Research is ongoing

End Products Overview

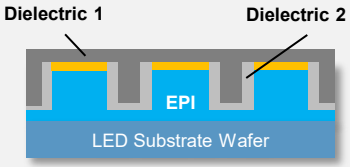


	Direct view displays		Micro Display
			
Product	**µLED Pixel**	**µLED Smart Pixel**	**µLED array on CMOS driver**
Applications	Smart watch, smart phone, laptop, TV…		AR, HUD, VR…
Further processing	Mass transfer		Integration with optics
Bottleneck	Mass transfer of the pixels		Extreme pixel pitch

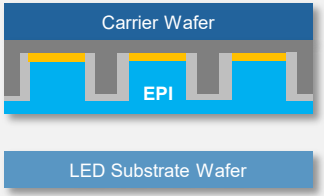
The next slides exhibit a representative but not a full list of EVG technologies for µLED displays manufacturing. The process flows vary significantly company to company.

µLED | Pixel

1. Epi Patterning + Etching, Deposition



2. Adhesive Bonding, Substrate Laser Lift Off



3. GaN etching, CMP

4. Etching, Annealing

Next step: mass transfer

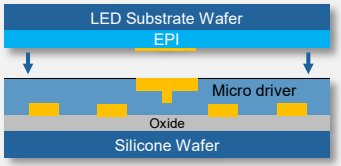
EVG Technology	Application	Equipment
Optical lithography	Patterning of the EPI wafer to singulate the µLEDs	6XX IQ aligner
Spin & Spray coating	Adhesive coating	1XX
Adhesive bonding	EPI transfer + LED transfer	5XX 850 Gemini
Laser Lift Off	EPI substrate removal	850DB

µLED pixel process is the least complicated.

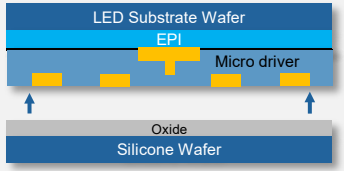
Nonetheless, advanced solutions with multiple selective-etched dielectric layers are common.

µLED | Smart Pixel

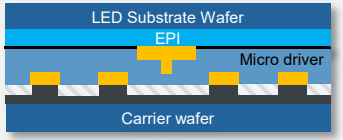
1. Adhesive bond, Metal aligned bond



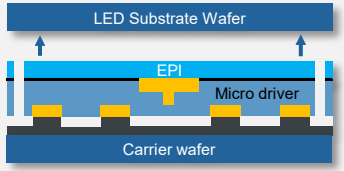
2. Debonding



3. Adhesive bonding



4. Substrate LLO, Patterning + Etching



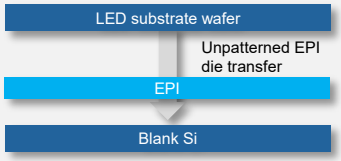
Next step: mass transfer

EVG Technology	Application	Equipment
Ultra Thin Layer Transfer	Substrate MOS Driver substrate	BondScale
NanoCleave	Alternative to Thinning and wet oxide etching	850DB
Adhesive bonding	EPI transfer + LED transfer	5XX 850 Gemini
Laser Lift Off	EPI substrate removal	850DB
Metal Bonding	Substrate MOS Driver substrate	5XX Gemini

Smart pixel process flow is more complicated and can require additional aligned bonding.

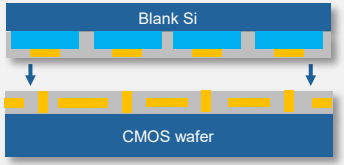
µLED | Micro Display

1. **LED wafer reconstitution, planarization, patterning.**

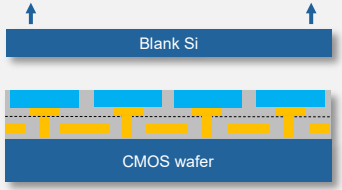


2. **Reconstituted wafer planarization and patterning.**

3. **Hybrid bond**



4. **Carrier removal, optics, color conversion**

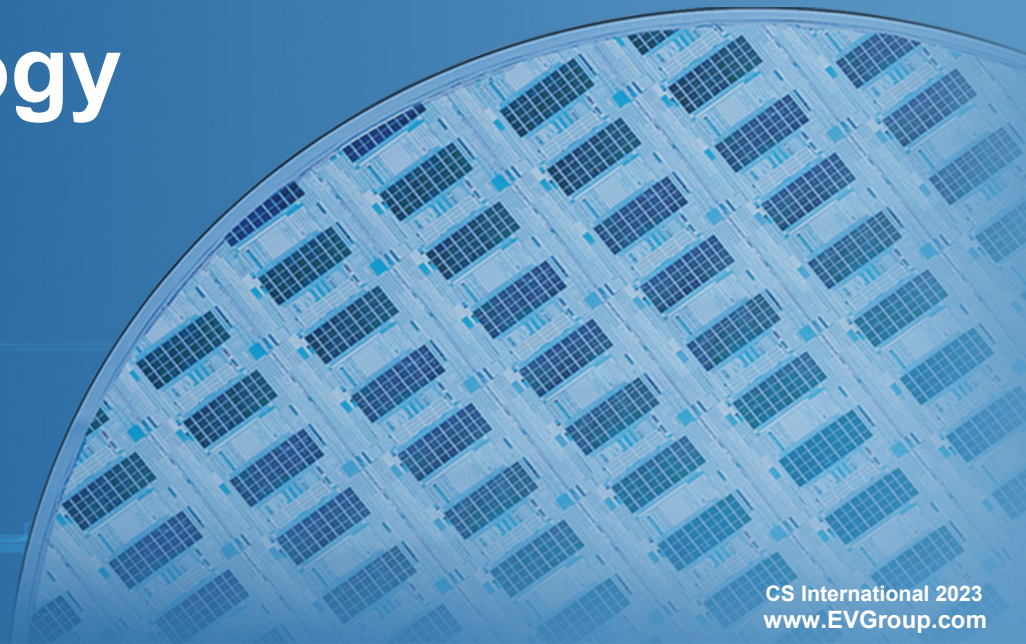


Next steps: color conversion/integration

EVG Technology	Application	Equipment
Laser Lift Off	EPI substrate removal	850DB
Wafer Reconstitution	Utilization of 300mm frontend semiconductor processing	320
Hybrid bonding	Fine pitch bond of the µLED EPI wafer to the CMOS driver wafer	GEMINI FB
NIL	Optics formation	7XXX
Spin & Spray coating	Color conversion layer deposition	1XX

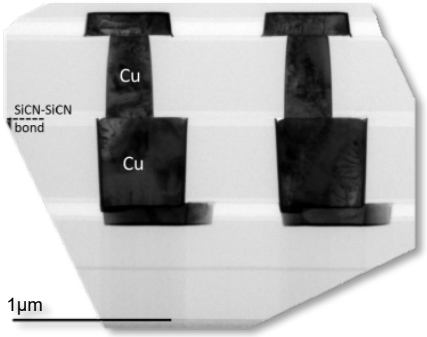
µDisplay manufacturing requires high precision alignment bonding to fulfill the fine pixel Pitch requirements.

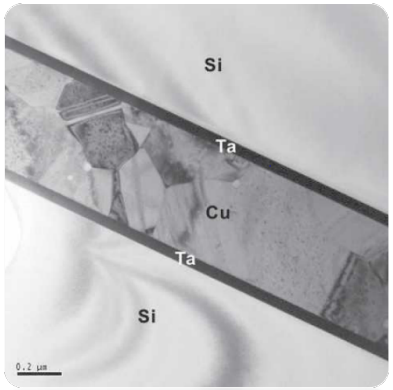
Bonding Technology Demonstrators

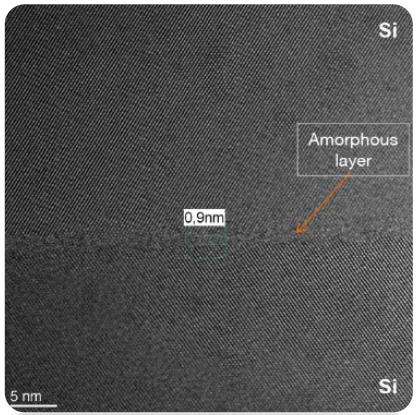


EVG Wafer Bonding Technology | µLEDs Integration Pitch

		Pitch
No Interlayer	Anodic	
	Fusion	2 µm
	Hybrid	2 µm
Metal Interlayer	Thermo-compression	5 µm
	Solder-based Eutectic/TLP	30 µm
Insulating Interlayer	Adhesive	30 µm
	Glass frit	

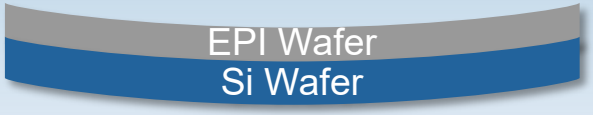




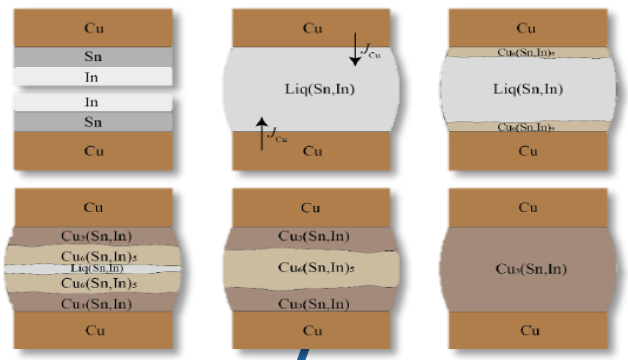


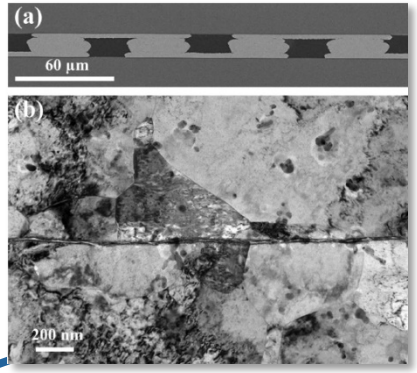
Metal Interlayer Bonding | Challenges, Knowledge and Expertise

CTE Mismatch



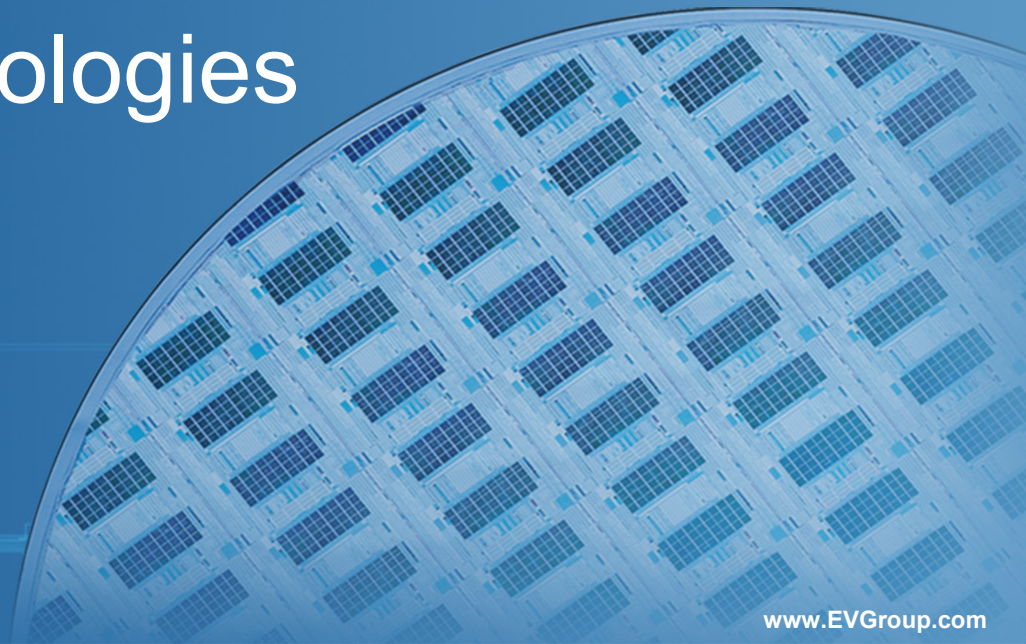
➔ Bonding T has to be minimized.





	AuIn	CuIn	AuInSn	CuInSn	CuCu	CuCu	TiTi	SiSi
Bonding Temperature	180°C	180°C	150°C	150°C	180°C 200°C	RT	RT	RT
Remelt Temperature	450°C	450°C	>350°C	>350°C	NA	NA	NA	NA
Bonding Process	TLP	TLP	TLP	TLP	TC	Com Bond	Com Bond	Com Bond

EVG Unique Technologies



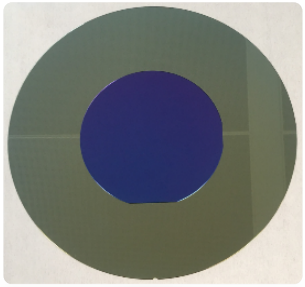
Heterogenous Wafers Bonding I Different Substrate Dimension

Bonding of wafers of different size enables seamless integration of EPI and CMOS wafers

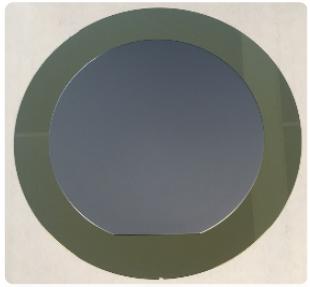
Smart View NT2 3δ < 150nm*

Smart View NT3 3δ < 150nm*

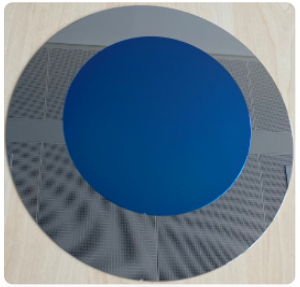
100 mm GaAs / GaN	150 mm GaAs / GaN	200 mm Si	300 mm Si



100 mm / 200 mm



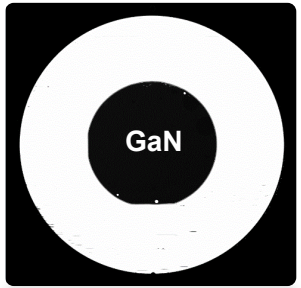
150 mm / 200 mm



200 mm / 300 mm

PVA TePla

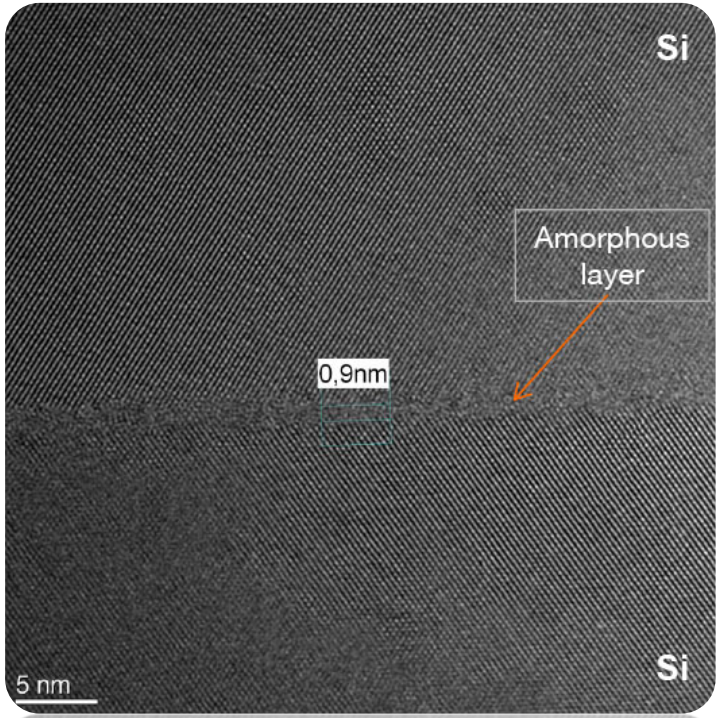
SAM Bonding area > 99%.



100 mm / 200 mm

150 mm / 200 mm

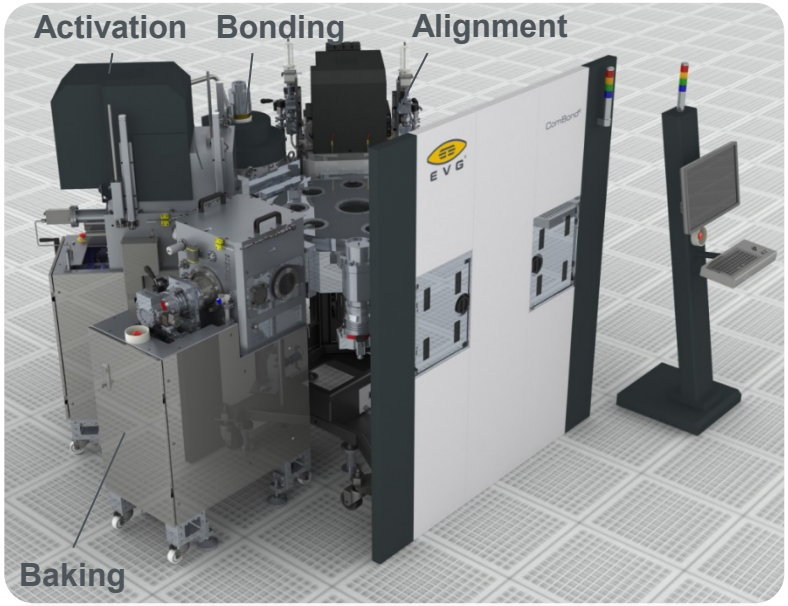
*LED applications



ComBond®

ComBond® | Unique high vacuum wafer bonding platform

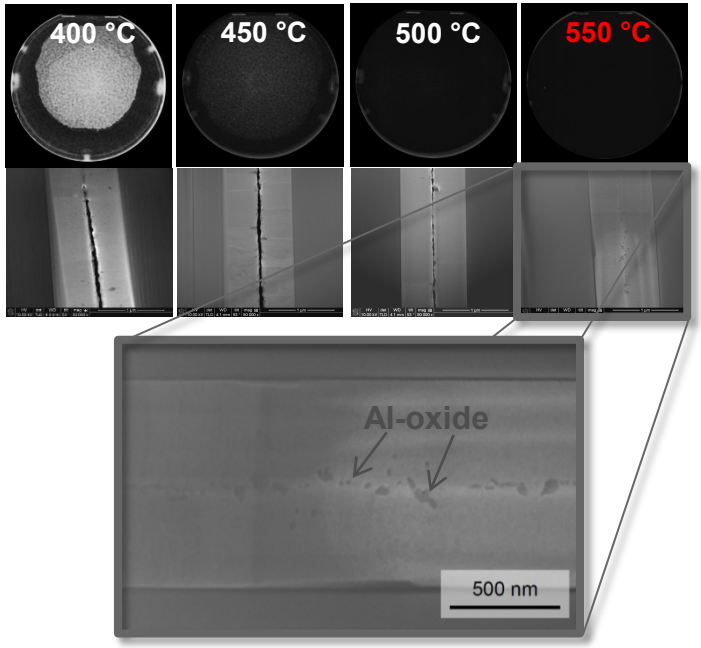
- Oxide-free metal bonding
- Optical alignment in high vacuum
- Great for the process development phase
- Enabling new products and devices



- Room temperature heterogenous integration
- High vacuum encapsulation for leading-edge MEMS devices

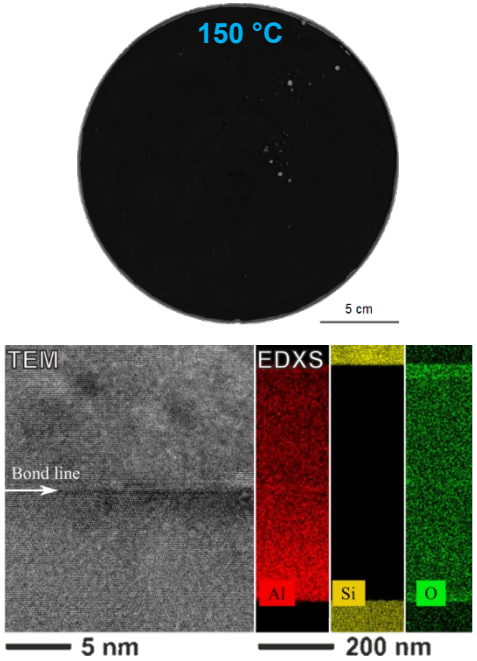
Oxide-Free Thermo-Compression Wafer Bonding

Conventional Bonder (EVG®520IS)



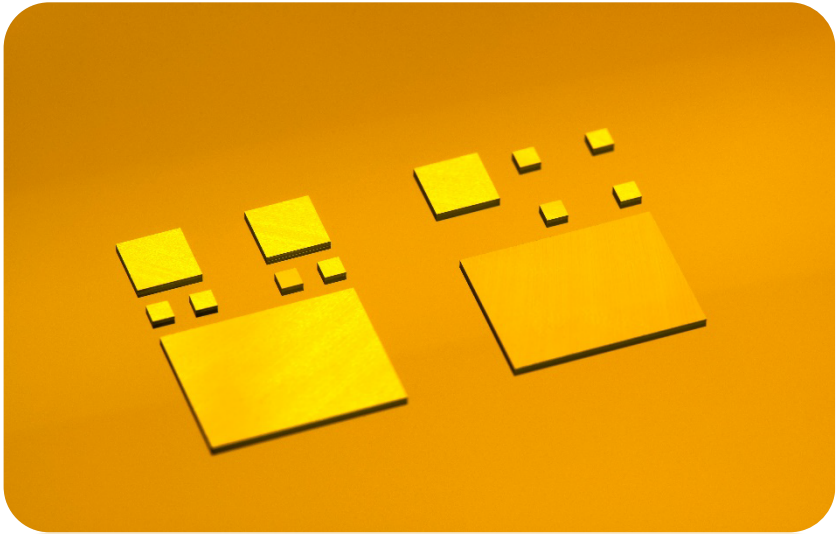
*Dragoi et al., Microsyst Technol, **18** (7-8), pp 1065–1075 (2012)*

EVG ComBond®



Hinterreiter et al., «Surface pretreated low-temperature aluminum–aluminum wafer bonding", Microsyst Technol, (2017)

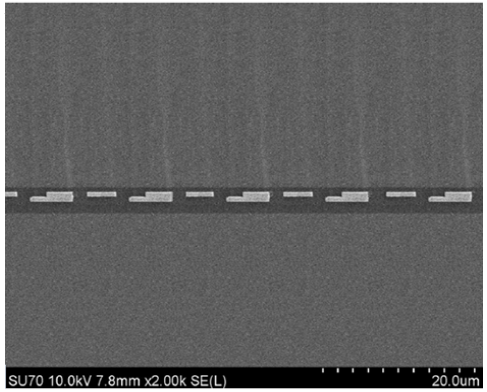
Bonding Materials	
Si (100)	Si (100)
	Sapphire
	GaN
	Ge
	$LiNbO_3$
	$LiTaO_3$
	Mo
	Si_xN_y
Si (111)	Si (100)
	Si (111)
$Si(SiO_2)$	Si
	$Si(SiO_2)$
SiC (4H)	Si
	SiC (4H)
	Poly-SiC
Poly-SiC	Poly-SiC
GaAs	InP
	Si
	SiC
Au	Au
Cu	Cu
Al	Al
Ti	Ti



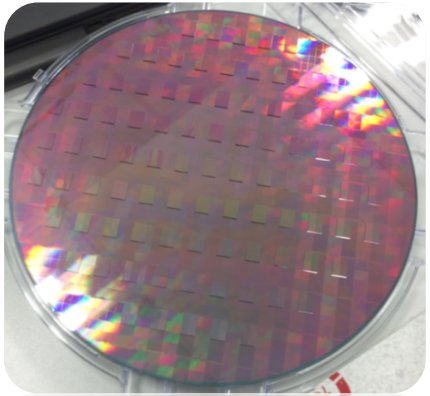
Die to Wafer Bonding

Co-D2W Bonding | Process Results – Hybrid Bonding

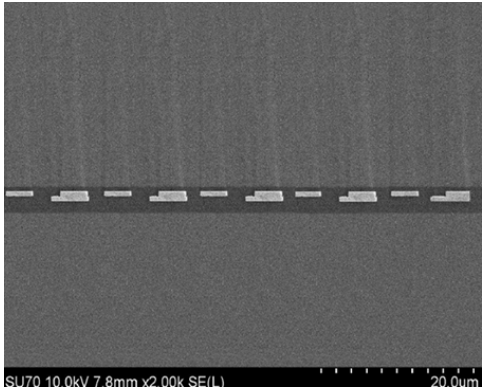
Edge Die

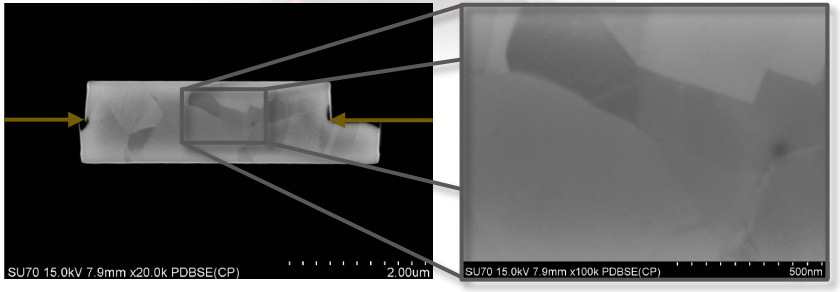


300mm 10x14 Dies

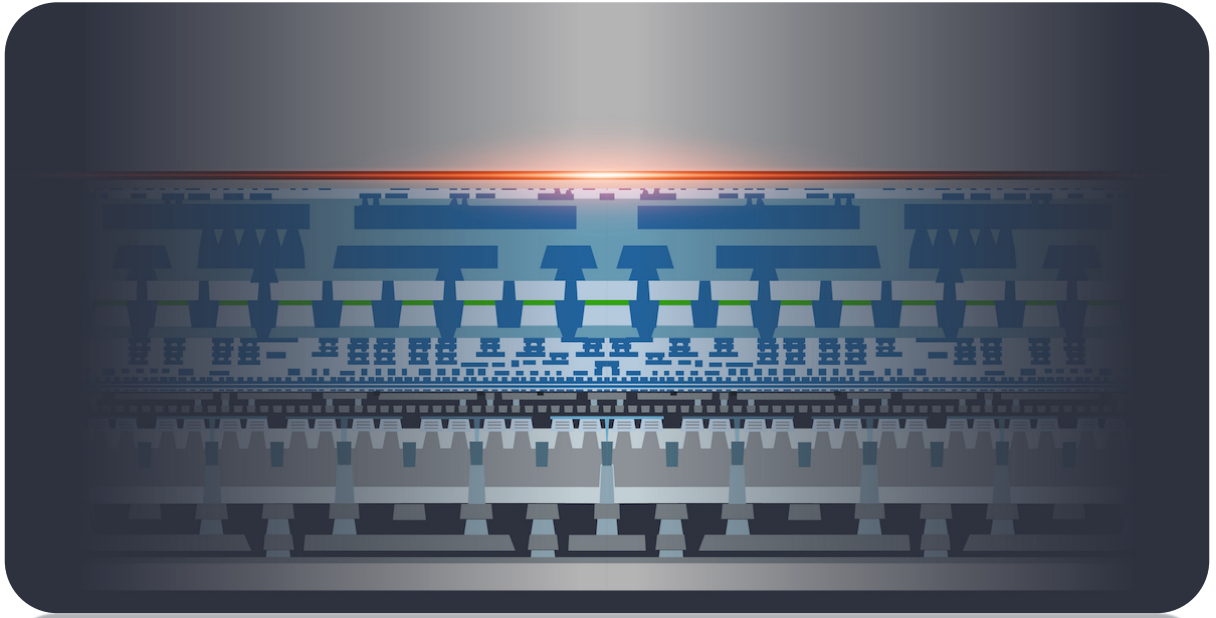


Center Die





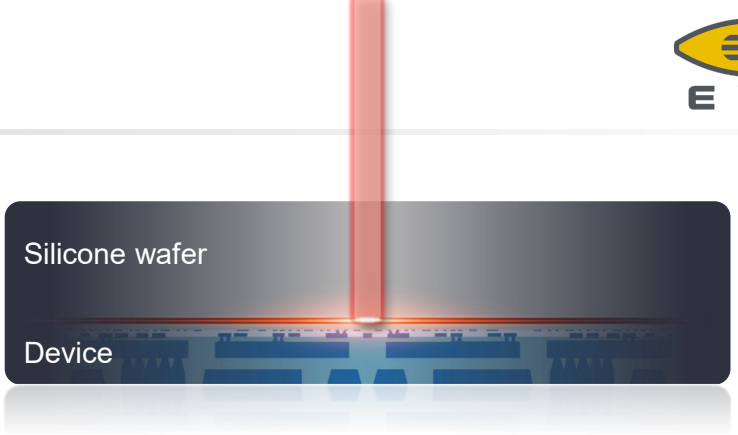
Excellent collective die to wafer bonding performance



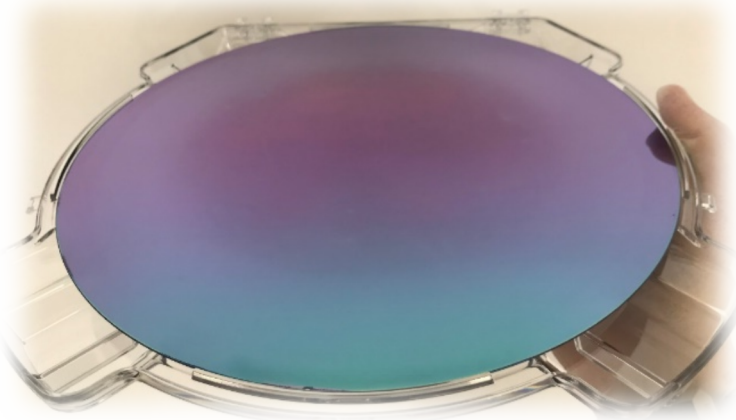
NanoCleave

NanoCleave

- Enables silicon wafers as temporary carriers
- Laser debonding through silicon
- Nanometer precision
- Ultrathin (<10µm) die and wafer processing

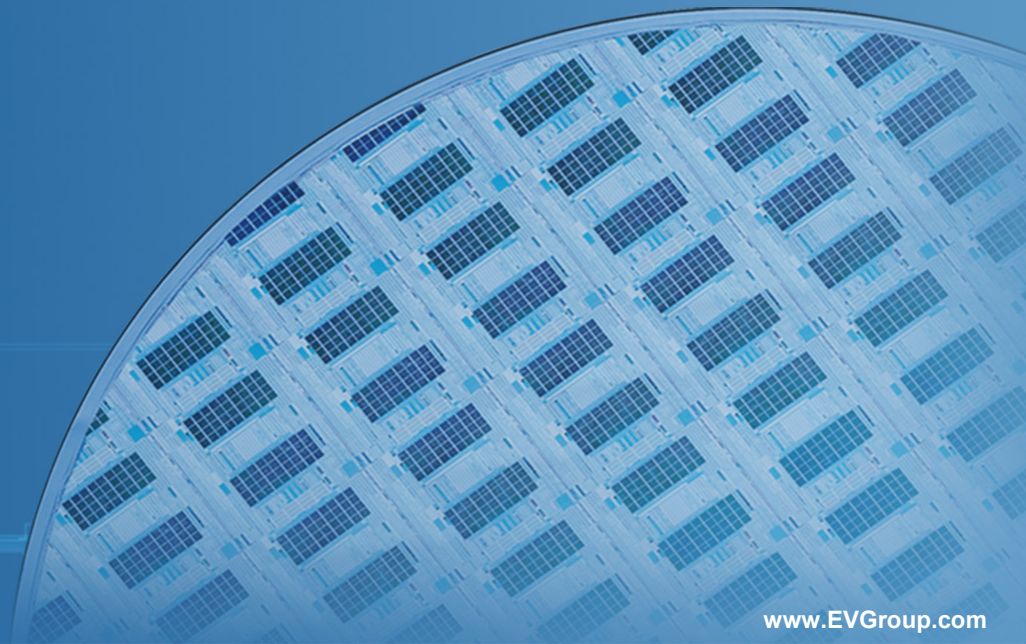


Carrier DB interface



Device DB interface

Conclusions



Conclusions

- 73% wafer bonding market share
- Broad equipment portfolio up to 300 mm
- Excellent process know-how established over decades
- Process development services
- State-of-the-art application labs and cleanroom facilities

Thank you!