Tektronix®

Enabling Test Automation in Power Electronics Reliability

PE International Conference 2024

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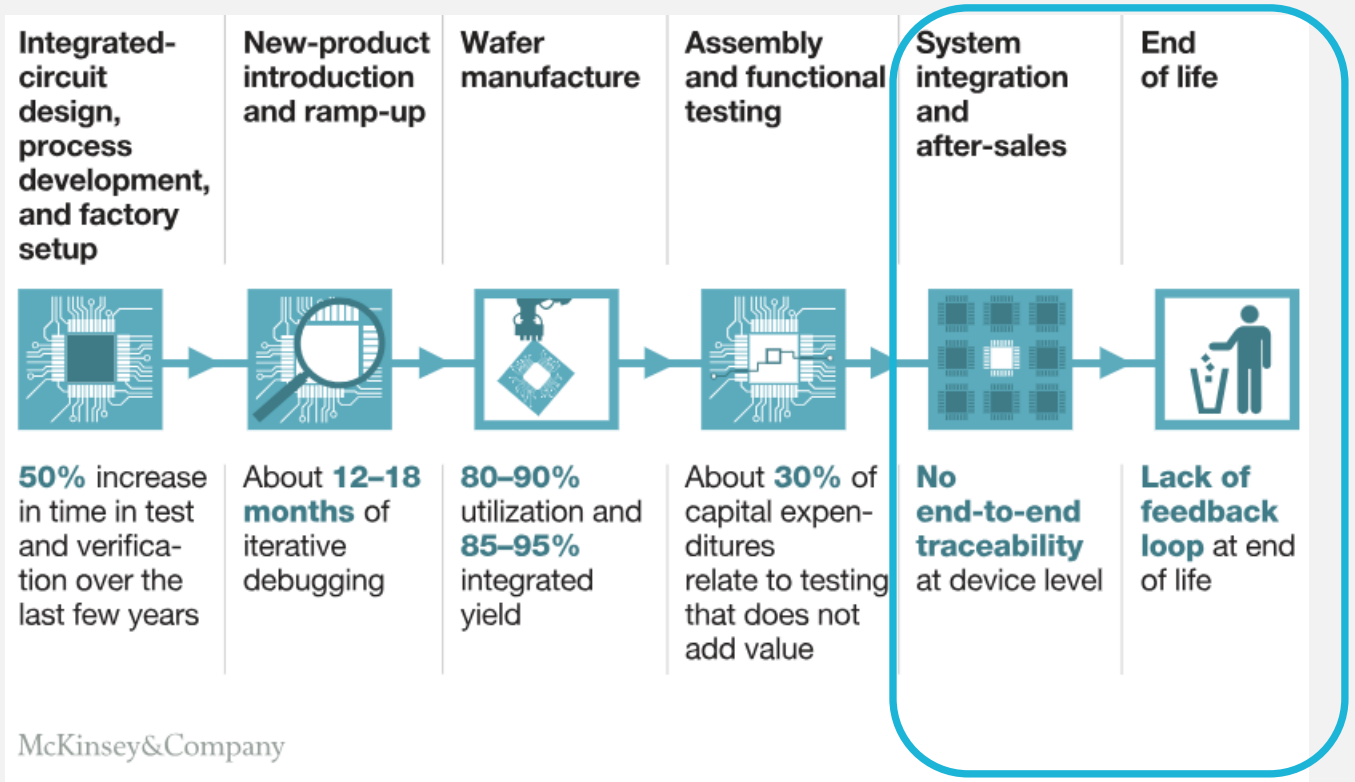
Terminology

*"The probability that an item will perform a required function **without failure** under stated conditions for a stated period of time."*

- **Advanced Analytics Integration** in Semi Manufacturing
- **NPI debugging** time reduction
- Trace a chip from design **through use**

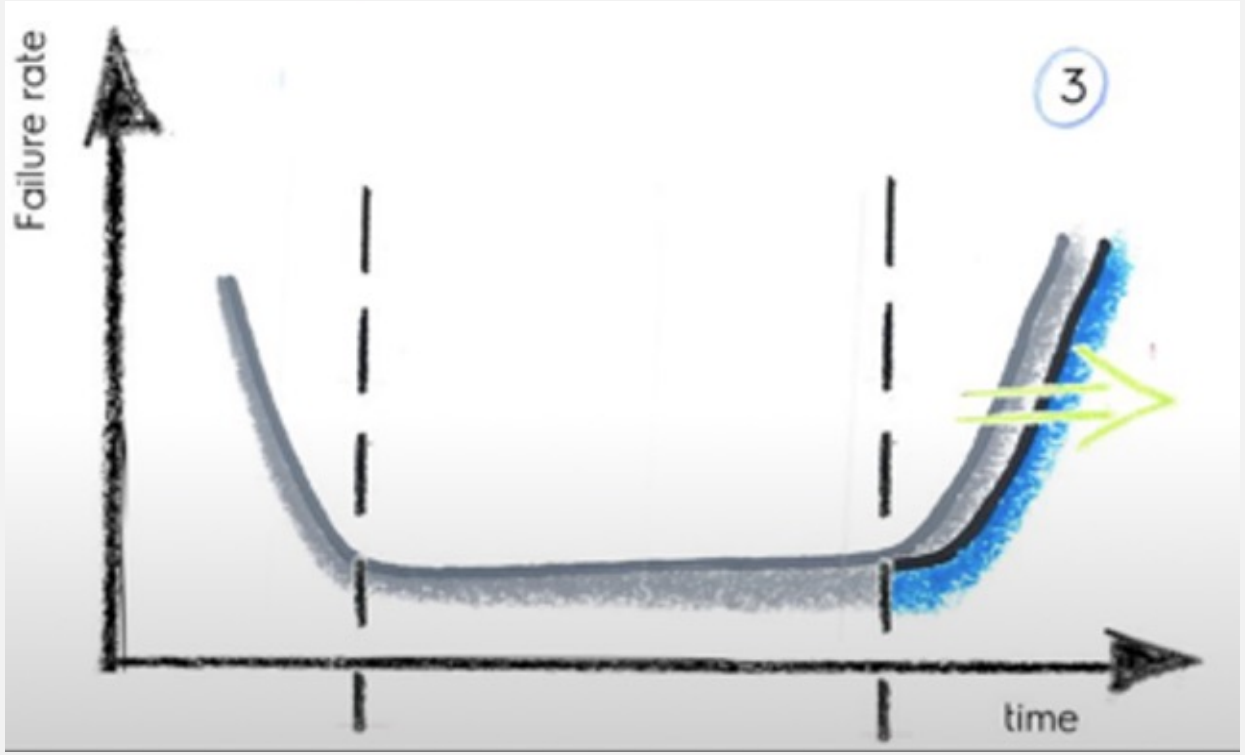
Product Development Phases



- R&D: material evaluation, process design
- Integration: Robust Process, High Quality
- Production

The Bathtub

- Quality
- Robustness
- Reliability

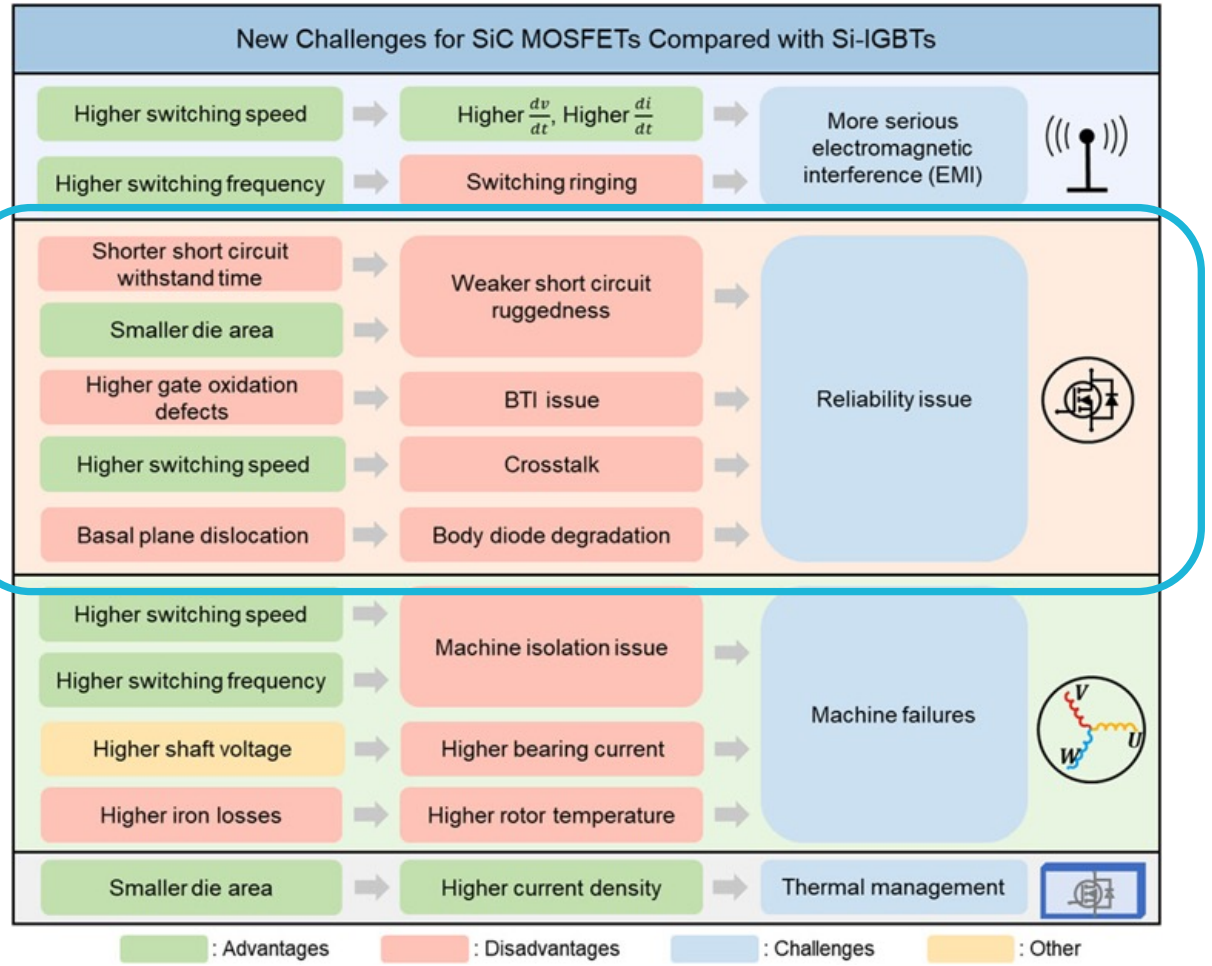


New Technologies, New Challenges

- Temperature distribution in the junction during Short Circuit Test
- Less robust as Si for longer short at high temp

- Gate oxidation, tunneling current flow
- NBTI: negative bias voltage instability

- In built body diode in SiC, but…
- Crystal growth BPDs cause degrad.



IET Power Electronics, Volume: 16, Issue: 12, Pages: 2103-2120, First published: 17 May 2023, DOI: (10.1049/pel2.12524)

Meeting Application related Standards

JEDEC
Global Standards for the Microelectronics Industry

STANDARDS & DOCUMENTS | COMMITTEES | NEWS | EVENTS & MEETINGS | JO

Standards & Documents Search

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Title	Document #	Date
RELIABILITY QUALIFICATION OF SEMICONDUCTOR DEVICES BASED ON PHYSICS OF FAILURE RISK AND OPPORTUNITY ASSESSMENT Status: Reaffirmed September 2019	JEP148B	Jan 2014
A concept is outlined, which proactively integrates qualification into the development process and		

Accelerated Stress Test	Industry Standard / NXP Mission Profile / Use Life	JESD47 / Commercial, Home and Industrial / 5-10 years	AEC Q100 Grade 1 / A1 / 15 years
High-Temperature Operating Life Test (HTOL)	JESD22-A108	1000h / 2000h 1) Tj=150 °C	1000h / 2000h Tj=150 °C
Preconditioning (PC)	J-STD-020	Performed prior to THB, HAST, T/C and AC	
Temperature Cycling (TC)	JESD22-A104	500c / 1000c -65°C - 150 °C	500c / 1000c -65°C - 150 °C
Highly Accelerated Stress Testing (HAST)	JESD22-A110	96h / 192h 85%RH / 130 °C	96h / 192h 85%RH / 130 °C
Temp and Humidity Bias (THB)	JESD22-A101	1000h / 2000h 85%RH / 85 °C	1000h / 2000h 85%RH / 85 °C
High Temperature Storage Life (HTSL)	JESD22-A103	1000h / 2000h Ta=150 °C	1000h / 2000h Ta=150 °C
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001-2012	2kV / 2.5kV	2kV / 2.5kV
Charged Device Model (CDM)	JESD22-C101	500V / 750V	500V (corner 750V) / 750V
Latch-Up (LU)	JESD78	± 100 mA - Ta, max / ± 100 mA - Tj, max	± 100 mA - Ta, max / ± 100 mA - Tj, max

From NXP website: Product Qualification | NXP Semiconductors

How Infineon controls and assures the reliability of SiC based power semiconductors

depth with an emphasis on the differences with respect to Si technology. In Si MOSFETs Infineon has acquired in the past a solid understanding of BTI and has substantially contributed to scientific progress in collaboration with renowned university partners [13] [14] [15]. The acquired know-how on the degradation physics and electrical measurement techniques has now been transferred to Infineon SiC devices [16] [17]. Indeed, many similarities regarding DC BTI exist in Si and SiC technologies despite the different material properties [18]. However, a few aspects are different and have to be considered in order to correctly measure and assess application relevant parameter variations.

4.1.2 Measuring DC BTI in SiC power devices

Threshold voltage variations caused by DC BTI consist of two components: one fast, recoverable component and one quasi-permanent (very slow recovery) component [19] [20]. The quasi-permanent component determines the long-term drift of a device whereas the fast component recovers in the short term.

In order to obtain comparable drift values, industrial standards on the determination of BTI drift have been developed, such as e.g. JESD22 [21] and its extension AEC-Q101 [22]. These standards were based on Si technology and need to be refined for SiC technology as will be outlined below.

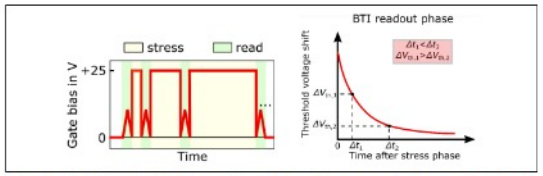


Figure 6 Typical DC BTI MSM (Measure-Stress-Measure) sequence using the example of a PBTI (Pulsed BTI) stress. On the left side, the measurement signal over time is displayed. The right hand side shows the time dependent recovery of the threshold voltage drift, illustrating the influence of readout delays on the extracted threshold voltage shift. Even small differences in readout timing may lead to large variations of the extracted threshold voltage drift.

Texas Instruments
www.ti.com
Addressing GaN Failure Mechanisms

3 Addressing GaN Failure Mechanisms

Failure mechanisms are present in all devices. Reliability engineering consists of making devices robust to failure mechanisms and their resulting failure modes. For GaN devices, the major failure modes are the *increase of leakage currents* and *changes in parameters* such as on-resistance. These can result in a reduction in efficiency or in circuit malfunction. Hard-failure can also occur.

In GaN devices, the primary failure mechanisms are *Time Dependent Breakdown (TDB)*, *hot-carrier degradation*, *and charge trapping*. Time Dependent Breakdown is a well-known phenomenon[13] in dielectrics used in silicon processing, and its modeling is treated in JEDEC publications[14]. It occurs due to high electric-field and is responsible for increased leakage currents and can lead to hard-failure. Hot-carrier degradation is also well-known in Si MOSFETs, where hot-carrier stress causes defect generation. Hot-carriers are created by hard-switching in power FETs, and have been seen to result in both charge trapping and wearout in GaN FETs[5, 15].

GaN FETs operate with high electric fields in several regions, as shown in Figure 3-1. TI GaN FETs have been engineered for TDB lifetime with the use of special test structures for each of these high-field regions. A model has been built incorporating 1.8 million device hours of testing and shows a low FIT rate of 0.8 FIT with 10 years of continuous application of 480 V and 125°C for the LMG3410R070 product.

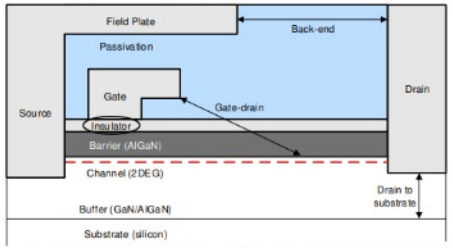
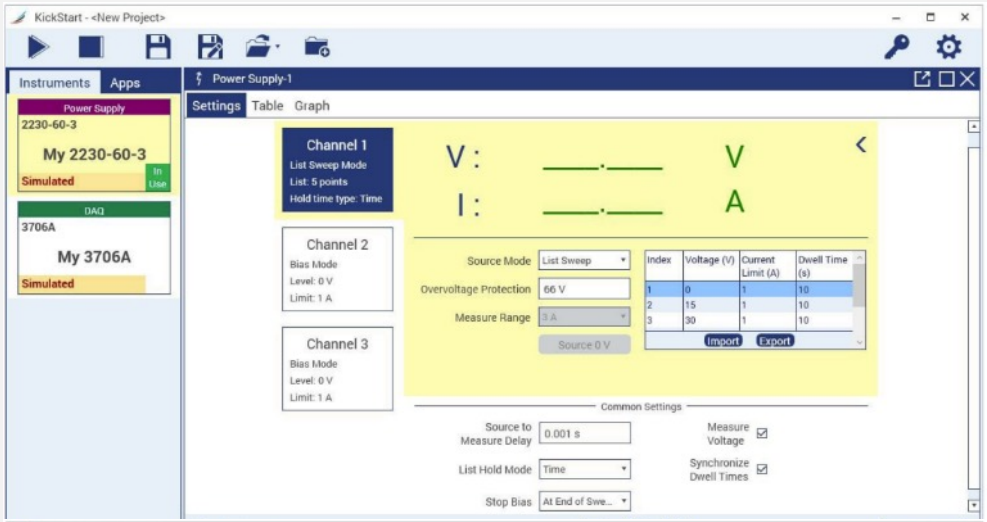


Figure 3-1. Schematic cross-section of the GaN device showing the high-field regions in the device.

Asks to T&M Suppliers

- Technology required sourcing ranges and measurements precision
- Modularity and flexibility (sequential and parallel test support)
- High Channel Density
- Instrument Reliability, Planned Calibration
- Test Criteria, protocol standard integration
- Accurate Failure mode execution
- Environmental Test Seamless Integration
- Probe Station Seamless Integration
- **Open Programming & Automation Support**

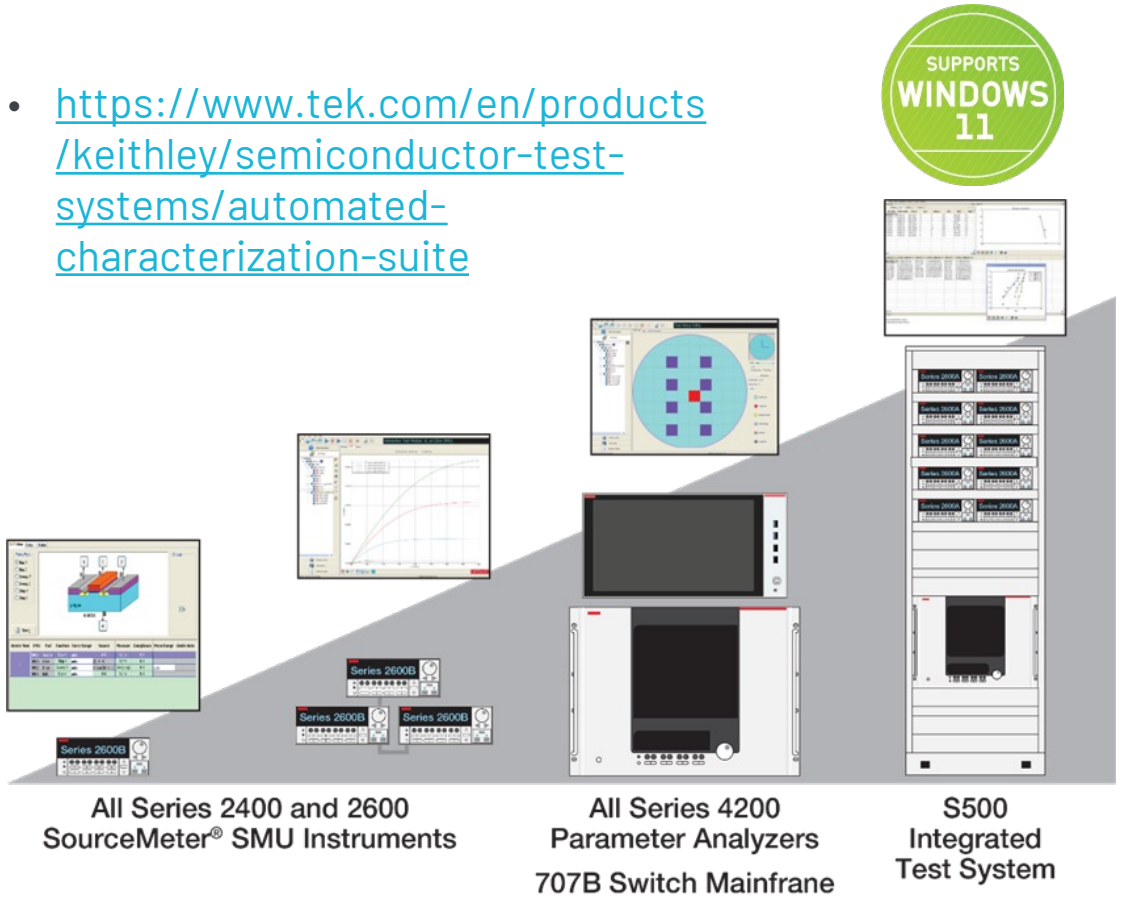
Packaged Device Scenario

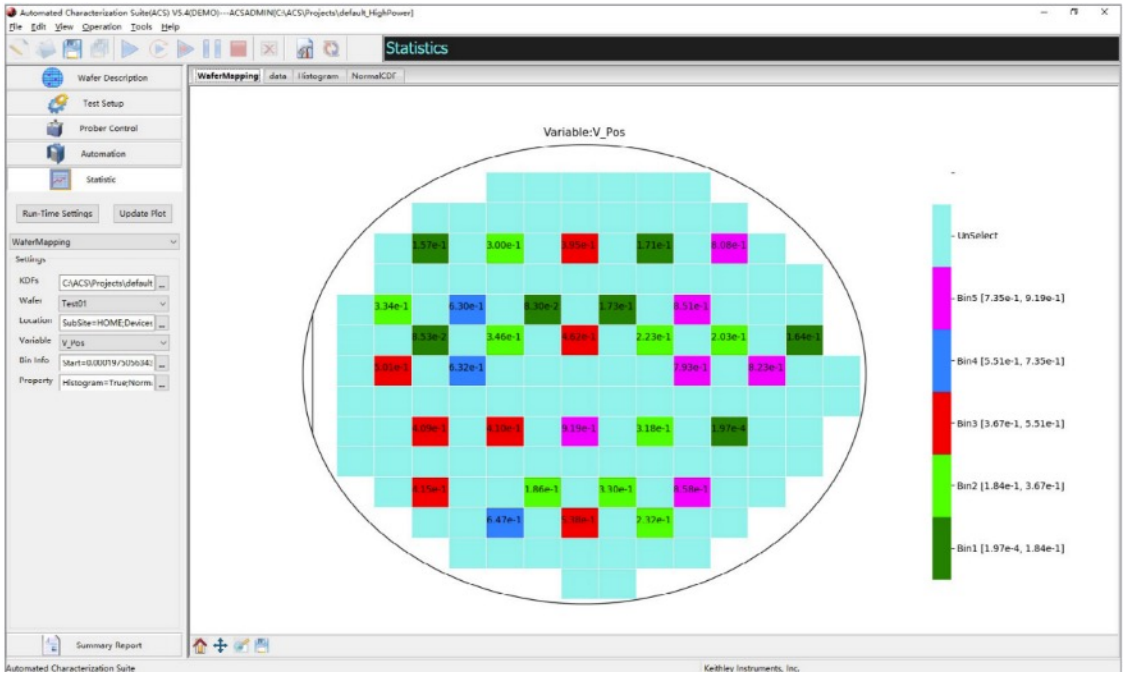


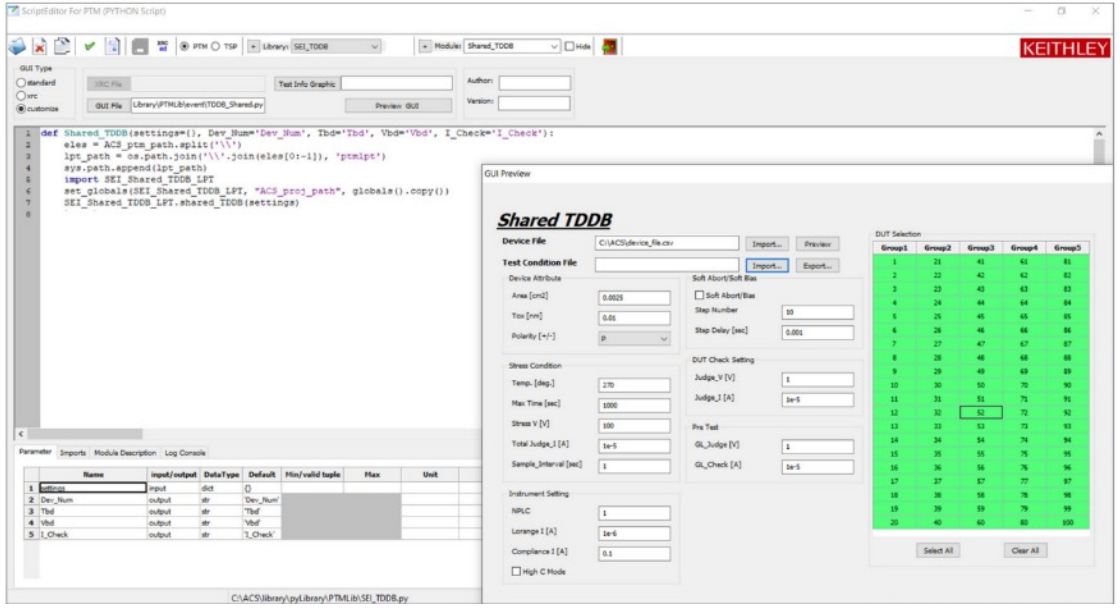
Wafer Level Scenario

- Advanced Characterization Suite (ACS)

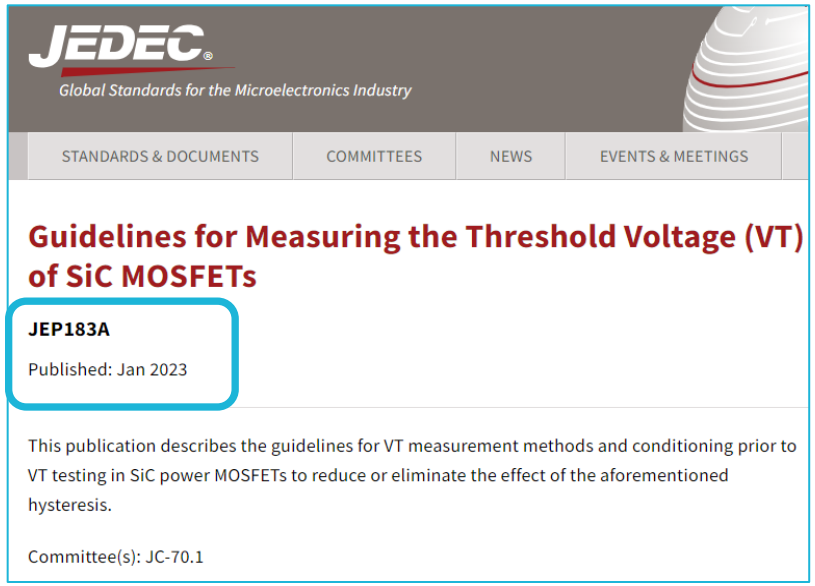
- https://www.tek.com/en/products/keithley/semiconductor-test-systems/automated-characterization-suite







A Typical SiC MOSFETs Reliability Issue

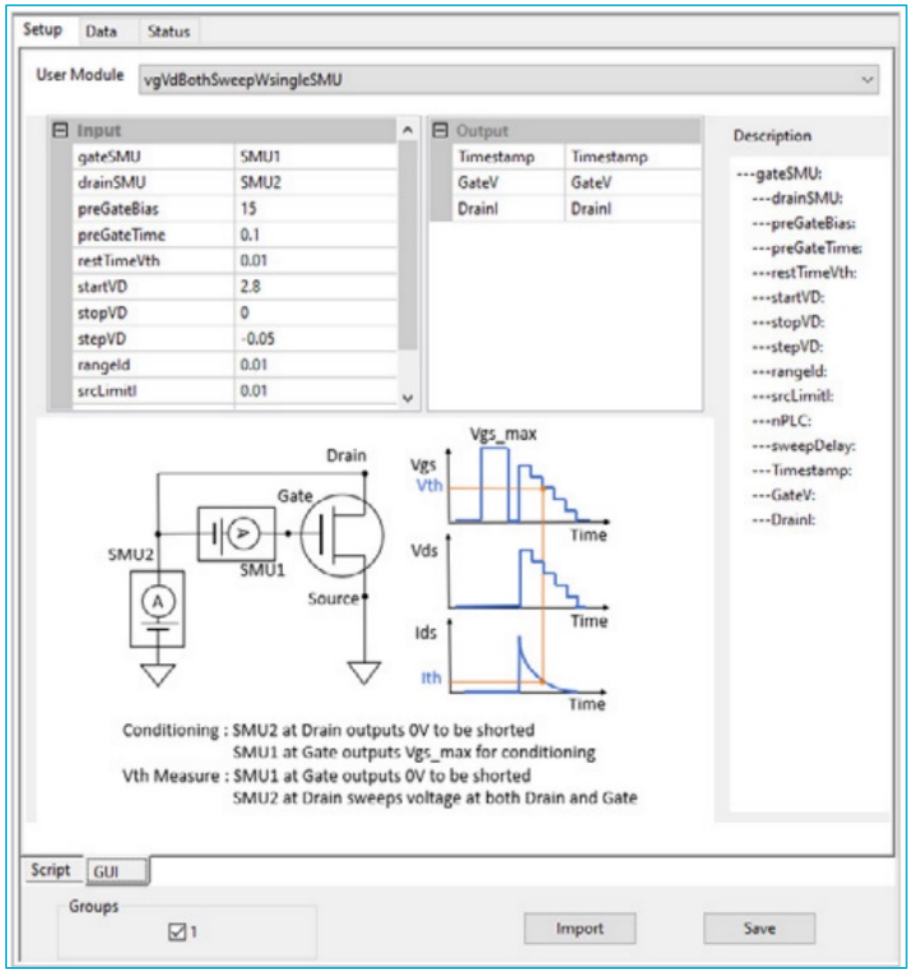



```
For sweeping gate voltage and fixing drain voltage
* newVTH = newVthSiC_JEP183()
* newVTH.vgSweepVdFixed(15,100e-3,10e-3,2.8,0, -0.05,2.5,1e-3, 0.1, 0.5, 0.002)

For sweeping both gate voltage and drain voltage
* newVTH = newVthSiC_JEP183()
* newVTH.vgVdBothSweep(15, 100e-3, 10e-3, 2.8, 0, -0.05, 10e-3, 7e-3, 0.1, 0.002)

For sweeping both gate voltage and drain voltage with single SMU
* newVTH = newVthSiC_JEP183()
* newVTH.vgVdBothSweepWsingleSMU(15, 100e-3, 10e-3, 2.8, 0, -0.05, 10e-3, 7e-3, 0.1,0.002)

For fixing both gate current and drain current
* newVTH = newVthSiC_JEP183()
* newVTH.vgVdBothFixedBias(-4, 100e-3, 10e-3, 5e-3, 20, 5, 1, 50e-3)
```



Summary

- **Automation of Testing in Reliability is fundamental** for Optimization and Enablement of Advanced Analytics
- **Prerequisites are : Fast Interconnection** Links, **Test Scripting** facilitation, **Modular** and **Reliable** sourcing and measurment, high **Channel Density**
- **Standard Integration and Specific Use Cases Support**
- **Field** Experience validation

Thanks

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