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ANGELTECH

PE INTERNATIONAL CONFERENCE

18TH-19TH APRIL 2023, BRUSSELS, BELGIUM

SmartSiC™ from Soitec a greener, faster and better technology for SiC

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April 2023

SOITEC AT A GLANCE

Business Outlook
- **FY23 ~ $1.2B**
- **FY26: > $2.1B**

FY22 R&D
11% of revenue

Investments
- **FY22-26: €1.1B**

1rst | **Largest manufacturer of Engineered Substrates**

2 | **Unique technologies** SMART CUT™, SmartSiC™

2,200 | **Employees Worldwide** GLOBAL PRESENCE

GLOBAL INDUSTRIAL FOOTPRINT

INVESTMENT IN CAPACITY EXPANSION ACROSS ALL PRODUCT LINES

Country	Soitec Fab	Product	Diameter	Max capacity (wafers per year)
FRANCE	BERNIN 1	SOI	200mm	~1Mwpy
	BERNIN 2	SOI	300mm	~700Kwpy
	BERNIN 3	POI	150mm / 200mm	Raising capacity to reach ~750Kwpy
	BERNIN 4 NEW	SiC SOI refresh	150mm / 200mm / 300mm	Building capacity to reach ~500Kwpy
SINGAPORE	PASIR RIS	SOI	300mm	Raising capacity to reach ~1Mwpy
	PASIR RIS EXTENSION NEW	SOI	300mm	Expanding capacity to reach ~1Mwpy (production starting by end FY25)
BELGIUM	HASSELT	GaN	150mm / 200m	Raising capacity to reach ~60Kwpy
CHINA	SIMGUI	SOI	200mm	~450Kwpy

Bernin, France*

Pasir Ris, Singapore*

(*) For illustrative purposes only

30 YEARS TO BUILD A UNIQUE POSITION IN THE SEMICONDUCTOR INDUSTRY

STRATEGIC PARTNERSHIPS IN THE ENTIRE SEMICONDUCTOR ECOSYSTEM TO SERVE 3 END-MARKETS

BULK MATERIALS

Strategic Agreement w/ our Suppliers

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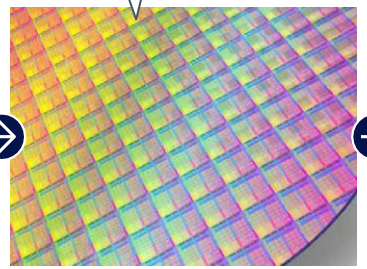
LEADING SUPPLIER

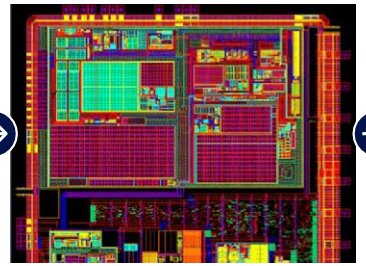
ENGINEERED SUBSTRATES

>2 Mwpy

Joint Development Agreements



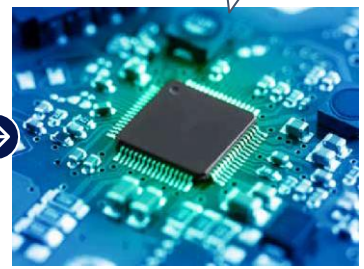
FABS / IDM



DESIGN

Design Capabilities to support Design Development on our Engineered Substrates

Technology engagement with Fabless and IDM



FABLESS / IDM

END MARKETS

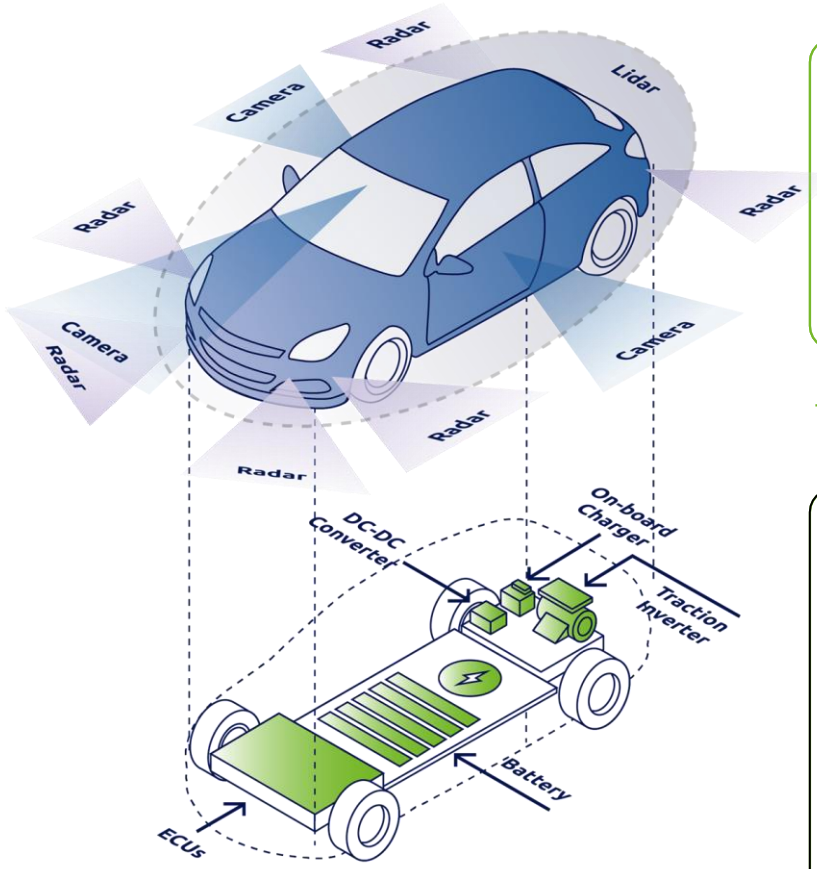
MOBILE COMMUNICATIONS

AUTOMOTIVE & INDUSTRIAL

SMART DEVICES

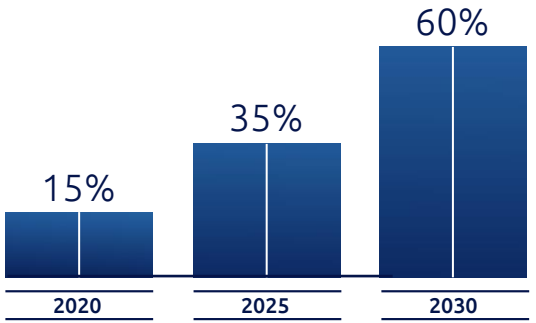
AUTOMOTIVE MEGATRENDS

DRIVE INNOVATION FROM SUBSTRATES TO SYSTEMS

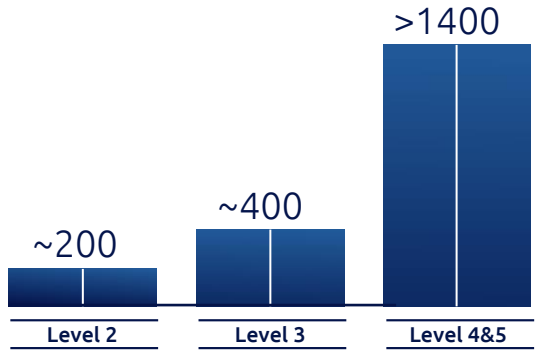


DIGITALISATION

- Fusion processor
- Radar processor
- Image sensor
- Domain controller



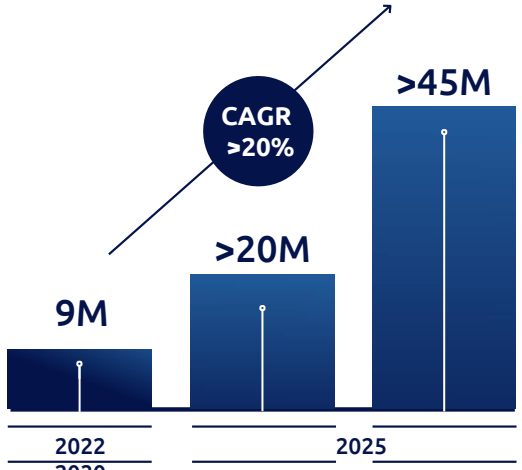
Autonomous cars level 2 & above (%)



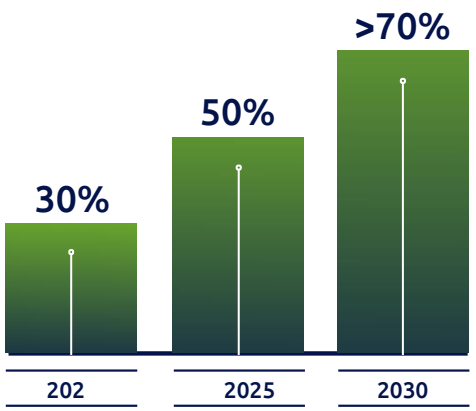
ADAS semiconductor content ($)

ELECTRIFICATION

- SiC Diode
- SiC MOSFET
- PMIC
- BMS
- Gate drivers
- Smart actuator



Global EV sales (units)



SiC BASED EV POWERTRAIN (%)

Source: Soitec estimates, Infineon, NXP, IHS, The International Council on Clean Transportation (ICCT) 2020, LMC, IEA 2021, Exawatt, Yol

POWERTRAIN – A HIGHLY CRITICAL SYSTEM FOR THE EV MARKET

SiC GENERATES VALUE AT SYSTEM LEVEL AND ENABLES COST REDUCTION

POWERTRAIN COST: ~10,000$

Electric motor
- Electric motors
- e-transmission

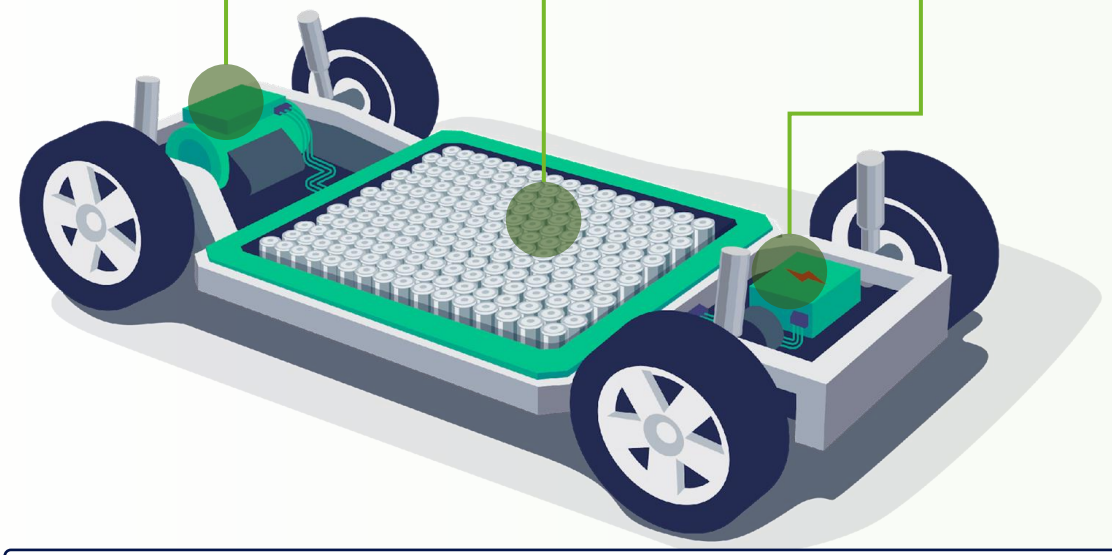
~1,100$

Battery pack & modules
- Battery pack
- Modules and cells
- BMS

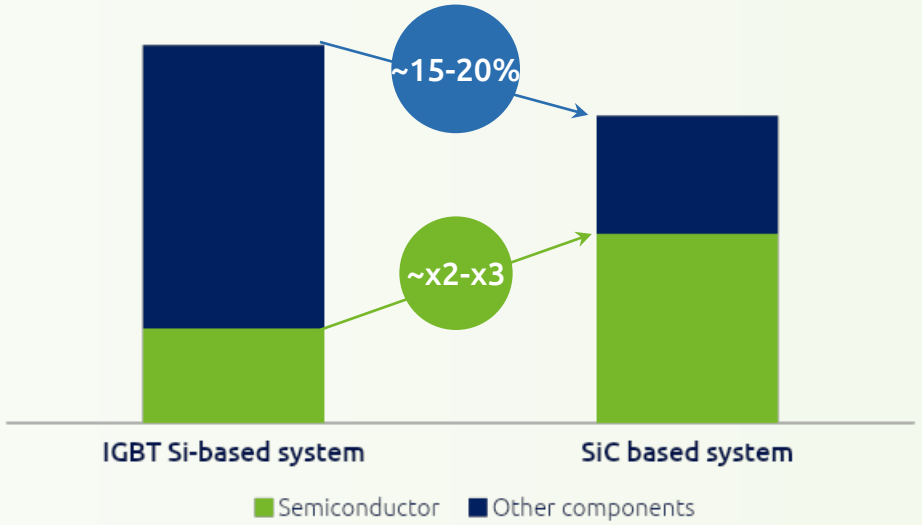
~8,000$

Power electronics
- E-drive / inverter (DC/AC)
- DC/DC Converter
- On-board charger (AC/DC)

~1,500$



TOTAL SYSTEM COST – UP TO 20% REDUCTION

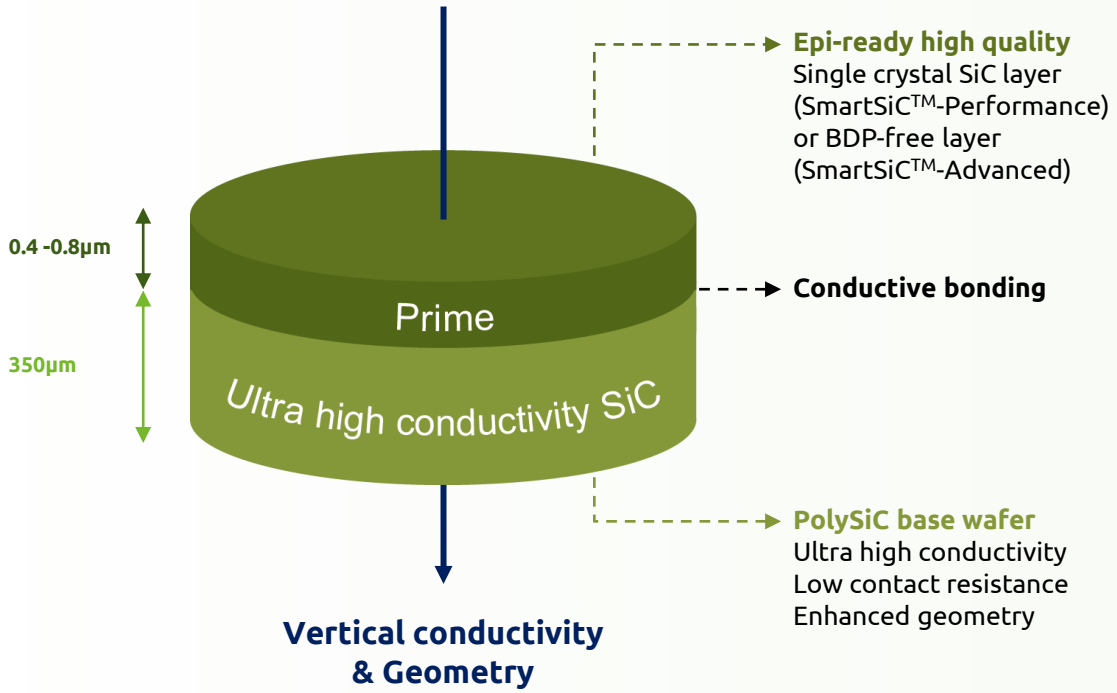


Shorter charge time 800V	**~50% faster**
Increase battery range	**5% – 10% more range**
Reduce system / battery costs	**$500 – $1,000 savings**

HOWEVER A MORE PERFORMANT AND HIGHER ADDED VALUE SiC SUBSTRATE IS NEEDED

SmartSiC™ ENGINEERED SUBSTRATE

UNRIVALLED VALUE PROPOSITION TO ENABLE GREENER, FASTER & BETTER SiC ADOPTION



UNRIVALLED VALUE PROPOSITION

SmartSiC™ vs. Bulk SiC:

- 40,000 Tons of CO_2 reduction for every 1 million wafers vs. standard SiC
- 200mm scalability to accelerate SiC adoption through 10x re-usability
- Enabling new generations of SiC devices thanks to an improvement of RDS_{ON} of up to ~16%
- Reducing Capex & Opex for device manufacturers

>10x

mono-SiC wafer re-usability

~8x

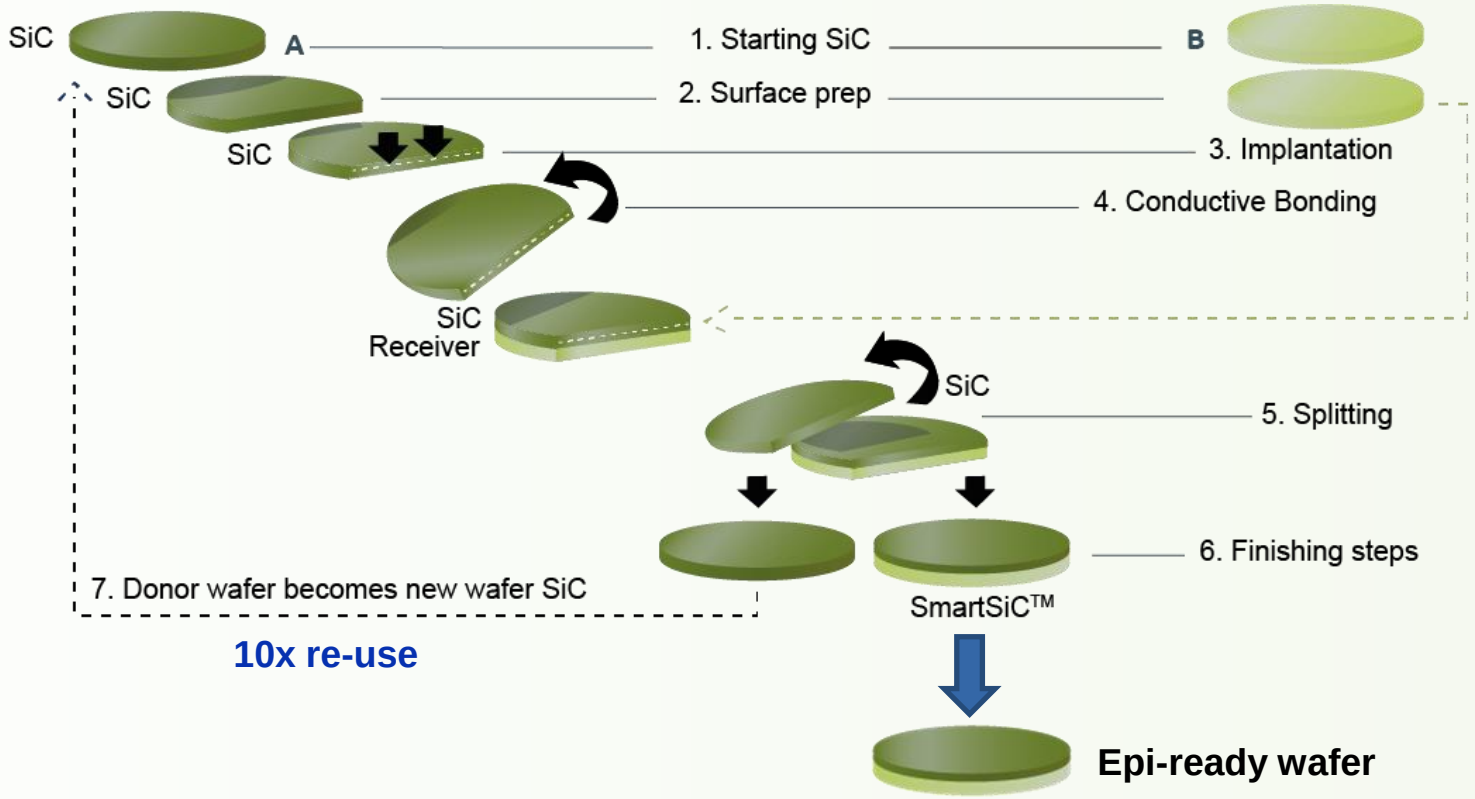
higher substrate conductivity

SmartSiC™, THE PROVEN SMART CUT™ PROCESS ADAPTED TO SiC

HIGH VOLUME MANUFACTURING EXPERTISE OF >2M WAFERS PER YEAR

Single-crystal SiC donor wafer
(Prime crystal quality)

polySiC handle wafer
(Ultra high conductivity SiC)



SmartSiC™, THE FASTEST PATH TOWARDS 200mm DEPLOYMENT

DISRUPTIVE ACCELERATION FACTOR

SmartSiC™ ENABLES HIGHER PRODUCTIVITY

20%

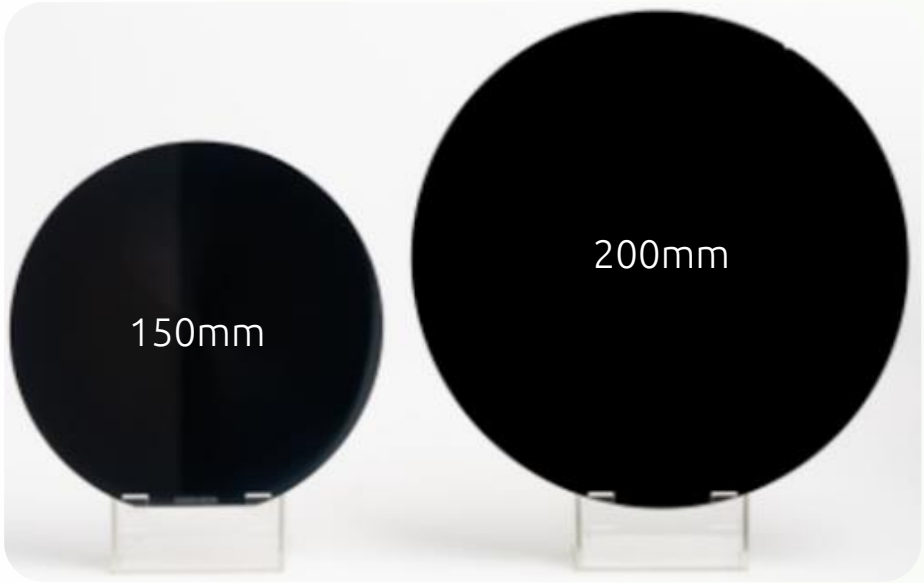
Smaller Die size

SmartSiC™ enabling more devices per wafer

x1.82

Higher usable area

200mm allowing improved manufacturability



200mm SmartSiC™ DIFFERENTIATION

200mm further adds to 150mm SmartSiC™ performance improvements

Higher **yield**

Better **efficiency** of Smart Cut™ process

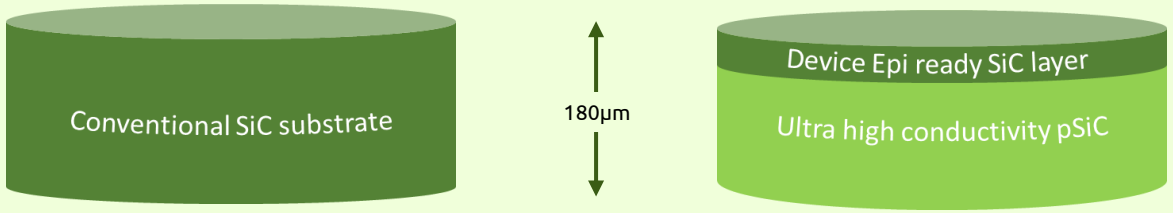
Faster **scalability** in 200mm

Lower **cost of ownership**

SmartSiC™, THE ENABLER FOR BETTER DEVICE PERFORMANCE

REDUCED RESISTIVITY BRINGS IMPROVED CURRENT DENSITY

LOWER SUBSTRATE R_{ON}.A



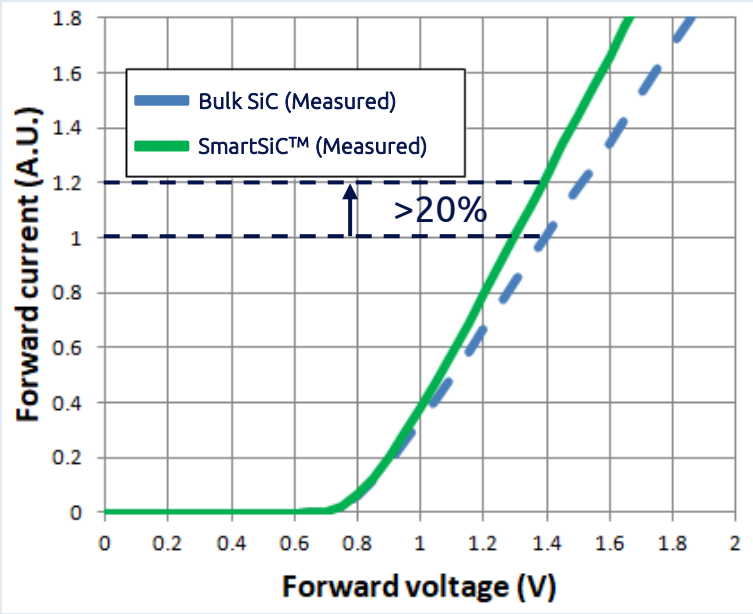
Standard SiC substrate | **SmartSiC™ substrate**

mSiC 20mΩ.cm	Substrate →	pSiC **2.5mΩ.cm**	Interface **10µΩ.cm²**
100 µΩ.cm²	BS metal contact →	**5µΩ.cm²**	
460µΩ.cm²	Total R_{Subs}.A →	**60µΩ.cm²**	

SmartSiC™ reduces the substrate contribution by 8x

A NEW PARADIGM FOR DEVICE PERFORMANCE

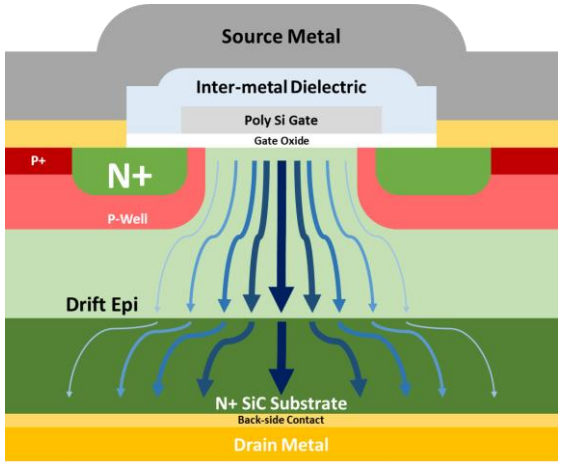
Proven higher current density



Enabling higher power density and reliability

SmartSiC™, SUBSTRATE GAINS EQUIVALENT TO A GENERATION DEVICE

LOWER RESISTIVITY MAKES SUBSTRATE CONTRIBUTION CORNERSTONE



8x higher substrate conductivity

+

Better current spreading

+

10x lower resistivity of back-side contact

=

Device manufacturer	A	B	C
Release year	**2022**	**2022**	**2022**
MOSFET technology	Planar	Trench	Trench
Ron.A* (mΩ.cm²) @ 25°C	2.7	2.5	2.5
Die thickness* (µm)	180	150	110
Total Ron.A gain vs mSiC	**16.2%**	**15.2%**	**12.1%**

*** Based on publicly available information**

SmartSiC™, TOWARDS HVM READINESS

SmartSiC™ READY TO RAMP-UP FOR EV's INVERTERS

FROM 10 KWPY PILOT LINE TO 500 KWPY HVM LINE

2022 | Q1-23 | Q2-23 | Q3-23 | Q4-23 | Q1-24 | Q2-24 | Q2-24 | 2025 | 2030

ISO 9001:2015 COMPANY — Q1-23

ISO 9001:2015 COMPANY — Q3-23

IATF 16949:2016 COMPANY — Q2-24

Pilot Line
10 kwpy

HVM Line (Ramp-up)
>100 kwpy

HVM Line (Full Capacity)
Up to 500 kwpy

150mm — Prototyping — High Volume Manufacturing

SmartSiC™-Performance
Ultra-low resistivity

200mm — Prototyping — High Volume Manufacturing

SmartSiC™-Advanced
Ultra-low defectivity
Ultra-low resistivity

200mm — Prototyping — High Volume Manufacturing

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