AIM Photonics

AIM Photonics Foundry providing Co-Process and Co-Development to Address Challenges in Photonic Integrated Circuit (PIC) Packaging

Presented by
David Harame, COO AIM Photonics

PIC INTERNATIONAL CONFERENCE
ANGELTECH

April 16, 2024 12:00-12:15 PM , Brussels, Belgium
PIC Packaging: Securing Optimal Integration and Performance

AIM PHOTONICS

AIM Photonics – A US Department of Defense Manufacturing Innovation Institute

Advance integrated photonic circuit and packaging **manufacturing** technology

Make the technology available

Create an adaptive integrated photonic circuit workforce

AIM provides an **accessible** best in class state-of-the-art 300mm Photonic Integrated Circuit (PIC) MPW, Heterogeneous-Integration (HI), Interposers, and Test, Assembly, & Packaging (TAP) capabilities and services. We provide end-to-end photonics and advanced packaging solutions.

NYCREATES Albany NanoTech Facility

- AIM uses the Albany NanoTech 300mm Facility with (>130K square feet of class-1 clean room)
- AIM also has the Rochester Test Assembly and Packaging (TAP) facility (12K square feet of class-1000 clean room)

AIM Photonics TAP facility

AIM Photonics PIC and Packaging Foundry enables co-design

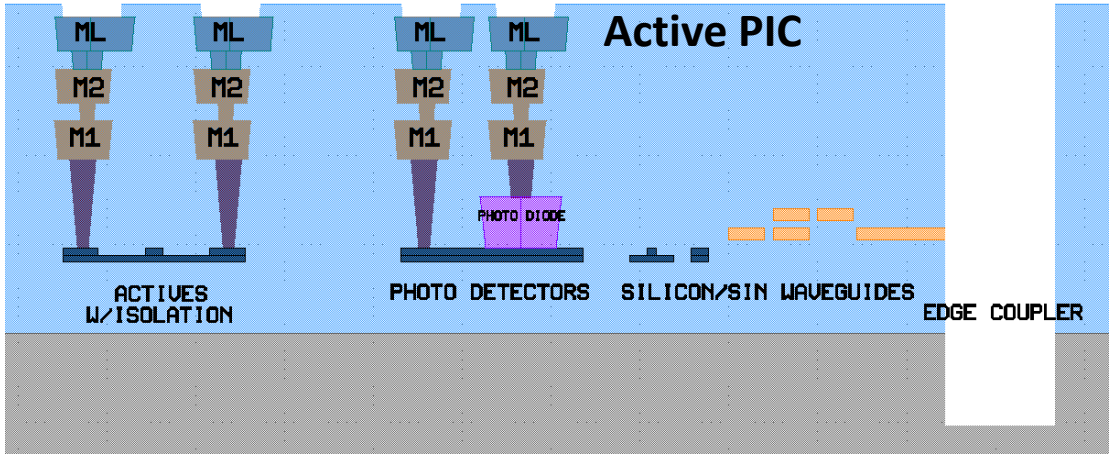
- Co-process Co-design is critically important for low cost low loss integrated photonic packaging
- It is important to leverage already existing electronic packaging assembly processes and tools in co-packaged optics designs.
- AIM has both the PIC side and the packaging side which enables co-design and an end to end "accessible" flow
- Innovation requires facilities with access to basic electronic and photonic packaging processes to try out new solutions
- Standardization is key for the industry to develop low cost solutions

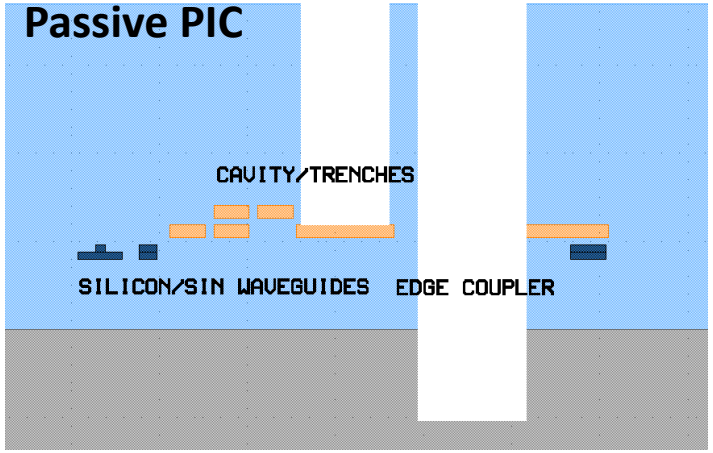
AIM Photonics Core Areas

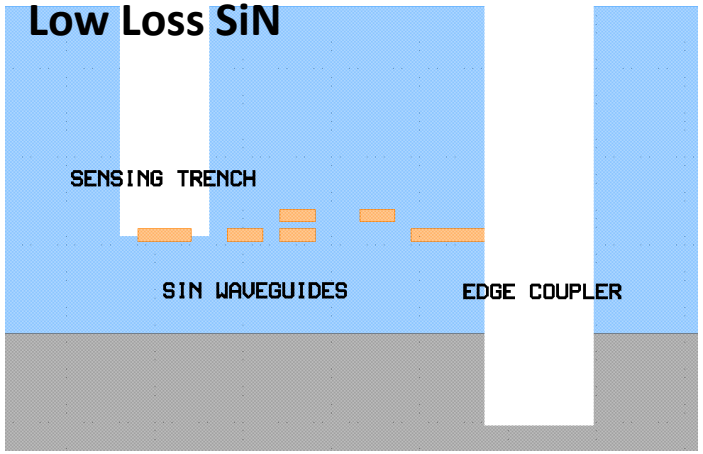
1. Photonic Integrated Circuits
2. Heterogeneous Integration and Interposers
3. Test, Assembly and Packaging
4. Electronic, Photonic Design Automation

AIM Photonics Production PIC MPW Technology Offerings

- AIM has a regular schedule of its best in class, mature 300mm PIC and Interposer MPW runs.

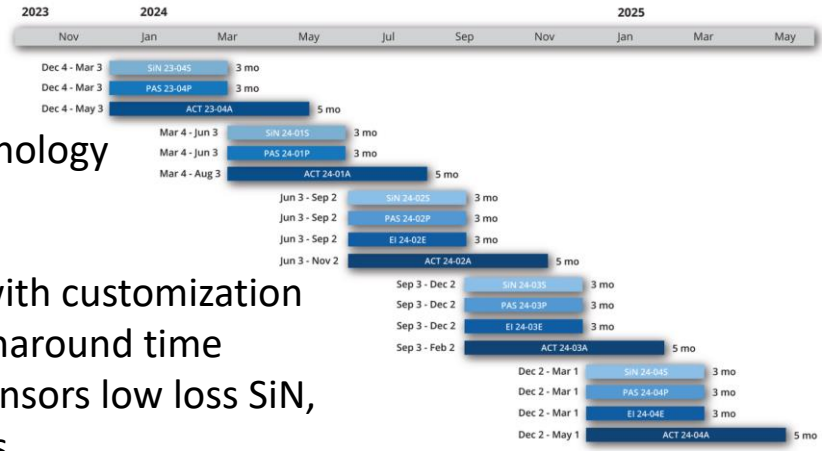




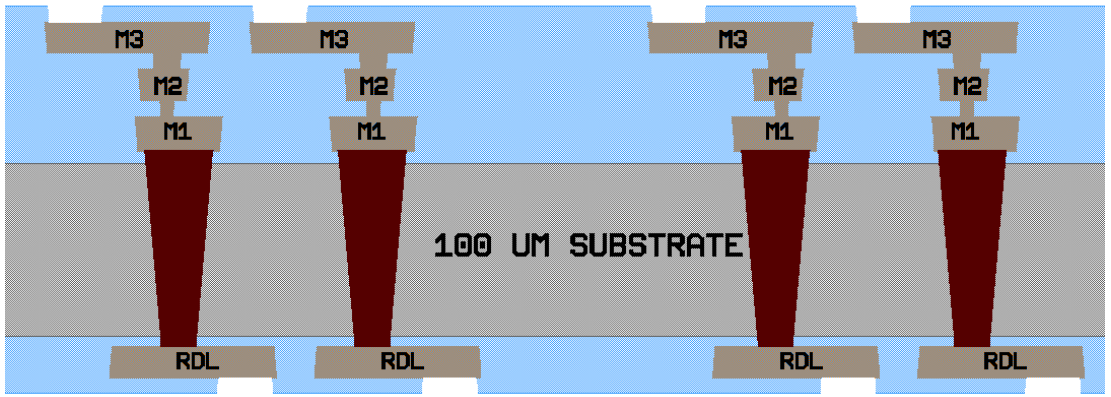


https://www.aimphotonics.com/mpw

- AIM has quarterly MPW release schedule
- Best in class 300mm technology performance
- Accessible technologies with customization
- Fastest 300mm MPW turnaround time
- Active and Passive PIC, Sensors low loss SiN, and Electronic Interposers



Electronic Interposers



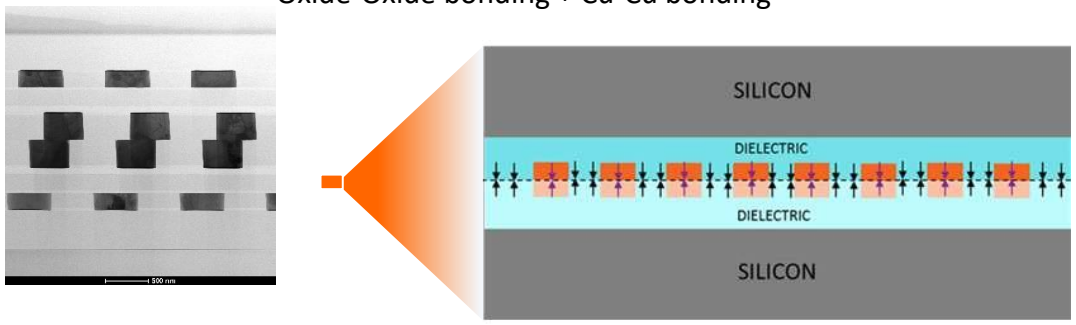
AIM Photonics' 300mm Wafer Level Heterogeneous Integration

These are AIM Photonics' processes running in the 300mm wafer HI center in Albany NY. AIM will do custom Heterogeneous Integration services for complex Co-Packaged optics.

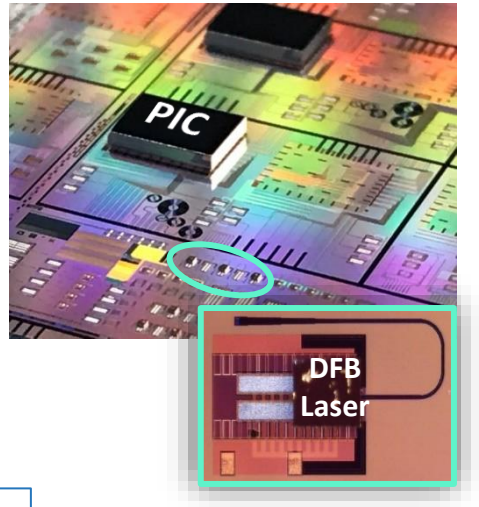
Wafer to Wafer bonding / de-bonding	Hybrid Bonding	2.5D chip on wafer	Dense Bumping

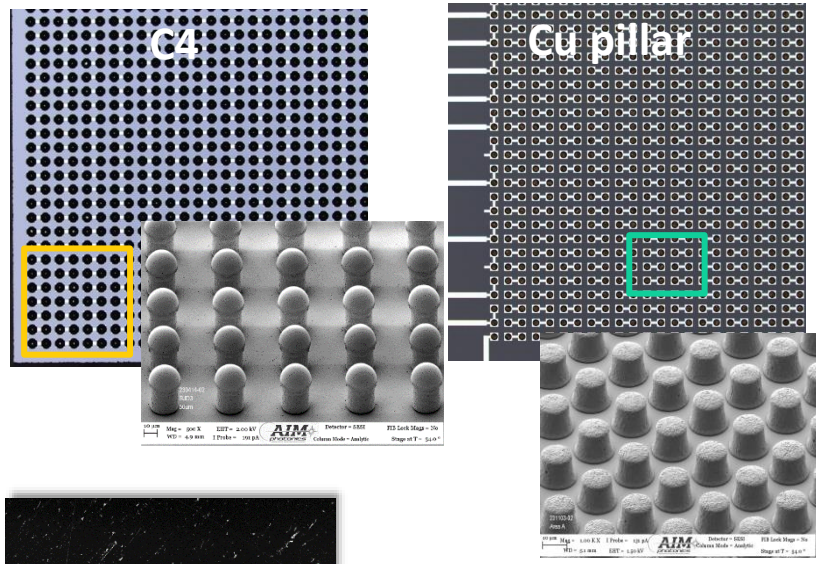
Hybrid Bonding

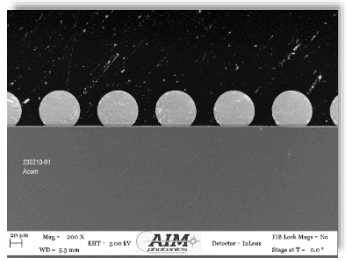
Oxide-Oxide bonding + Cu-Cu bonding



Source: AMD Hot Chips 2021



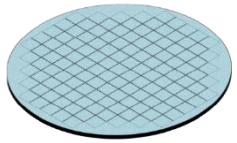


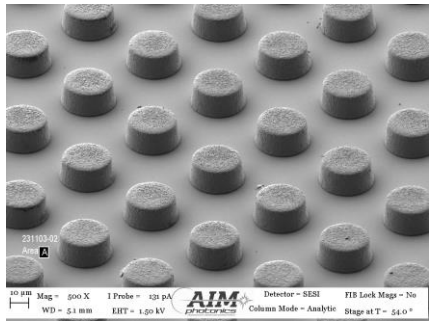


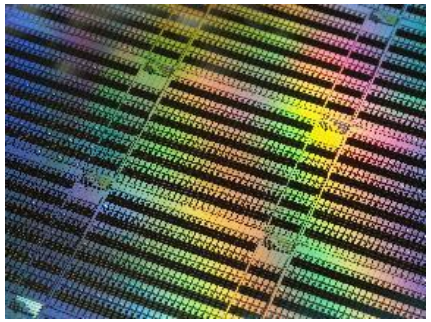
Heterogeneous Integration (HI) is defined as the integration of separately manufactured components into a higher-level assembly (chiplets, SiPs, modules) that, in the aggregate, provides enhanced functionality and improved operating characteristics.

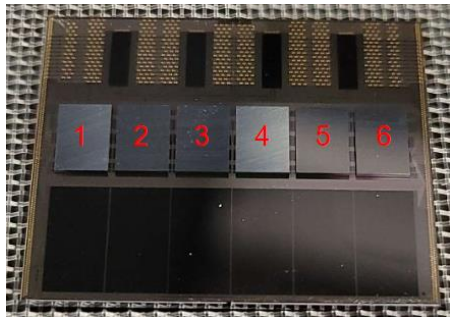
Existing and enabling processes at TAP

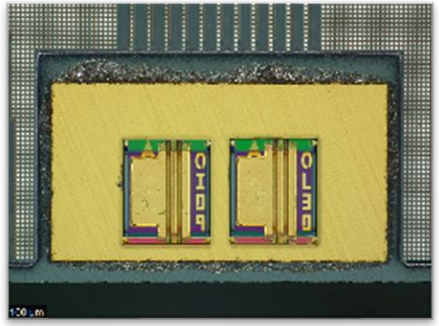
- The existing toolset at TAP is capable many types of 3D assembly builds from 300mm wafer bumping to chip-level thermocompression bonding, fiber attach, metrology and test.

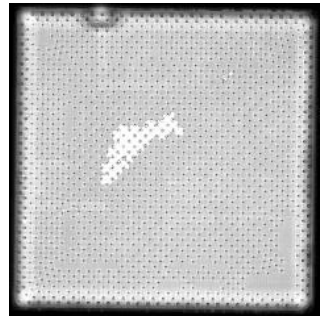


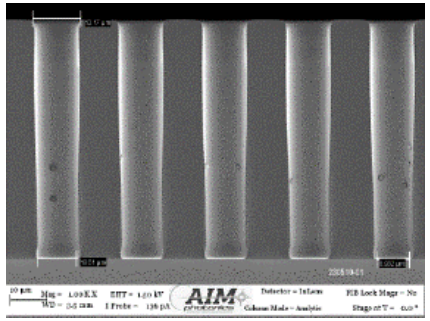


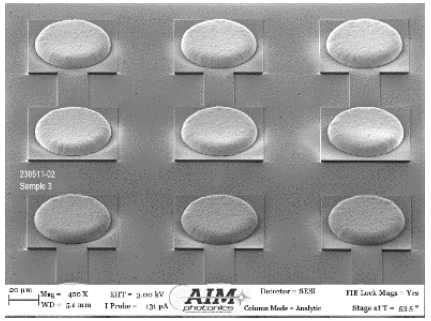


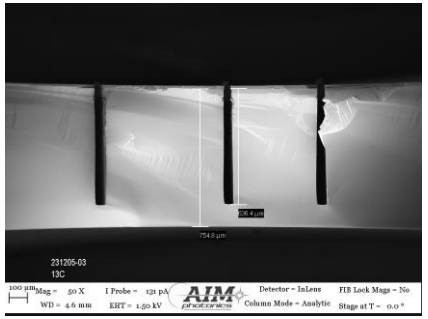


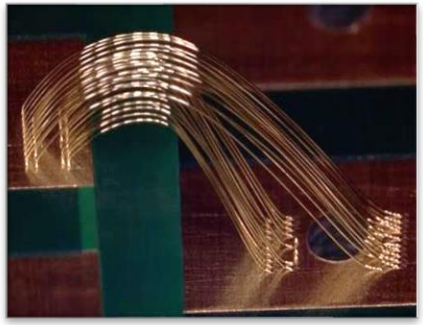


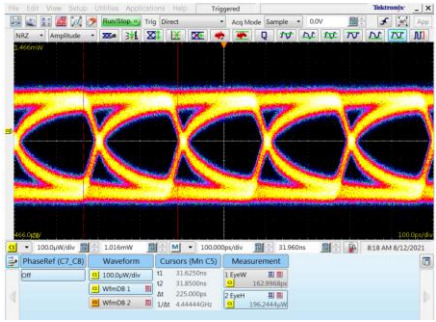








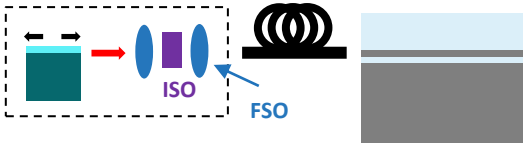




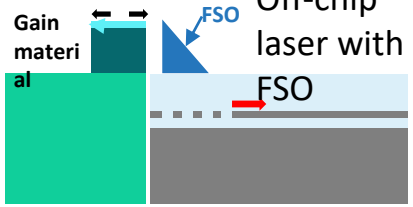
Techniques to attach a laser to a silicon PIC

- On-chip light sources are becoming more attractive due to tight integration with the PIC and low coupling losses
- Utilize Known-Good-Die (KGD) from commercial vendors
  - Leverage existing infrastructure and expertise
- For lower volumes and to maximize yield, flip-chip laser integration is preferred

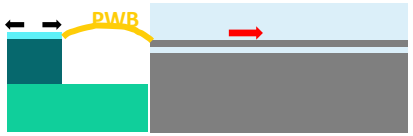
Conventional off-chip laser



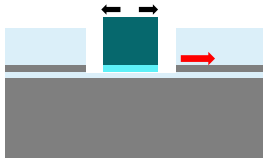
Off-chip laser with FSO



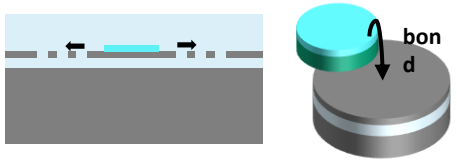
Off chip with Photonic Wire Bond (PWB).



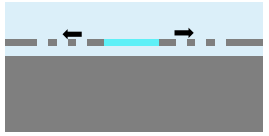
2.5D HI (flip chip or transfer printing



Hybrid III-V coupon with direct bonding or transfer printing on silicon



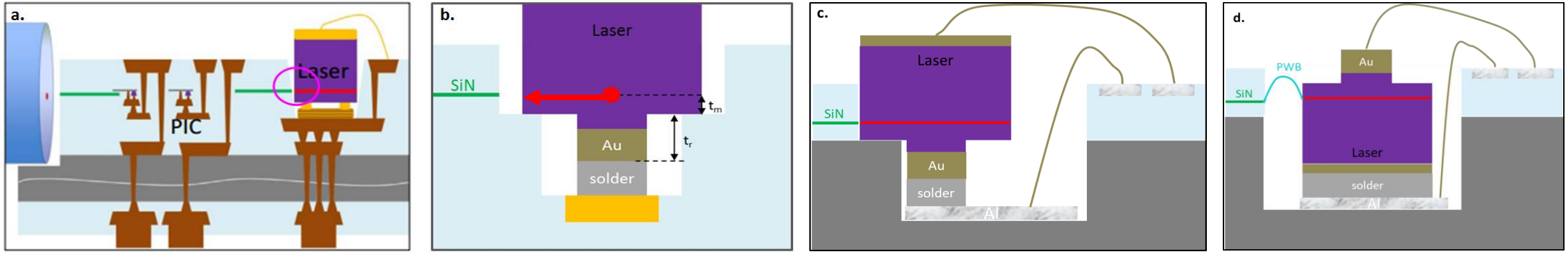
Monolithic (Heteroepitaxy)



Integration	Conventional off-chip	Off-chip with FSO	Off-chip with PWB	2.5D HI (flip-chip/µTP)	Hybrid III-V coupon (Direct bonding/µTP)	Monolithic (heteroepitaxy)
Coupling Loss	>2dB	>2dB	>2dB	1dB	1dB	Few dB
Output Power	High	High	High	Medium	Medium	Low
Polarization Control	Needed	Needed	No Need	No Need	No Need	No Need
Thermal Management	Easy	Easy	Easy	Medium-Difficult	Difficult	Medium
Linewidth Reduction	N/A	Good	Good	Good	Best	Good
Assembly Size	Large	Medium	Medium	Small	Small	Smallest
On-chip	No	No	No	Yes	Yes	Yes
Packaging Style	KGD	KGD	KGD	KGD	All or nothing	All or nothing

Adapted from: Shekhar, S., Bogaerts, W., Chrostowski, L., Bowers, J. E., Hochberg, M., Soref, R., & Shastri, B. J. (2023). Silicon Photonics--Roadmapping the Next Generation. *arXiv preprint arXiv:2305.15820*.

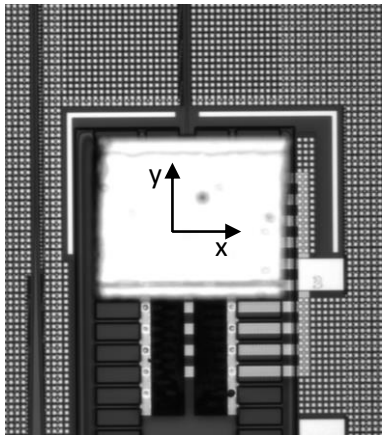
AIM Laser Integration for On-chip Light Sources

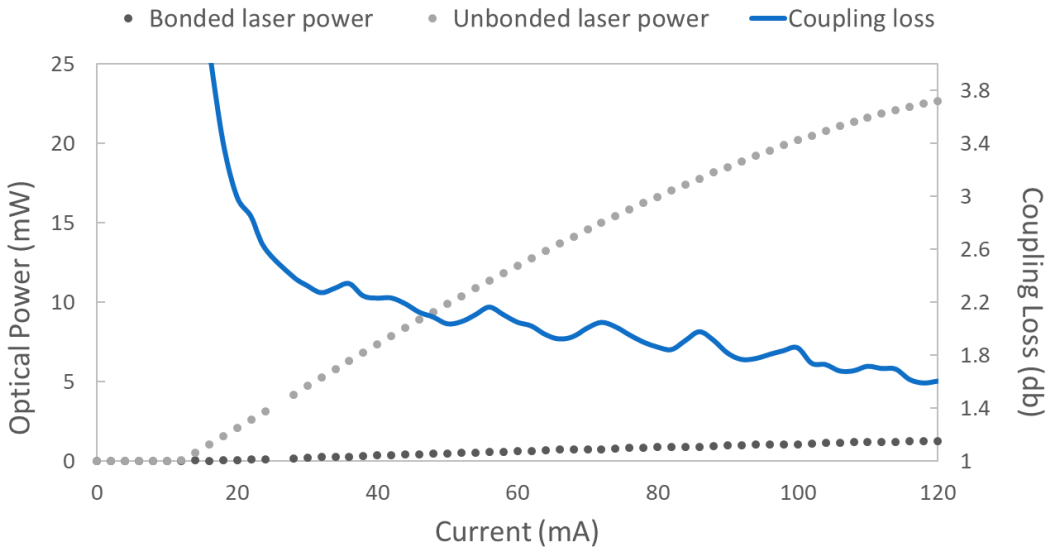


a. Cross-section of the active interposer with a flip-chip attached III-V laser source. **b.** Detailed structure of laser reference layer to output mode (t_m), reference layer to Au bond pad (t_r), and dielectric shelves for laser placement. **c**. Schematic of laser attach on AIM Photonics PIC MPW platform (only interfacial layers indicated). **d.** Integration variant of **c**. using photonic wire bonding (PWB) instead of butt coupling (requires much deeper Si trench since laser is not flipped). *NOTE: figures not to scale.*

- Flip-chip laser attach with edge coupling variants
  - Total coupling loss @ 120mA: 1.58 dB (optimize for process yield)
- Platform flexibility:
  - Laser trench formation and waveguide layer variations, Interposer and PIC platforms
- Photonic wire bonds (PWBs) an option.

Laser in trench





Photonic packaging optical coupling methods

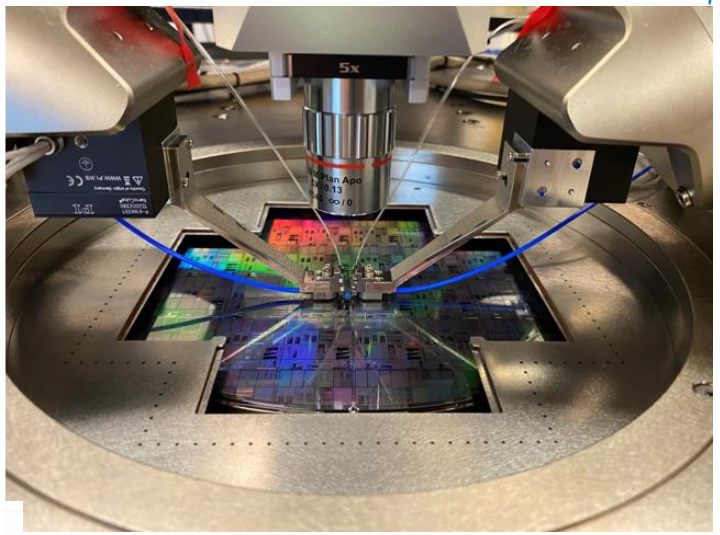
Photonic needs to be more like electronic couplers for sustainable low cost. Difficult to achieve specs in HVM

Technique	Loss	Polarization	Bandwidth	1 dB Alignment Tolerance	Density	Comment
Gratings	>1.5 dB	TE, TM	30-80 nm (1 dB)	2 µm	☹	Highest loss but simplest to test and couple to
Edge Coupling	>0.4 dB	TE & TM	>100 nm (3 dB)		☺	Alignment time
Evanescent	0.13 dB	TE & TM	>300 nm (1 dB)	>2.8		Requires exposed waveguides + alignment
Microlenses	>1.7 dB	TE & TM		30 µm		Alignment critical, mechanical coupling
Photonic Wirebonds	>0.5 dB	TE & TM	300 nm (1 dB)		☹	Writing time + loss
Free Space Polymer	0.5 dB	TE & TM	100 nm (1 dB)	6 µm	☺	Potential 3D and vertical

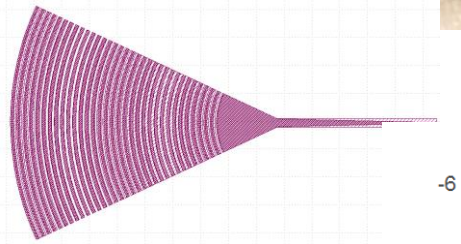
Also see L. Ranno, et. al., "**Integrated Photonics Packaging: Challenges and Opportunities,**" *ACS Photonics* 2022, 9, 3467−3485

Grating Coupling and Co-Process Co-Design

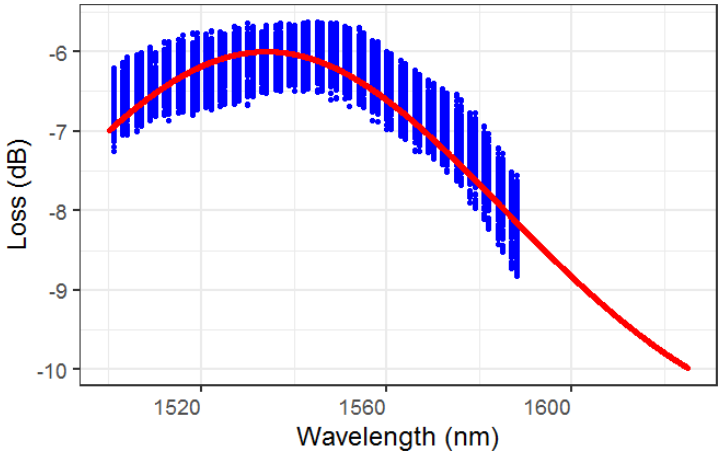
- Advantages and Uses:
  - Easy alignment (±1 mm)
  - Wafer level coupling so extensively used in wafer level characterization
  - Potential for High Density (with 2D arrays)
- Disadvantages:
  - High coupling loss (Typ. 3-4dB)
  - Low bandwidth (<100nm)
  - Polarization sensitive, angular dependence
- Co-Process and Co-Design
  - Requires careful design and optimization using existing process features



Example Measurement Setup



Example Grating Structure

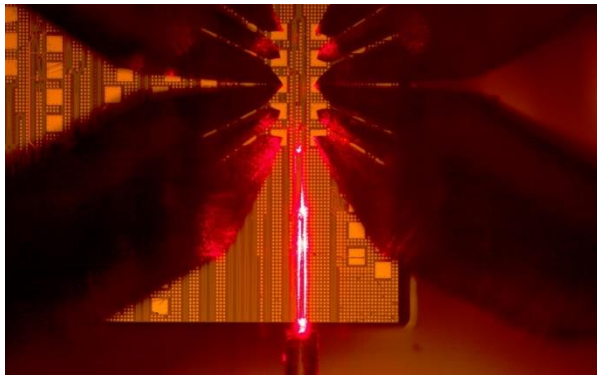


Example Loss (dB) vs. Wavelength

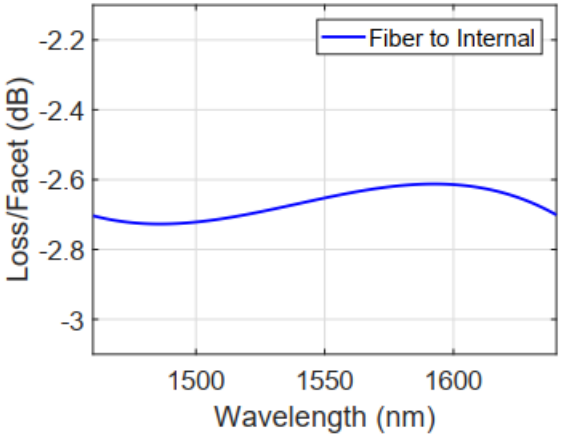
"Exploring the Methods, Challenges, and Solutions for PIC Packaging, " Stefan Preble, Photonics Media 2023

Edge Coupling Co-Process & Co-Design

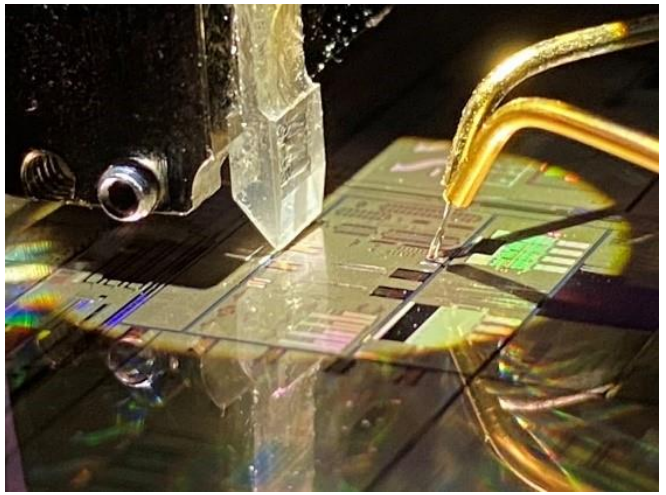
- Advantages of coupling over other methods
  - Low coupling loss (<3dB) achievable
  - Broad bandwidth (>100nm)
  - Polarization maintaining
- Disadvantages
  - Poor alignment tolerance
  - Efficient coupling to SMF28 requires thick oxide or Silicon substrate removal/undercut
  - Lower channel density (along the edge)
  - Requires edge preparation (etch or polish)
  - Difficult on wafer measurements
- Co-process Co-Design
  - Edge coupling structure for improved alignment tolerance
  - Thick oxide or Silicon substrate removal/undercut
  - Requires edge preparation (etch or polish)
  - Passive vs. active alignment

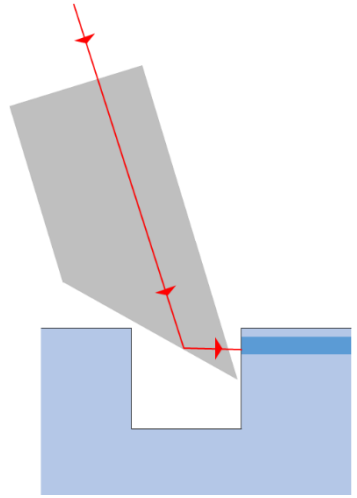


Example Edge Coupler measurement setup



Example Edge Coupler Loss/Facet (dB) vs wavelength measurement





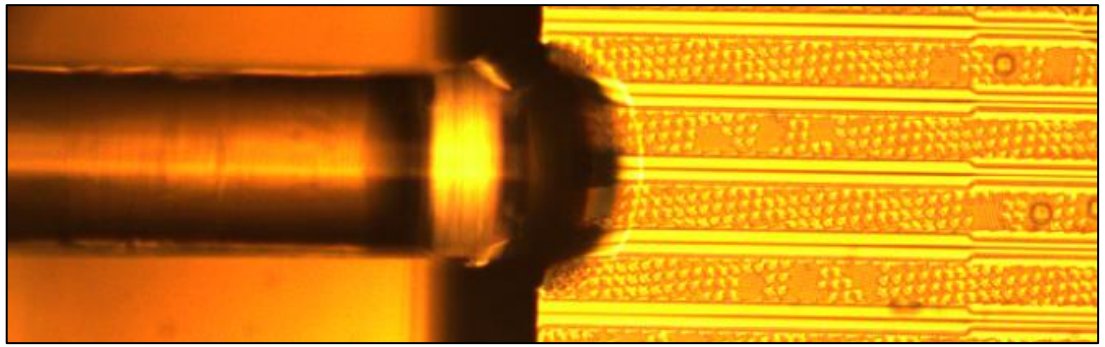
Example Wafer Level Edge Coupler Measurements

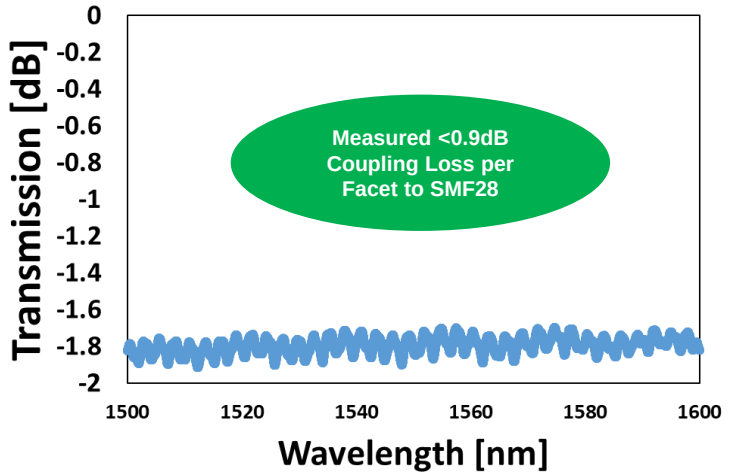
Low-Loss Coupling

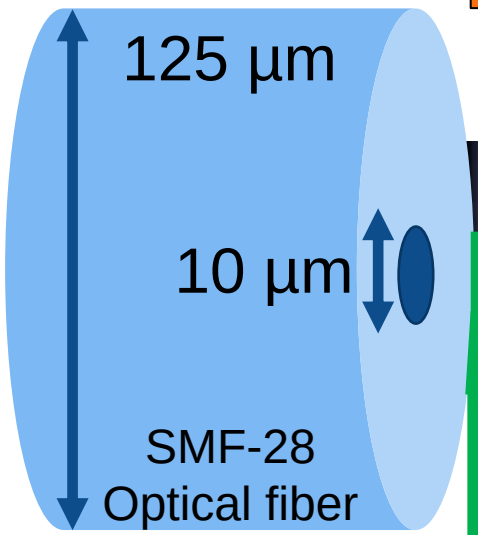
"Exploring the Methods, Challenges, and Solutions for PIC Packaging," Stefan Preble, Photonics Media 2023

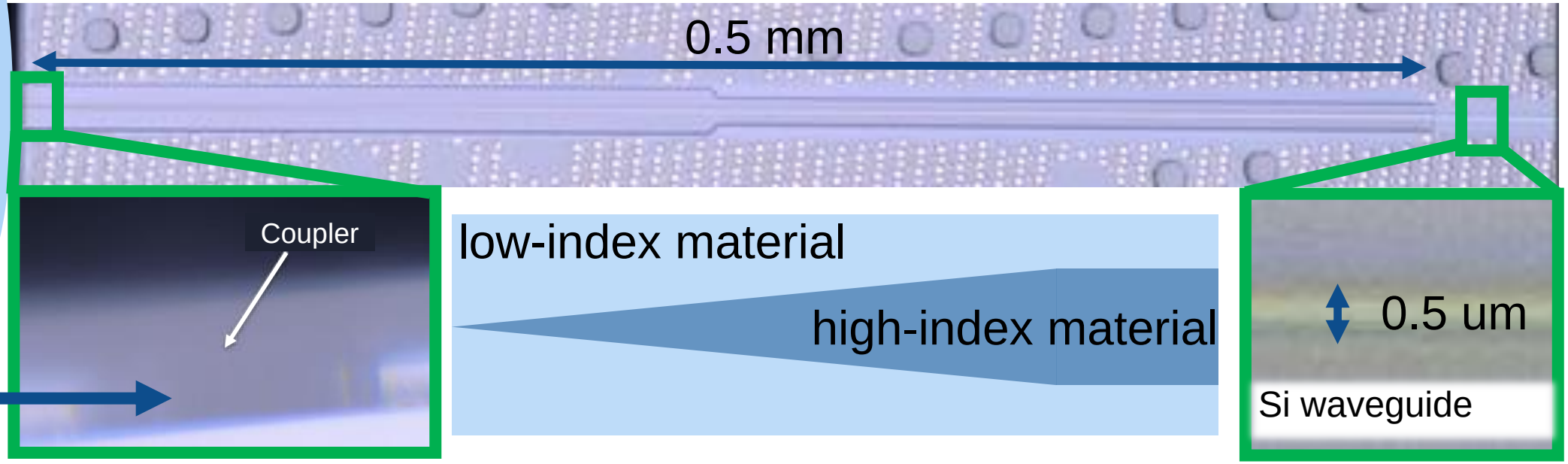
- Low-loss coupling directly to SMF28 (<1dB/facet)
  - Remove high index substrate underneath the edge coupler

Courtesy Stefan Preble RIT









Remove high-index substrate under waveguide

AIM Photonics Design-Assembly-Test Enablement Platform

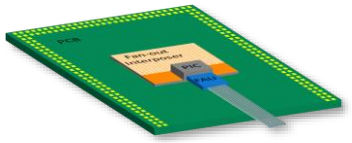
Design Rules

Layouts

Models

AIM Photonics PDK

User Circuit, Assembly Concept



AIM Photonics Interposer Design Kit

Assembly Rules

RF Sim Support

Interposer Design Kit

Assembly Design Guide

PIC, Interposer, Assembly Design

Fabrication at Albany NanoTech Complex, Albany, NY

Assembly, Packaging, at AIM Photonics TAP facility, Rochester, NY

AIM Photonics Measurement Design Kit

Design Guidelines

Padset Library

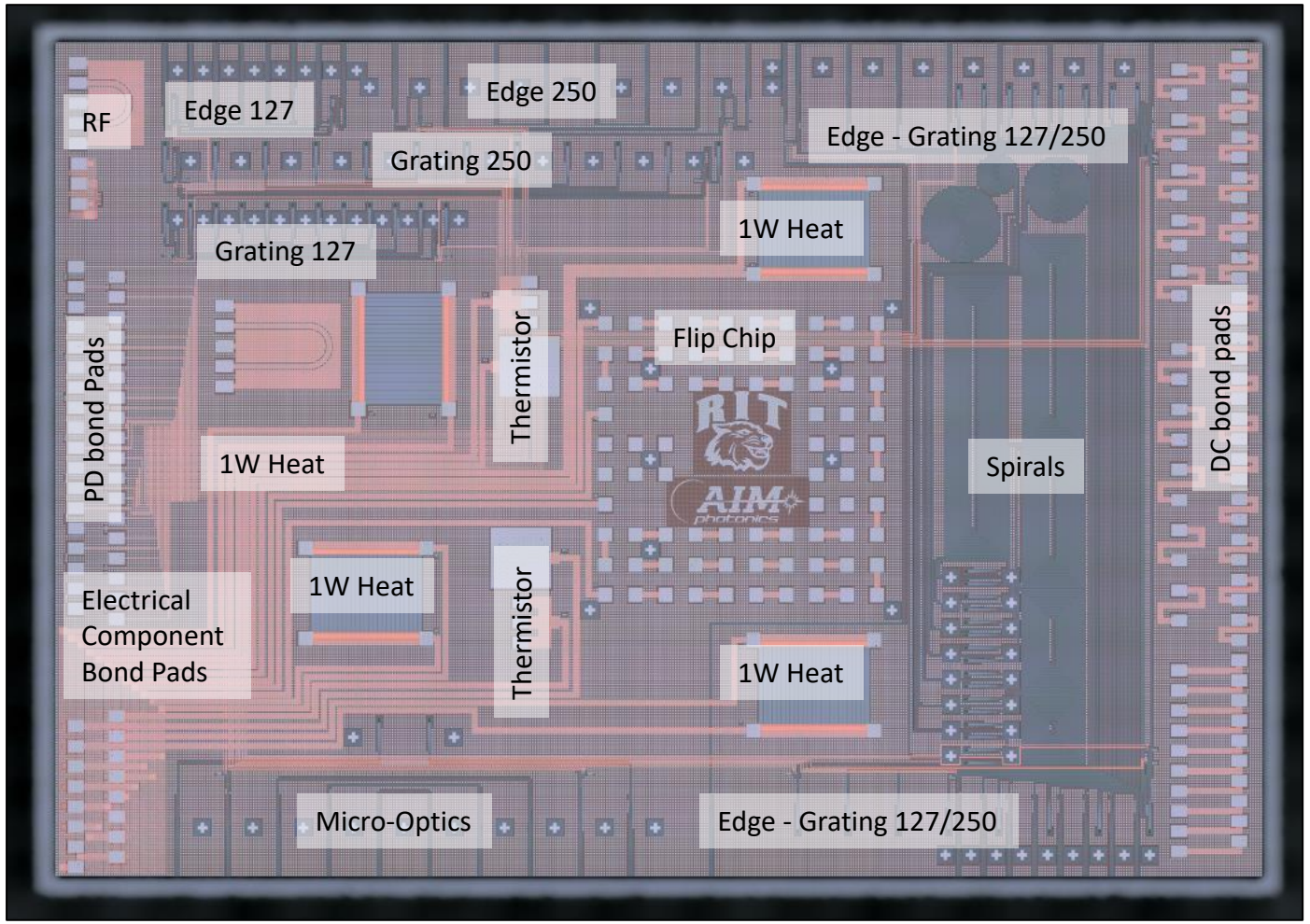
Test plans

Automated Test on Dies, Wafers

AIM Packaging Reference Chip for Standards

Reference chips facilitate the development of robust packaging processes and benchmarking of capabilities

- Edge and Grating Couplers
  - Standard Pitches and Mode Sizes
- Photodetectors for active alignment
- RF & DC Electrical Test Structures
- Flip Chip Electronic IC Integration
- Heaters and Thermistors
- Platform for continuous innovation



Rochester Institute of Technology © stefan.preble@rit.edu

Summary

- Co-process Co-design is critically important for low cost low loss integrated photonic packaging
- AIM Photonics has both the PIC side and the packaging side which enables co-design and an end to end “accessible” flow
- Innovation requires facilities with access to basic electronic and photonic packaging processes to try out new solutions
- It is important to leverage already existing electronic packaging assembly processes and tools in co-packaged optics designs.
- Standardization is key for the industry to develop low cost solutions