GE Aerospace

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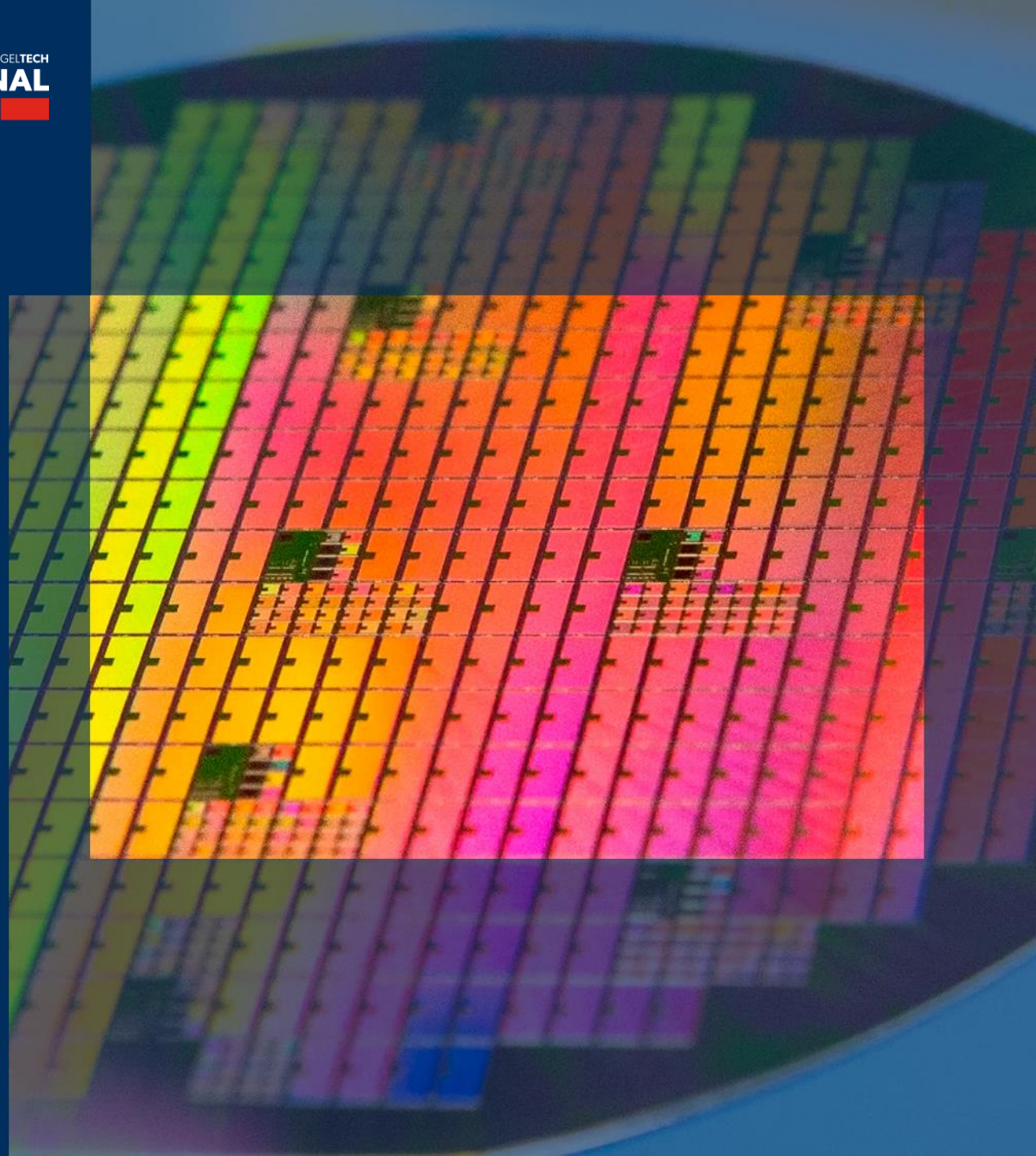
Giving SiC a Superjunction



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Future of SiC Medium-Voltage (MV) Applications

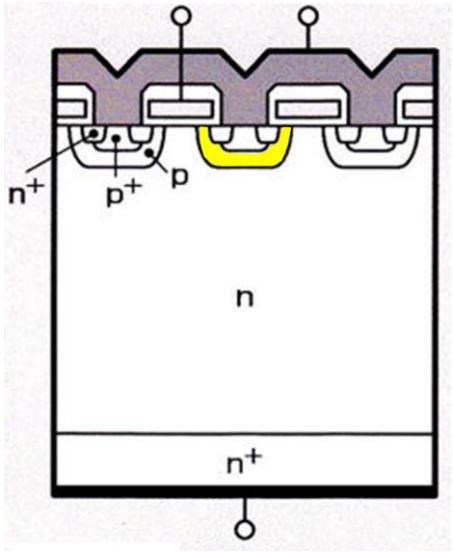
CHALLENGE :
SCALING SIC DEVICES TO ULTRAHIGH-VOLTAGE LEVELs for MV HIGH FREQUENCY SYSTEMS!

Outline

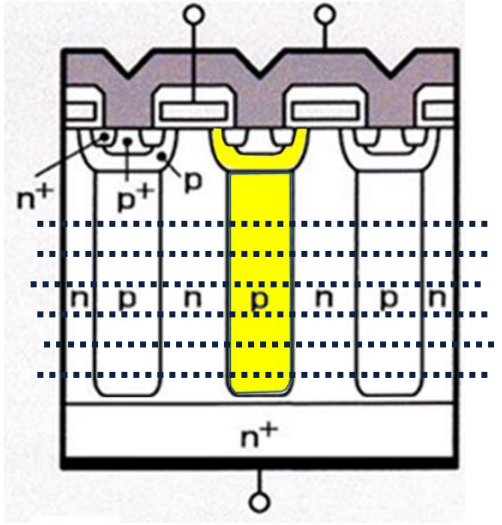
- Introduction on SiC device options for scaling to medium voltage applications
- 4.5 kV SiC Charge-Balanced MOSFETs
- 3.5kV and 5kV Deep-Implanted SiC Super-Junction Devices
- Summary and Conclusion

SiC Device Options for Scaling to Medium Voltages

Conventional Unipolar Devices



Super-Junction Devices



?

Any other practical SiC device design for best performance at LF and HF in MV space?

$R_{Drift} \sim BV^{2.4}$

- High conduction loss at elevated temperatures
- limited to low current densities….. ~20A/cm^2
- Marginally better than incumbent Si IGBTs in high frequency switching applications

$R_{Drift} \sim BV^{1\text{-}1.3}$

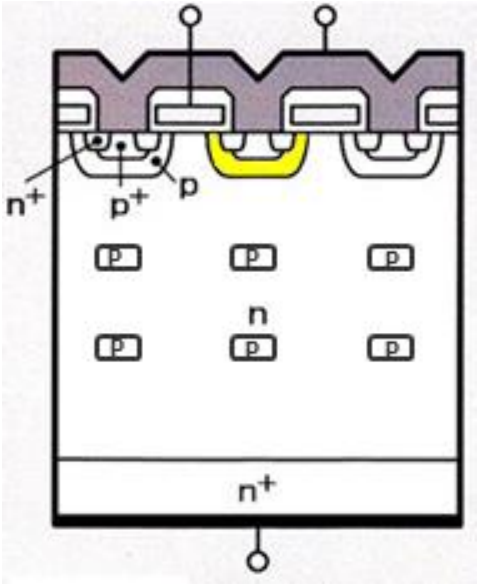
Complex fabrication process

- Multi-epitaxial growth: Limited to low voltage devices (thin epi)[1]
- Trench and re-fill: Suffer from crystallographic damages[2]

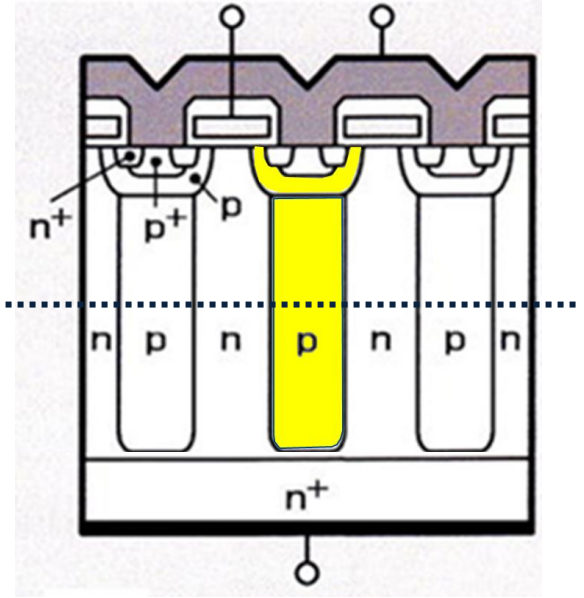
[1]T. Tanaka et al., 2018 IEEE Int. Electron Devices Meet., p. 8.2.1-8.2.4, 2019.
[2]R. Kosugi et al., in 2019 31st ISPSD, 2019, pp. 39–42.

SiC Device Options for Scaling to Medium Voltages

Approach 1
Charge-Balanced Devices



Approach 2
Deep-Implanted SJ Devices

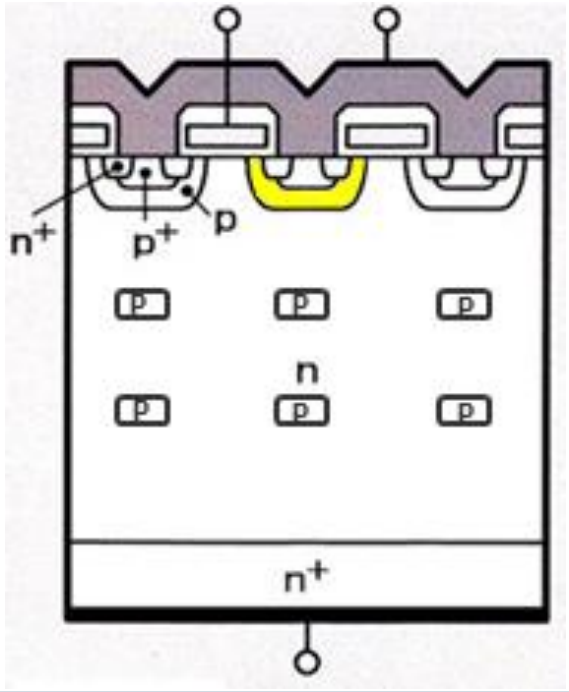


Approach 1

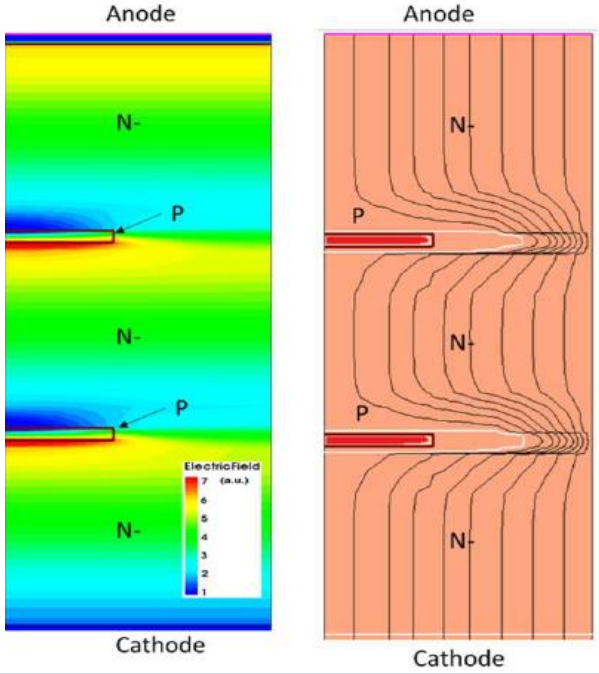
SiC Charge-Balanced Devices

SiC Charge-Balance Devices

Charge-Balanced Devices



Electric Field Distribution

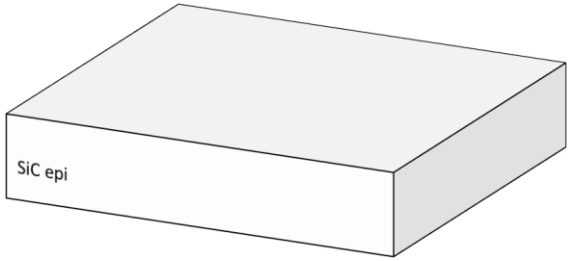


- New scalable drift region architecture
- Buried CB-regions can balance charges and behave as electric field dividers (similar to SJ devices)
  - Allowing increase of drift region doping for same breakdown voltage → Lower conduction losses

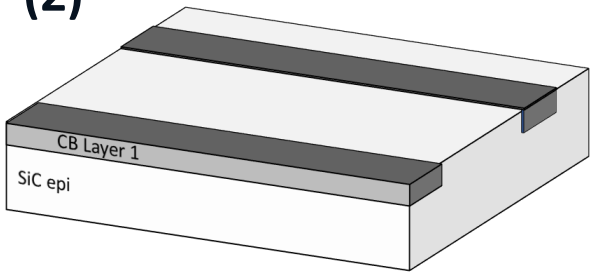
SiC Charge-Balanced (CB) Technology

Fabrication Steps (1-5)

(1)



(2)



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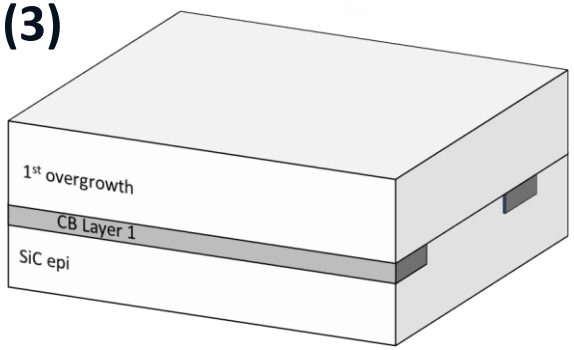
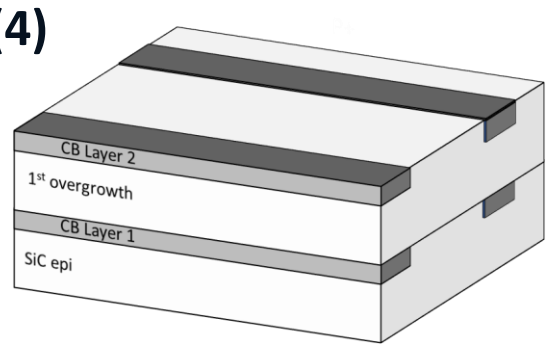


(4)



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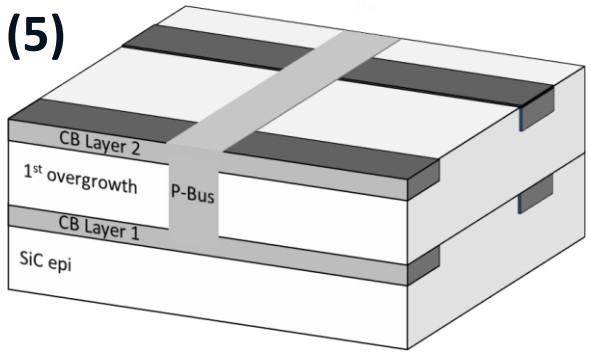


Starting material

- 10-12um n-type epitaxial layer ($1x10^{16}$ cm^{-3}).

Charge-Balanced (CB) Region

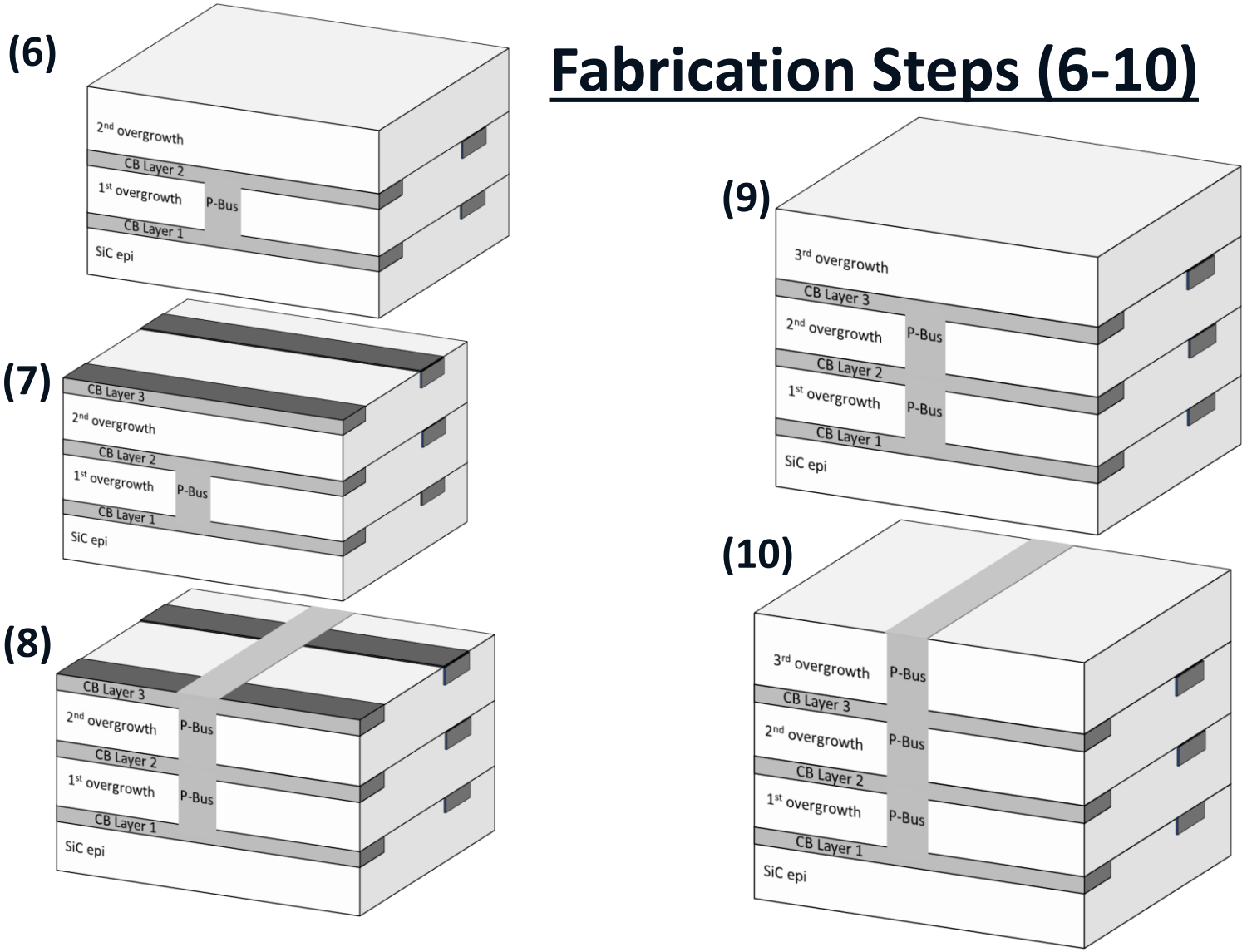
- Shallow Al implantation in between growth runs to form buried CB regions.

Deep Implanted P-Bus

- Intermittent vertical P-type pillars (P-Bus) to avoid floating CB-regions
- Formed using high energy implantation (>20MeV) of Al (12um deep) to supply holes from P+ anode/source contact to buried CB-layers.

SiC Charge-Balanced (CB) Technology

Fabrication Steps (6-10)



Epitaxial Over-growth

- Three consecutive epitaxial overgrowth (10-12um n-type $1x10^{16}$ cm^{-3}).

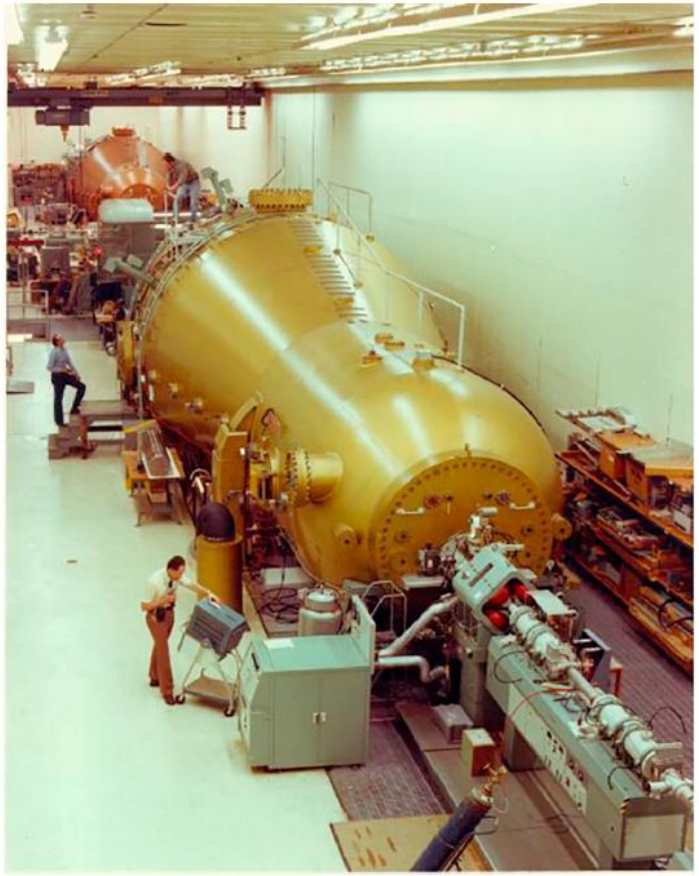
Charge-Balanced (CB) Region

- Multiple buried charge-balanced regions formed using shallow Al implantation.

P-Bus

- Multiple P-Bus pillars formed using similar high-energy implantation.

Deep Implantation of SiC



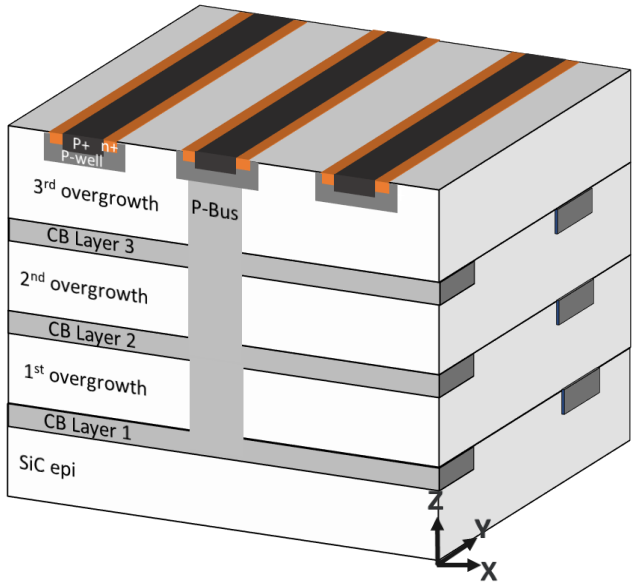
- High energy ion implantation at the Tandem Van de Graaff facility at Brookhaven National Laboratory[1].
- The accelerator offers 15-megavolt electrostatic acceleration and is ideal to form deep junctions in SiC.
- Low-dose high-energy implantation was done at room temperature.

[1]P. Thieberger, et.al, Nuclear Inst. and Methods in Physics Research B 442 (2019) 36–40

SiC Charge-Balanced (CB) Technology

4.5kV SiC CB MOSFET

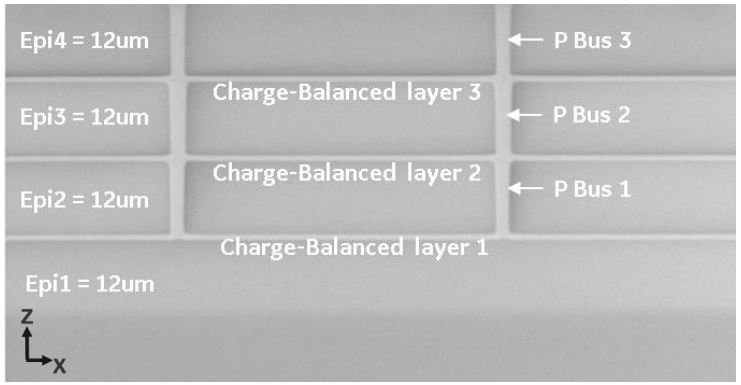
3D Perspective View



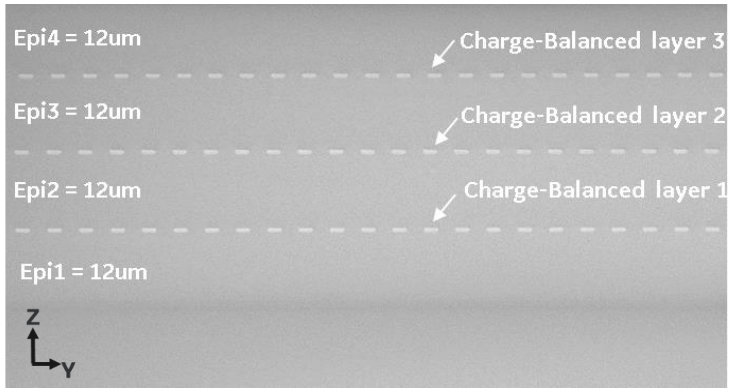
CB Drift layer and standard MOSFET on the top

Cross Sectional SEM View

Parallel to the MOSFET gate fingers



Perpendicular to the MOSFET gate fingers



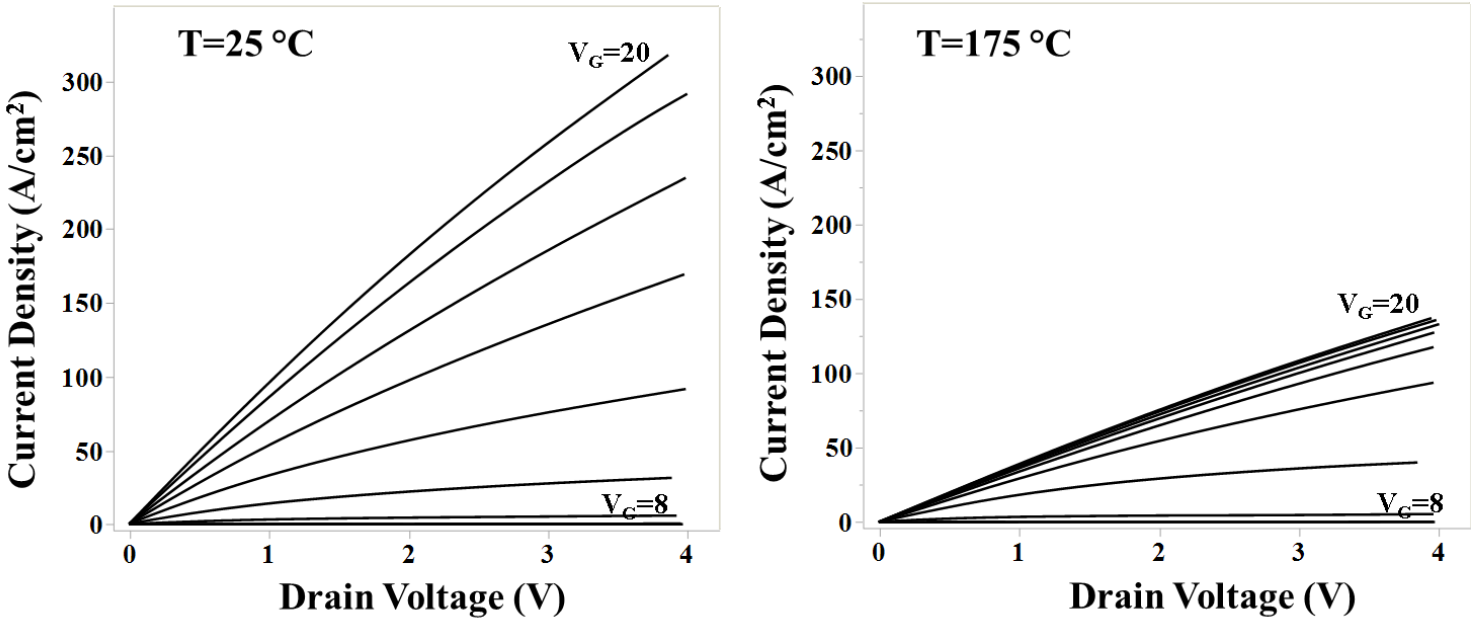
Advantages of Charge-Balanced Process

- **Scalable: 1.2kV to >4.5kV**
- **Compatible with any power device**
  - **PiN or JBS diodes, MOSFETs (planar/non-planar), JFETs or BJTs**

[1]**R.Ghandi et.al.** ***2020 ISPSD*****, pp. 126-129.**

4.5kV SiC Charge-Balanced MOSFETs

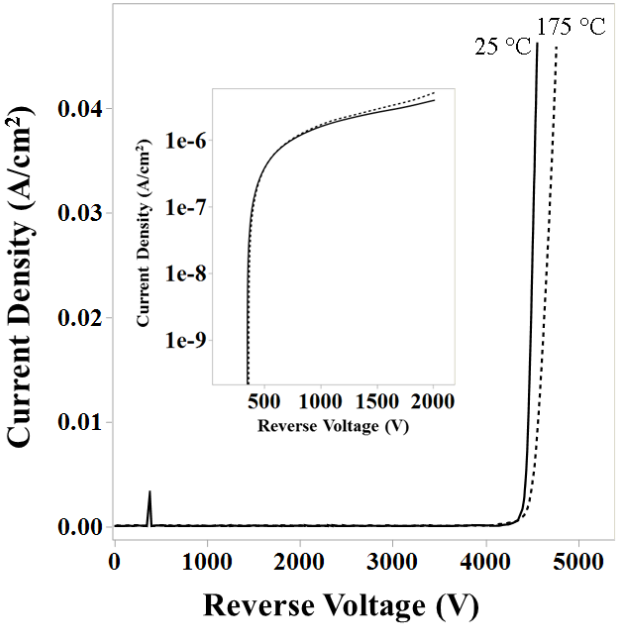
Forward Characteristics (V_D=0.1V)



$R_{on,sp}$ (25 °C) = 10 mΩ-cm²
$R_{on,sp}$ (175 °C) = 25 mΩ-cm²

20% improvement from SiC unipolar limit

Reverse Characteristics

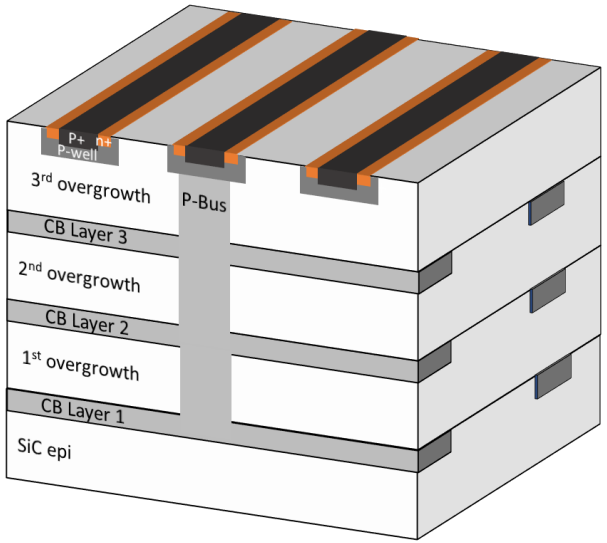


BV (25 °C) = 4.5 kV
BV (175 °C) = 4.64 kV

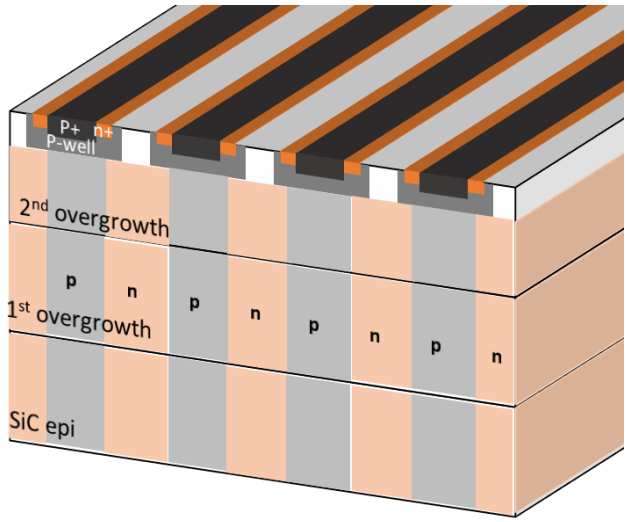
Leakage current density <1x10^{-5} A/cm² for V_R<2kV

Towards Deep-Implanted Super-Junction Technology

4.5kV SiC CB MOSFET



Deep Implanted SiC SJ Devices



- **Deep implanted p-Bus process can enable SiC super-junction technology.**

- **Challenge:**

  Demonstration of high-density, high aspect ratio implanted n-pillars and p-pillars.

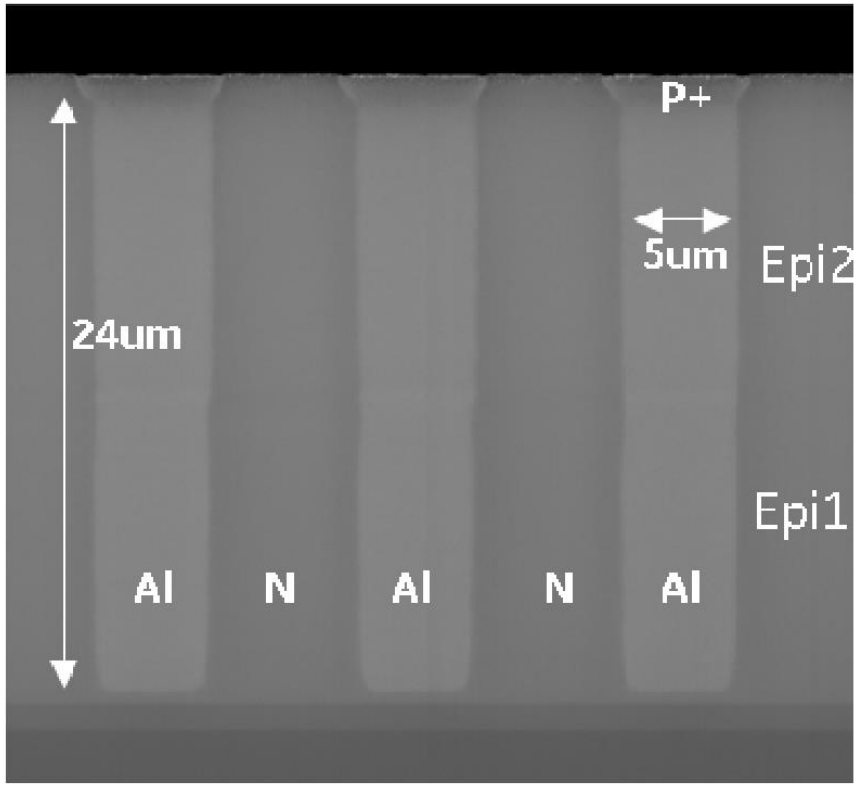
  Potential high-level of defects followed by multiple rounds of high-energy implantation.

Approach 2

SiC Deep-Implanted Super-Junction Devices

SiC Deep Implanted Super-Junction JBS Diode

GE's 3.5kV Super-Junction JBS Diode



Epitaxial Over-growth

- Two consecutive epitaxial overgrowth (12µm n-type $1x10^{15}$ cm^{-3})
- Total Drift Layer Thickness 24µm

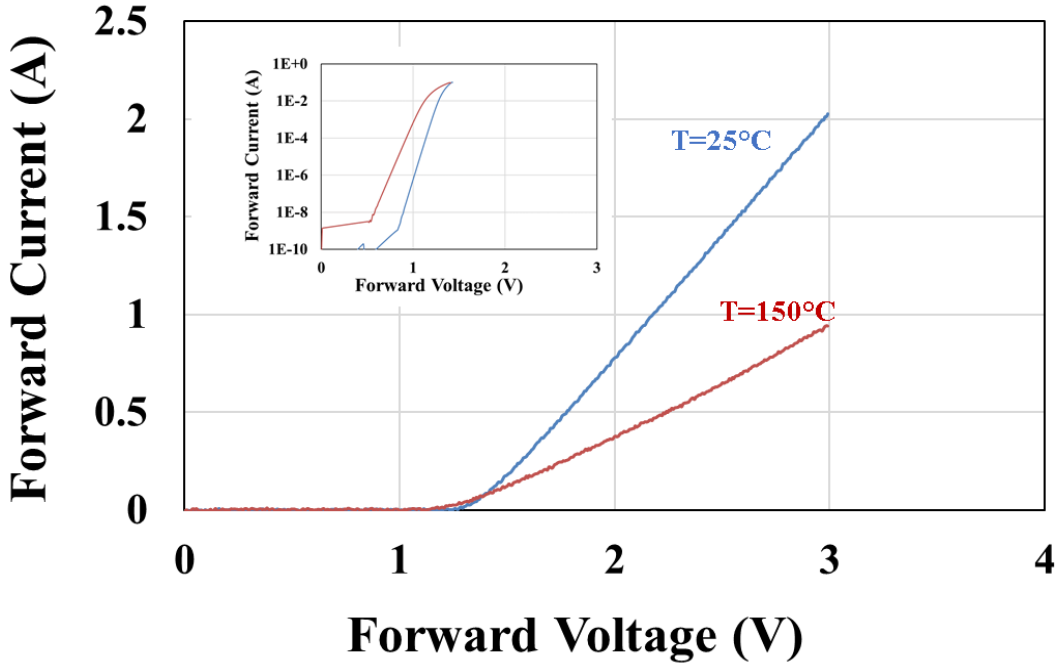
N-doped and P-doped SJ Pillars

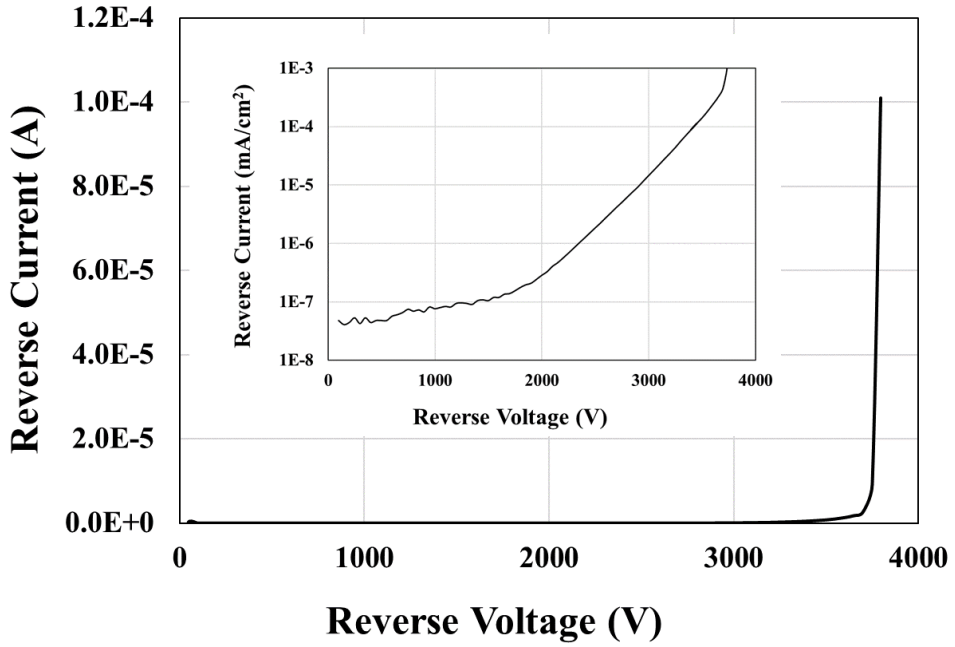
- Intermittent vertical P-type and N-type pillars (5µm $1x10^{16}$ cm^{-3})
- Formed using high energy implantation (>20MeV) of Al and N (12um deep)

Standard top P+ JBS and JTE Implantation, activation anneal, metallization and surface passivation

3.5kV SiC Deep Implanted Super-Junction JBS Diode

Forward and Reverse Characteristics





$R_{on,sp}$ (25 °C) = 4.5 mΩ-cm²
$R_{on,sp}$ (150 °C) = 9.6 mΩ-cm²

45% improvement from SiC unipolar limit

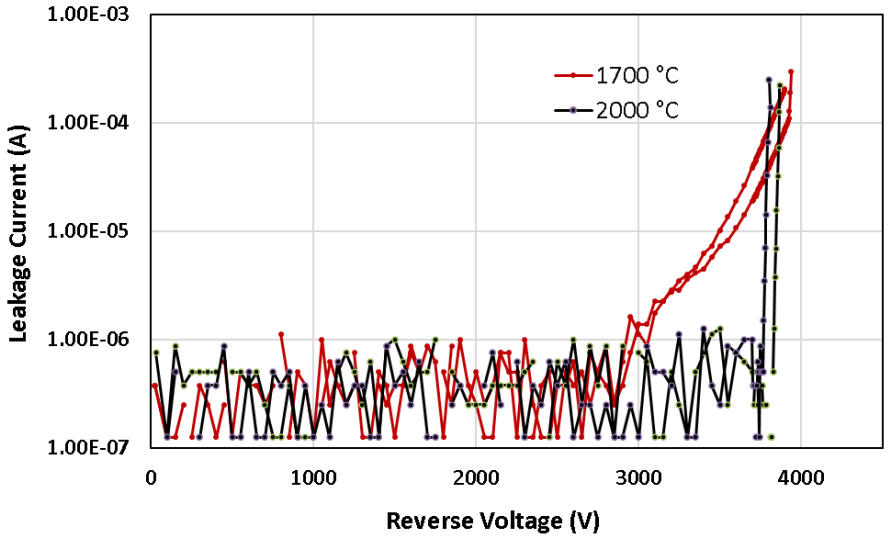
Breakdown Voltage at 15mA/cm²
BV (25 °C) = 3800V

Leakage current density <10 µA/cm² for V_R<3kV

Effect of Activation Anneal Temperature

Deep implantation of Al and N into SiC generates defects due to displacement of SiC atoms.

IV characteristics of SiC SJ-Diodes

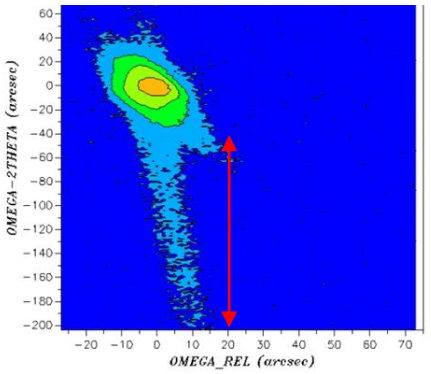


Observable leakage for 1700 °C annealed diodes.

For RT deep implanted SJ devices, standard anneal temperatures is not sufficient in suppressing all the defects.

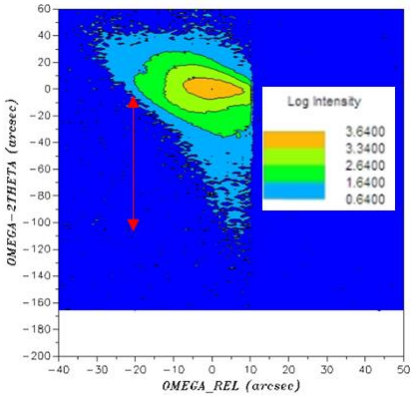
Reciprocal Space maps (RSMs) from SXRCT

1700 °C anneal



$\frac{1}{1000}$ of max intensity: -200 arc sec

2000 °C anneal



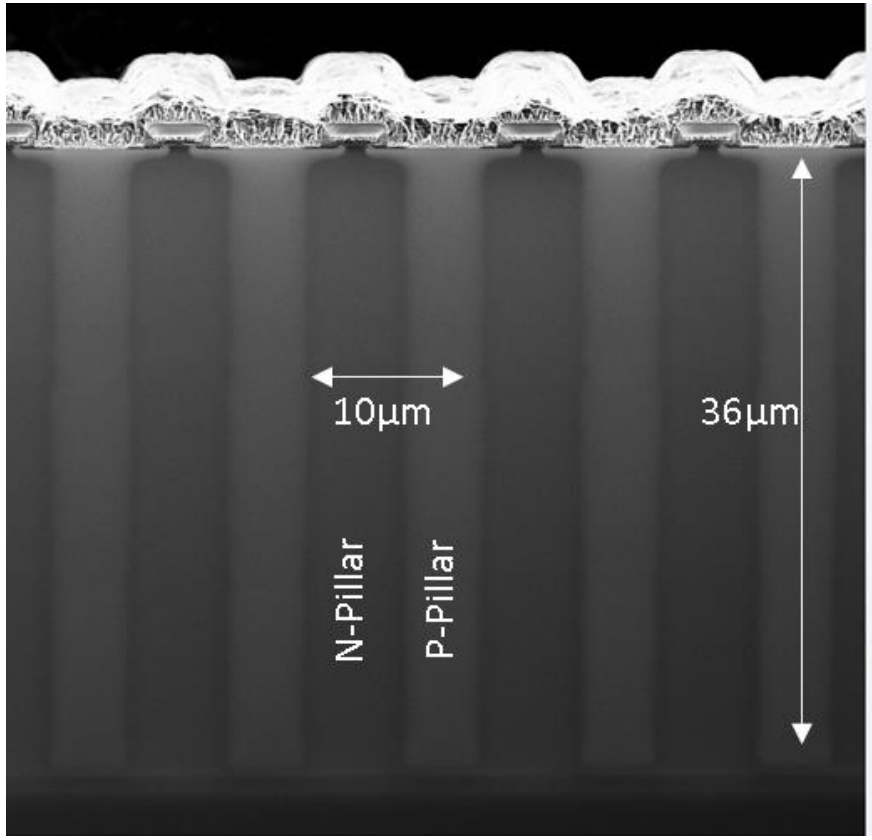
$\frac{1}{1000}$ of max intensity: -130 arc sec

Recovery of major damage at 2000 °C since strain in the samples are nearly uniform.

Z.Chen et.al, ECS Journal of Solid State Science and Technology, Volume 11, Number 6, 2022 (Stony Brook University)

SiC Deep Implanted Super-Junction MOSFETs

GE's 5kV Super-Junction MOSFETs (World's First!)



Epitaxial Over-growth

- Three consecutive epitaxial overgrowth (12µm n-type $1x10^{15}$ cm^{-3})
- Total Drift Layer Thickness 36µm

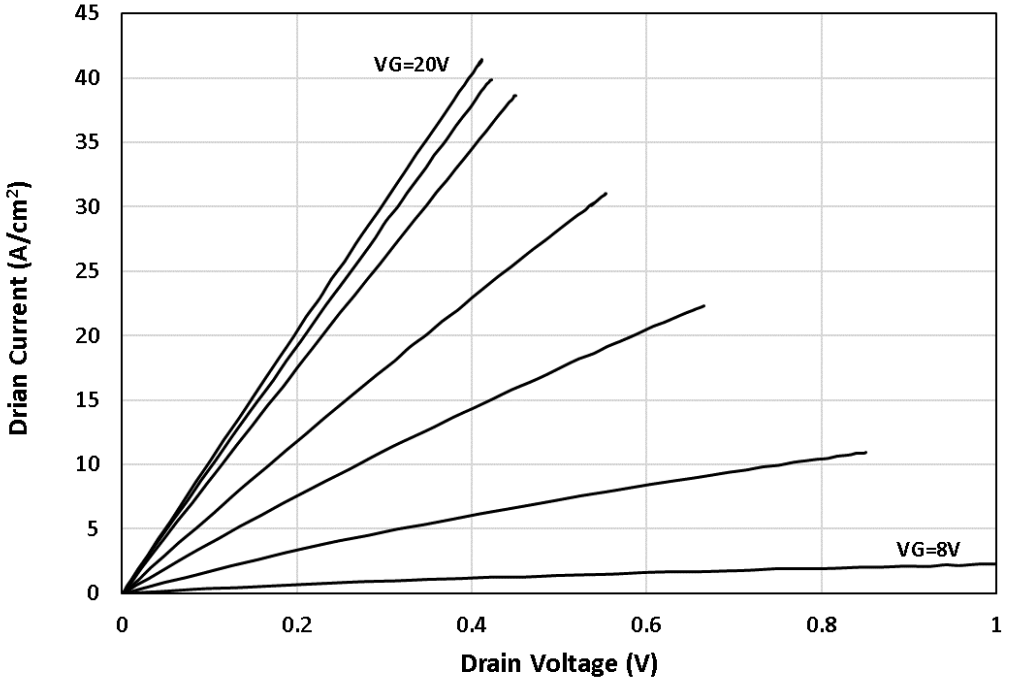
N-doped and P-doped SJ Pillars

- Intermittent vertical P-type and N-type pillars (5µm $1x10^{16}$ cm^{-3})
- Formed using high energy implantation (>20MeV) of Al and N (12um deep)

Top MOSFET Implantation, activation anneal, metallization and surface passivation

SiC Deep Implanted Super-Junction MOSFETs

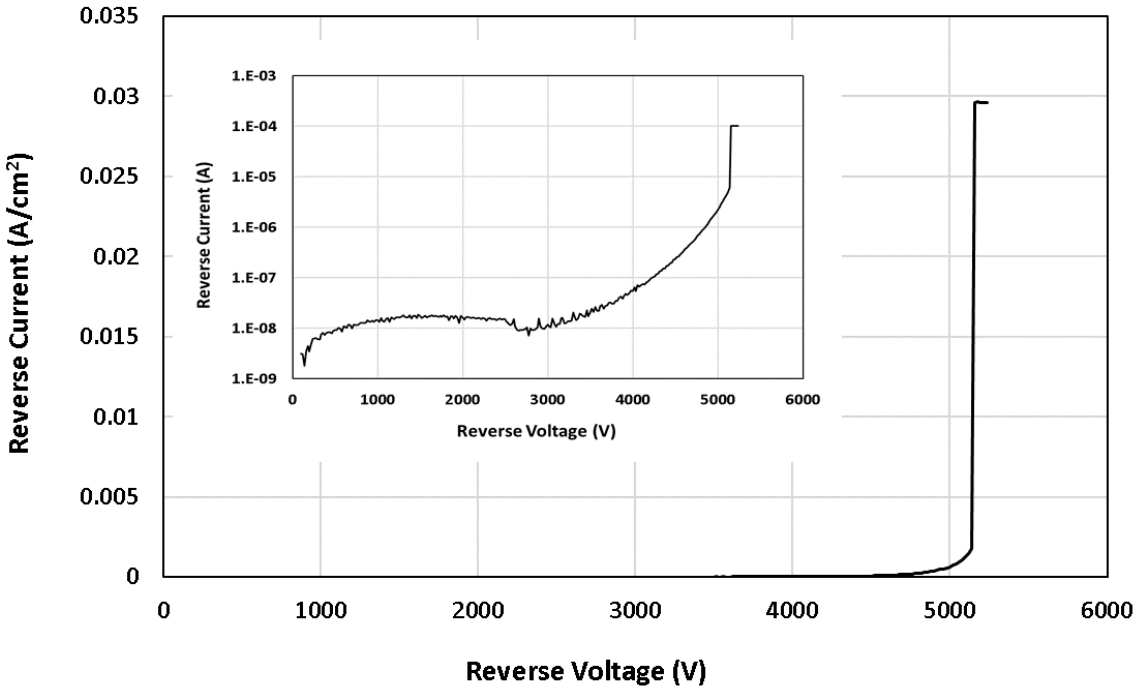
Forward Characteristics



$R_{on,sp}$ (25 °C) = 9 mΩ-cm²

25% improvement from SiC unipolar limit

Reverse Characteristics

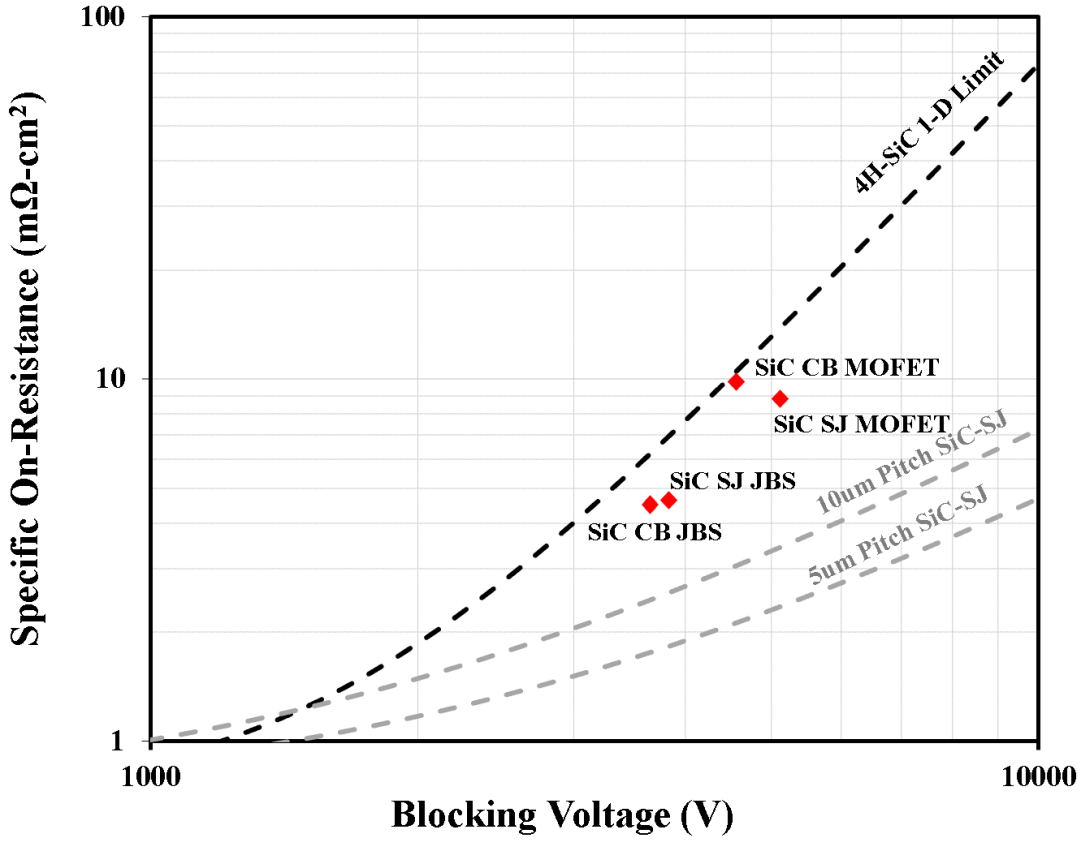


BV (25 °C) = 5100V

Leakage current density <1x10^{-5} A/cm² for V_R<4kV

Summary

- 3kV-5kV SiC Charge-Balanced and Super-Junction devices are breaking unipolar limit .
- Scalable processes and compatible to any other power devices.
- 3.5kV and 5kV deep-implanted SiC SJ JBS diodes and MOSFETs were successfully prototyped.
- High energy implantation of SiC require higher than typical anneal temperatures to suppress most of the defects.



Acknowledgment

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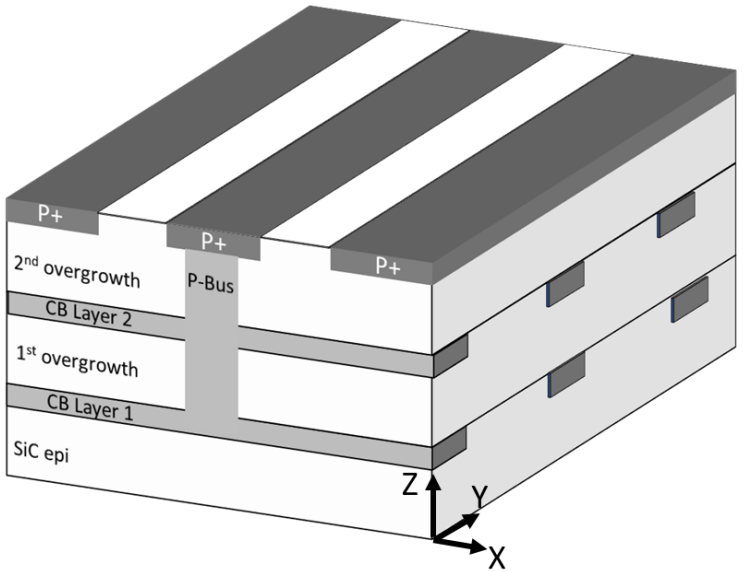
Backup Slides

SiC Charge-Balanced (CB) Technology

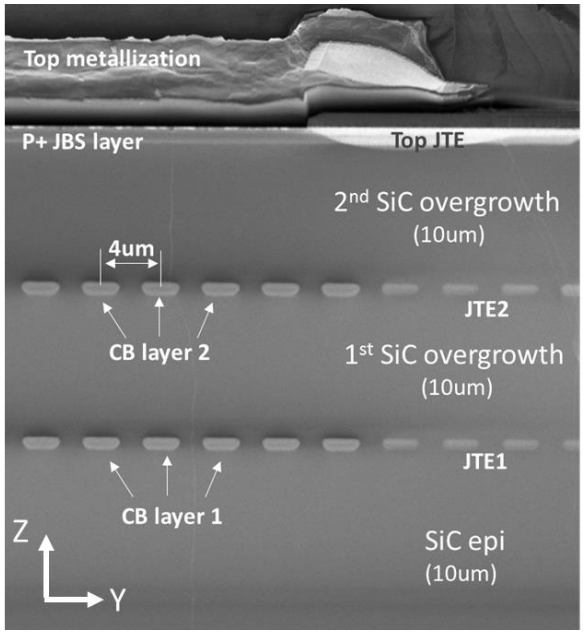
3kV SiC CB JBS Diode

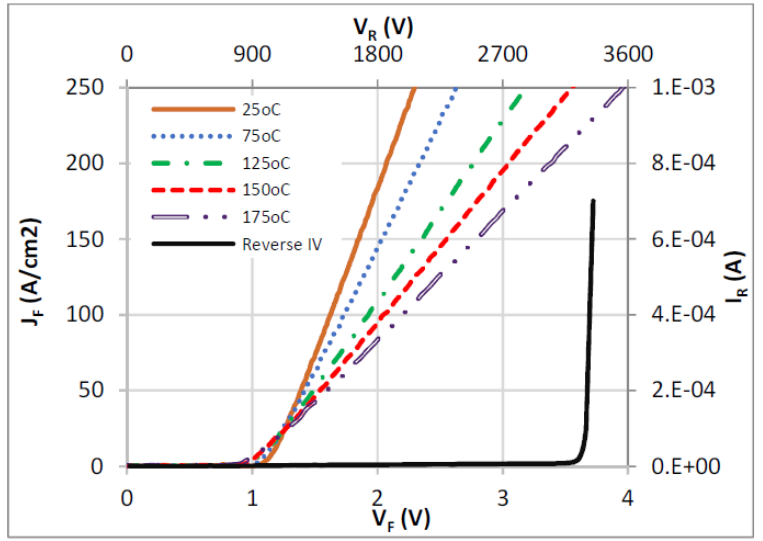
3D Perspective View



CB Drift layer and standard JBS on the top

Cross Sectional SEM View





3.3kV JBS diode:
$R_{on,sp}$ (RT) = 4.3 mΩ-cm²
$R_{on,sp}$ (150 °C) = 9.9 mΩ-cm²

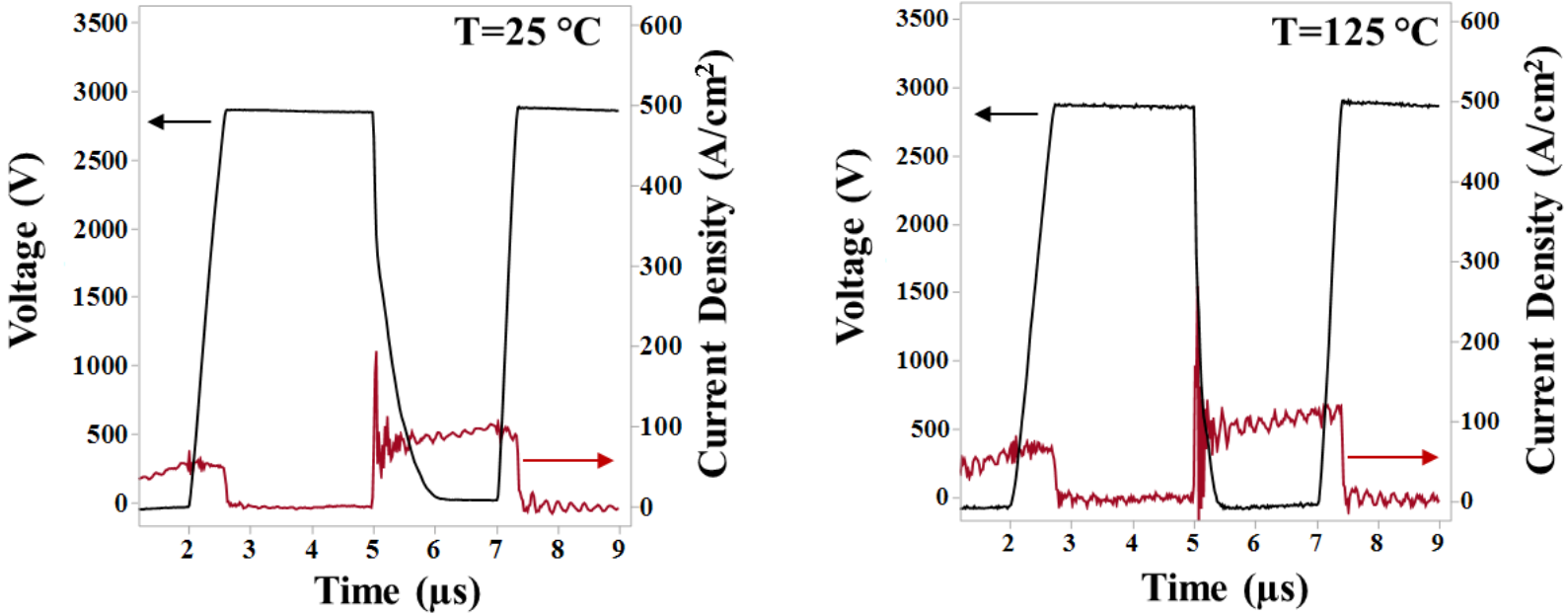
40% improvement from SiC unipolar limit

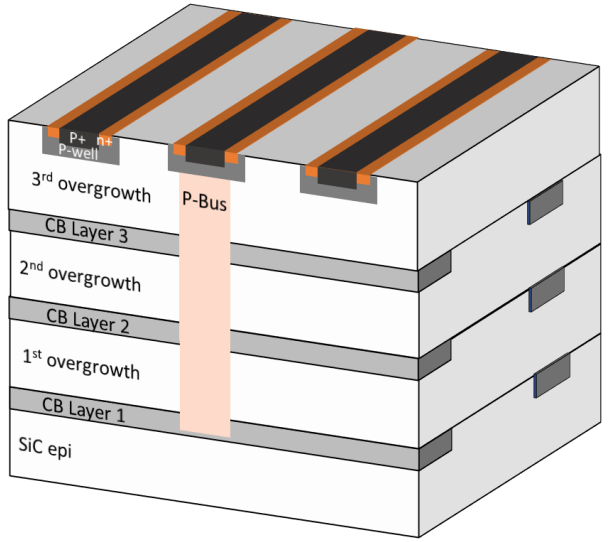
R. Ghandi et.al, 2019 ISPSD pp. 179-182 .

CB MOSFET Dynamic Characteristics

Double-pulse inductive switching

2.8kV and 500A/cm^2





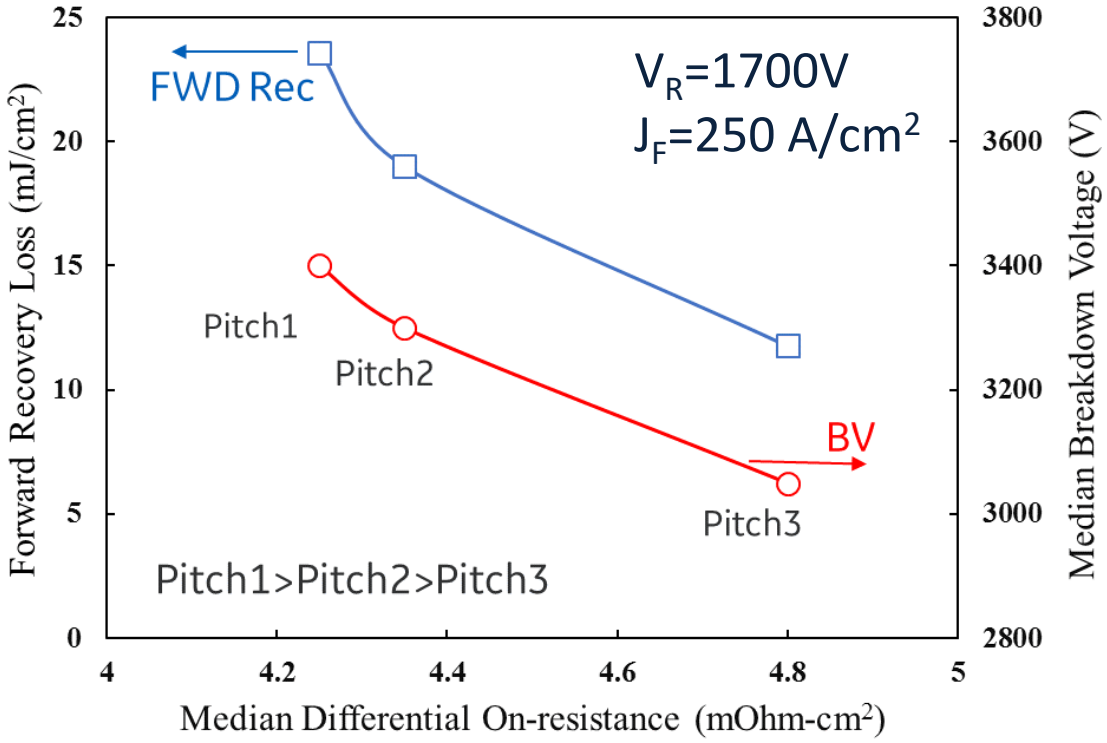
- Noticeable turn-on delay (forward recovery loss) at room temperature
  - Charge transitions delay from top source contacts to buried CB regions
- The delay is dependent on the resistance of P-Bus pillar
  - Significantly improved at higher temperatures (higher ionization rate)

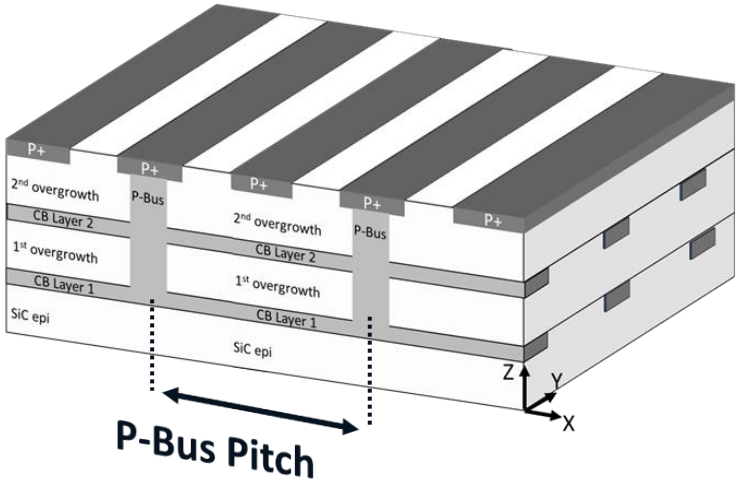
Total Switching loss at 2.8kV and 50A/cm^2
E_{Total} (RT) = 110 mJ/cm^2
E_{Total} (125 °C) = 95 mJ/cm^2

70% improvement from 4.5kV Si IGBT[1]
[1]5SMY 12L4500 ABB Datasheet

Improved Dynamic Characteristics

P-Bus design trade-off vs. switching loss ($E_{Fwd,rec}$) in CB Diodes

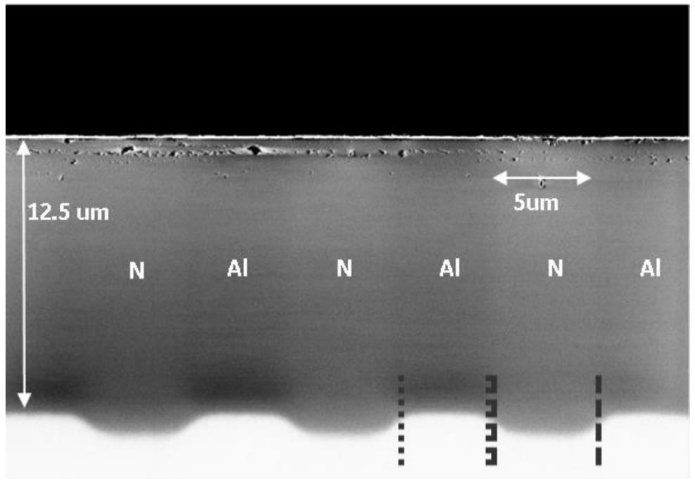


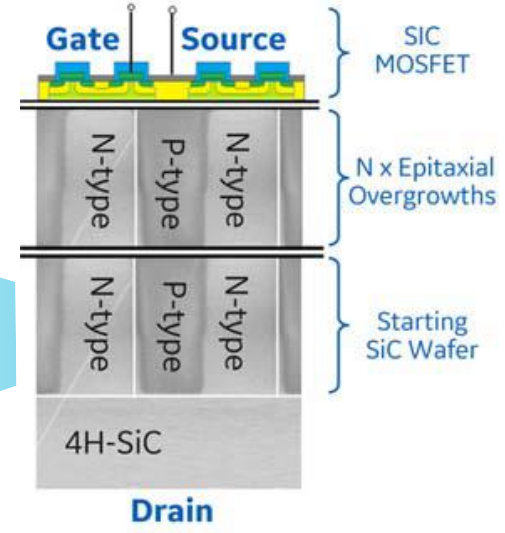


- ~40% improvement in forward recovery loss by implementing smaller P-Bus pitch.
- However, results in 12% higher differential on-resistance (smaller active area) and 15% decrease in breakdown voltage.

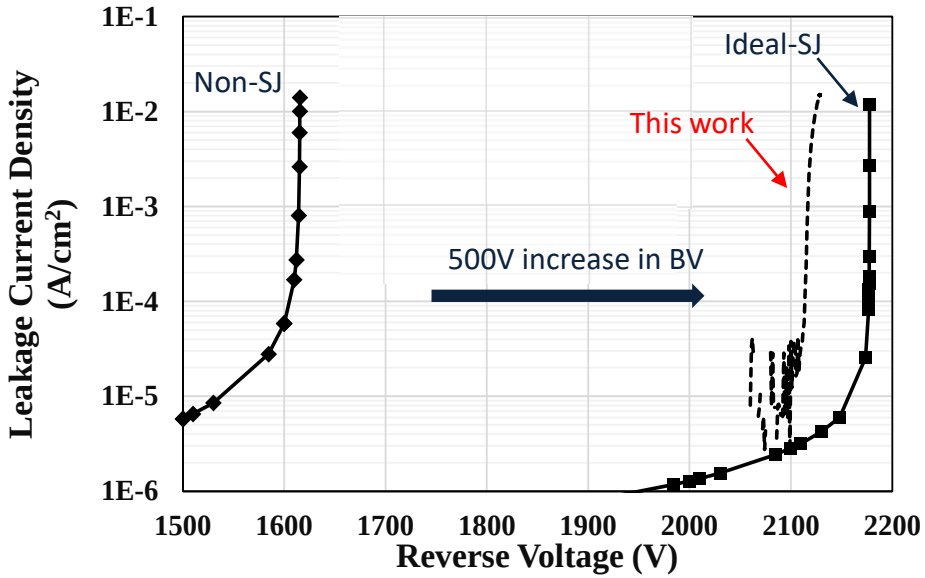
Demonstration of 2kV SiC SJ PiN Diodes

Deep implanted P/N pillars formed on a SiC wafer





Reverse IV characteristics of SiC SJ-PiN diodes

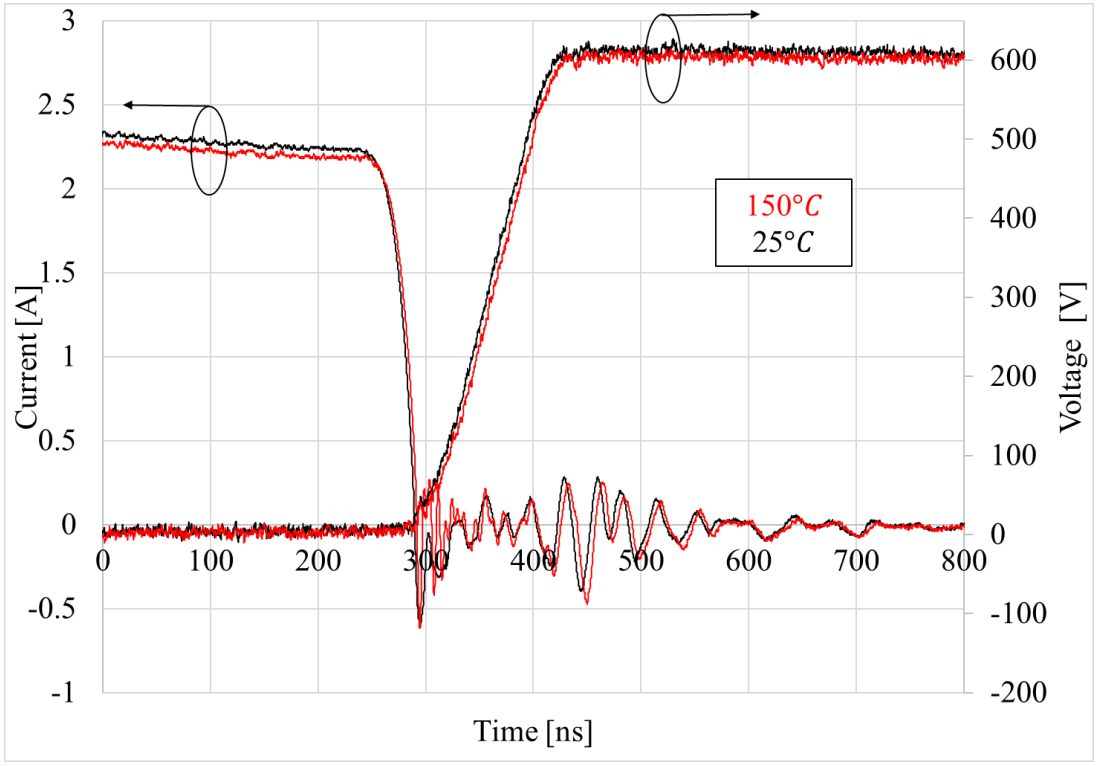


- High-energy implanted, single layer 2kV SiC SJ PiN diodes were fabricated as a first building block of deep-implanted SJ technology.
- SJ diodes result in breakdown voltages of >2100V (500V higher than the non-SJ diodes)[1]

[1]R. Ghandi, et.al, Mater. Sci. Forum, vol. 1062, pp. 477–481, 2022.

3.5kV SiC Deep Implanted Super-Junction JBS Diode

Reverse Recovery Characteristics
(450A/cm^2 and 600V)



- Fast recovery SiC SJ JBS diode.
- No change in the turn-off current and voltage waveforms from room temperature to 150°C
- Total capacitive charge is estimated to <700 nC/cm^2.