UNIVERSITY OF
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VCSELs on Silicon

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Dr. John Dallesasse Research Group

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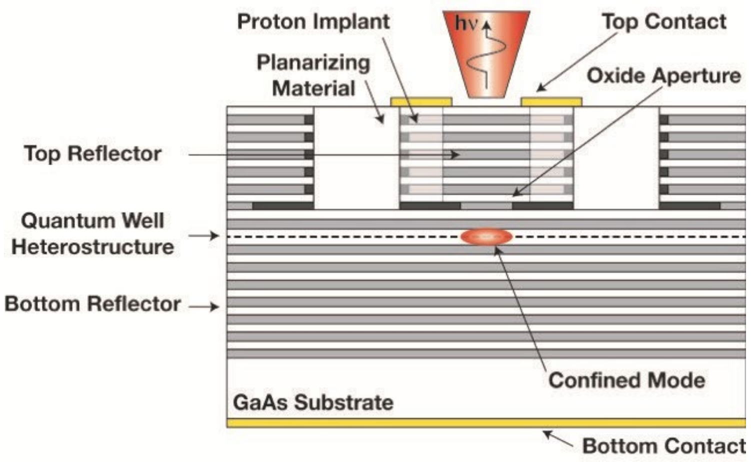
Outline

VCSELs on Silicon

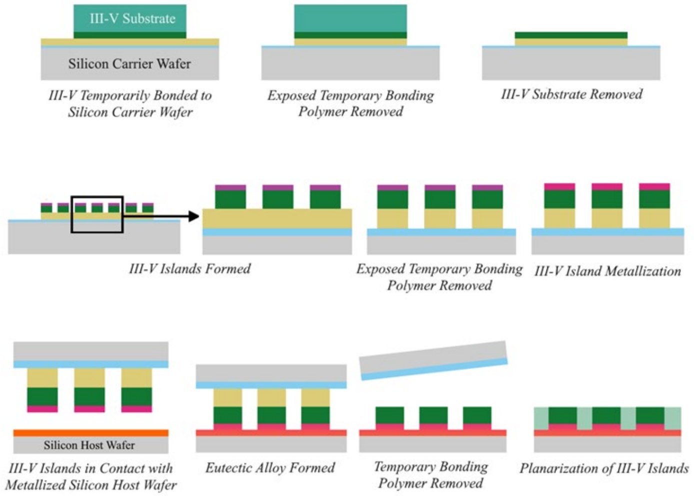
Introduction

- VCSELs
- Integration



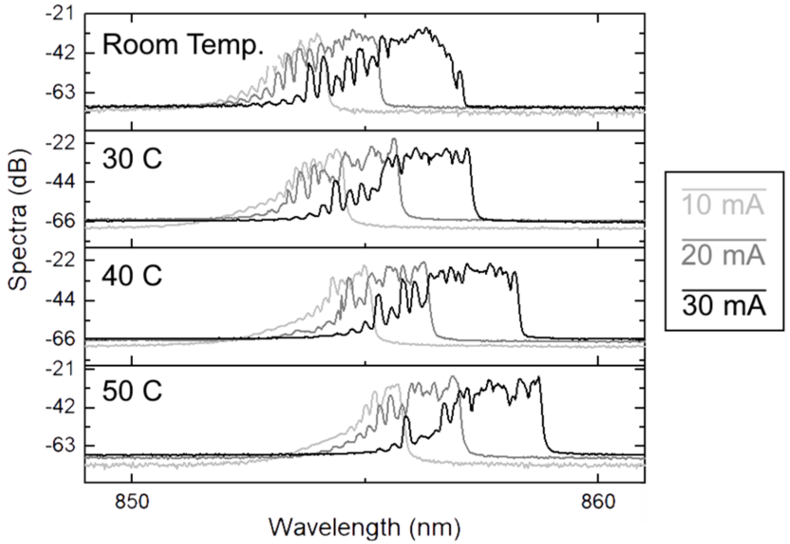
Process

- Integration method
- VCSEL design

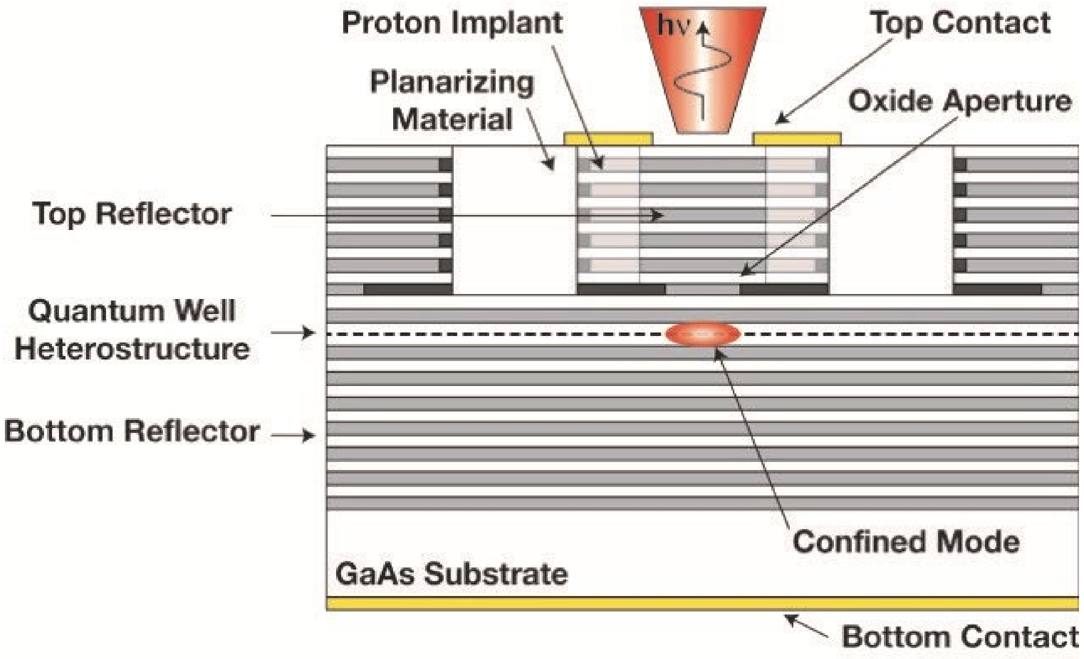


Performance

- Reduced spectral shift
- L-I-V



Why do we care about VCSELs?



“Vertical Cavity Surface Emitting Laser”

- Small footprint
- Monolithic fabrication (no cleaving!)
  - Distributed Bragg Reflectors (DBRs) act as mirrors
- Circular beam profile
- Low threshold current
- Single transverse mode*

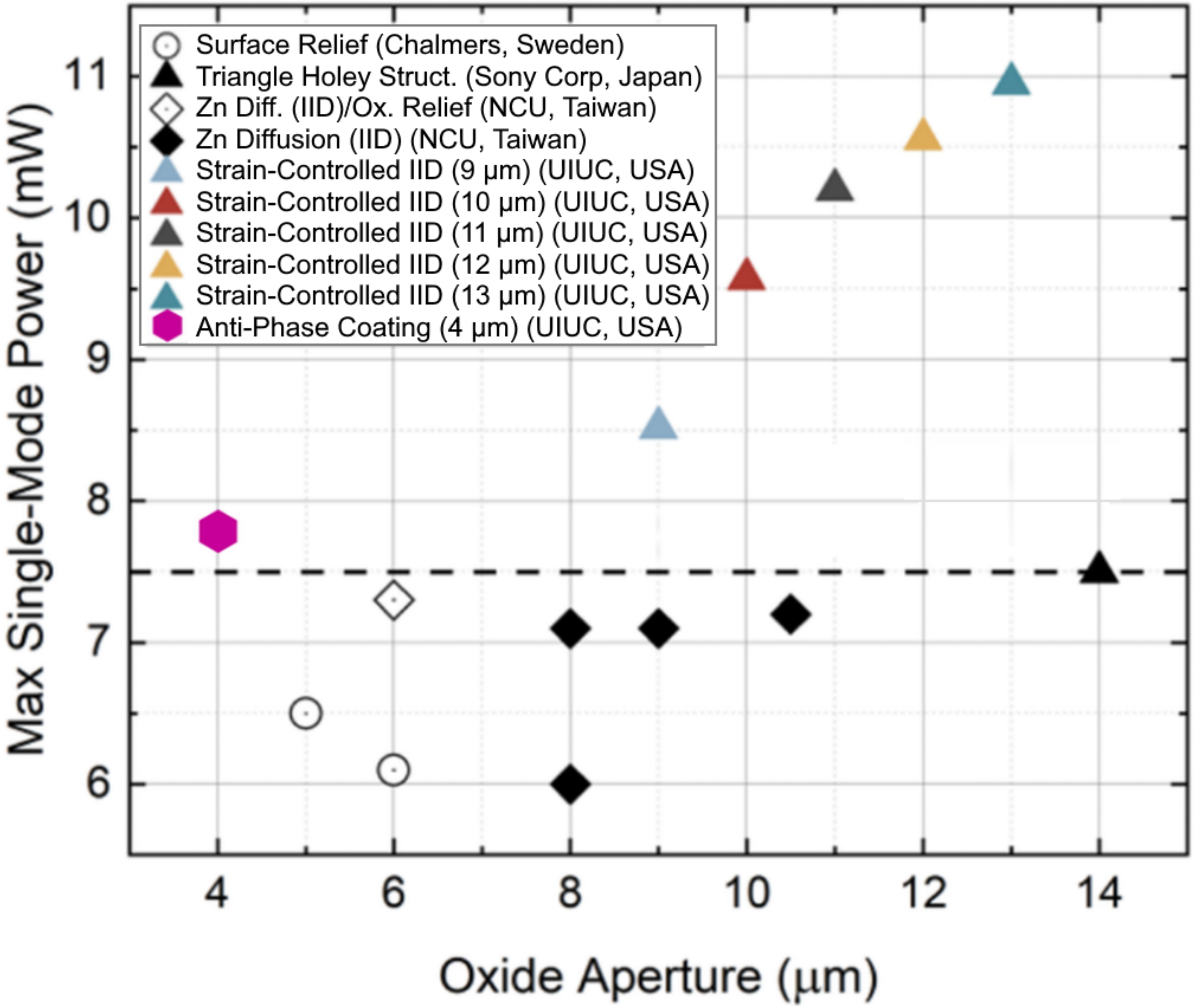
Common Applications

- LIDAR
- Facial recognition
- Optic communication

What we do with VCSELs

Dallesasse Group at UIUC

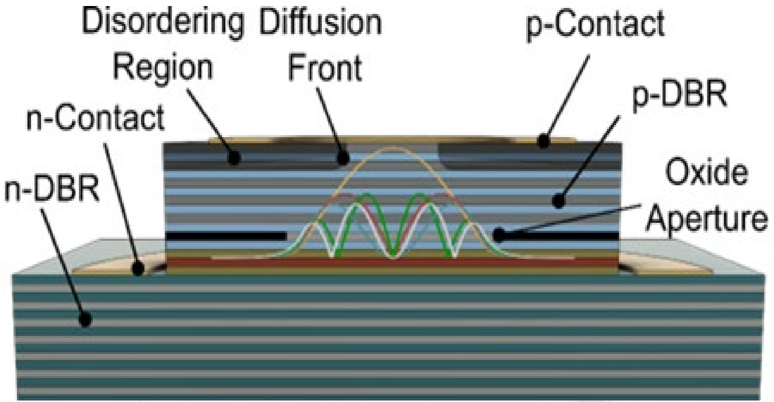
- High-power single-mode VCSELs
  - Impurity-induced disordering (IID)
  - Anti-phase coating
- Single-polarization VCSELs
  - Elliptical IID aperture
- **VCSELs on Silicon**
  - Epitaxial transfer integration

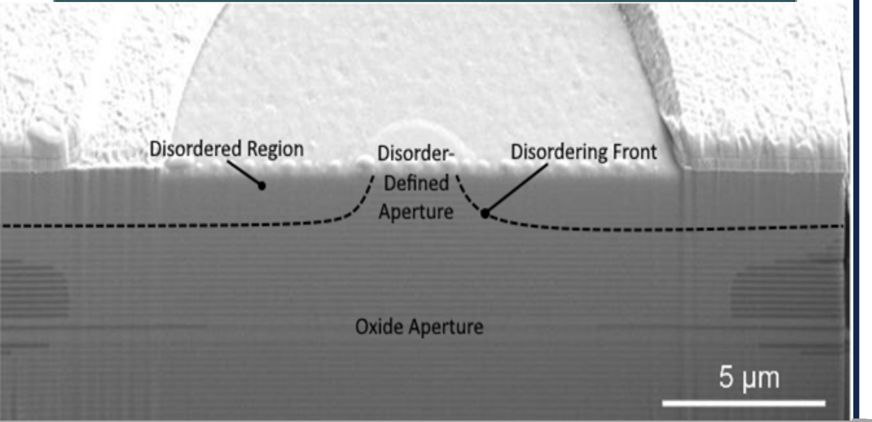


Our Other VCSEL Projects - Overview

High-Power Single-Mode *(Impurity-Induced Disordering)*

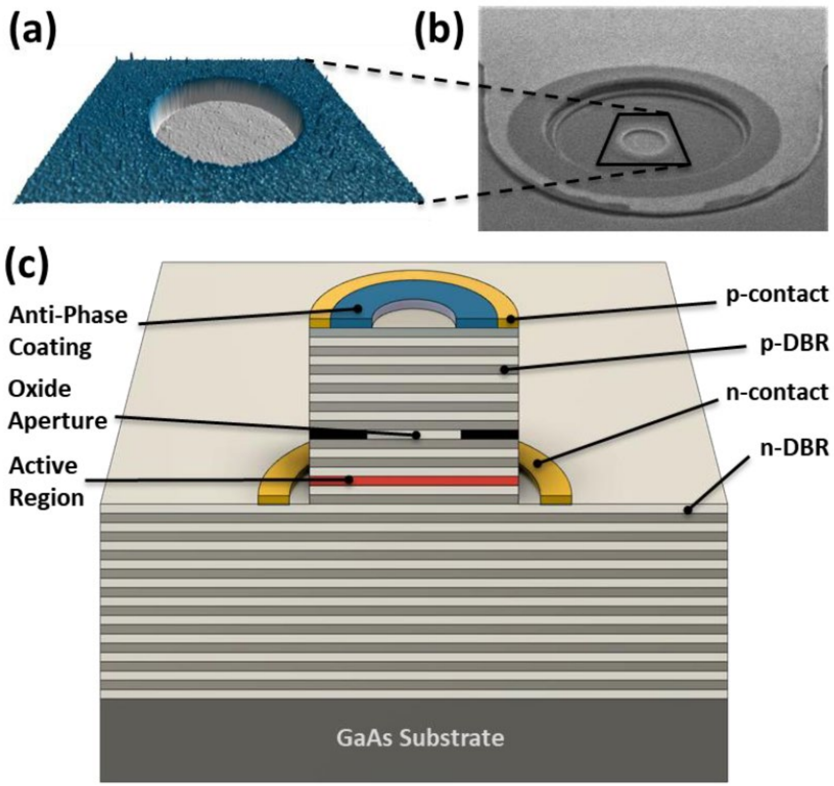
- **Record single-mode power**
- Reduced differential resistance





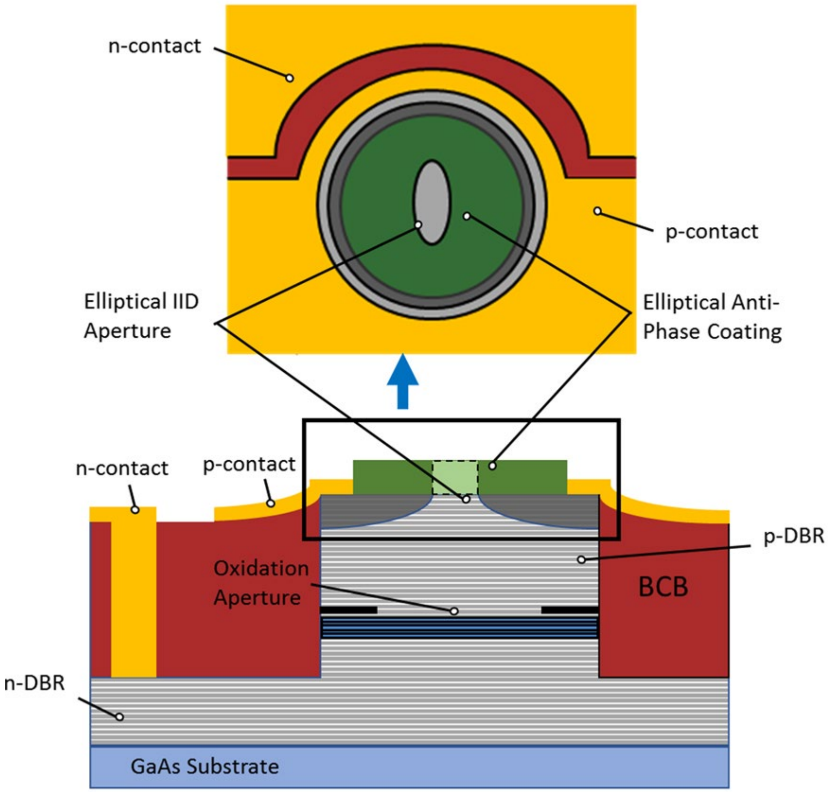
High-Power Single-Mode *(Anti-Phase Coating)*

- High single-mode power
- **Wafer-scale process**



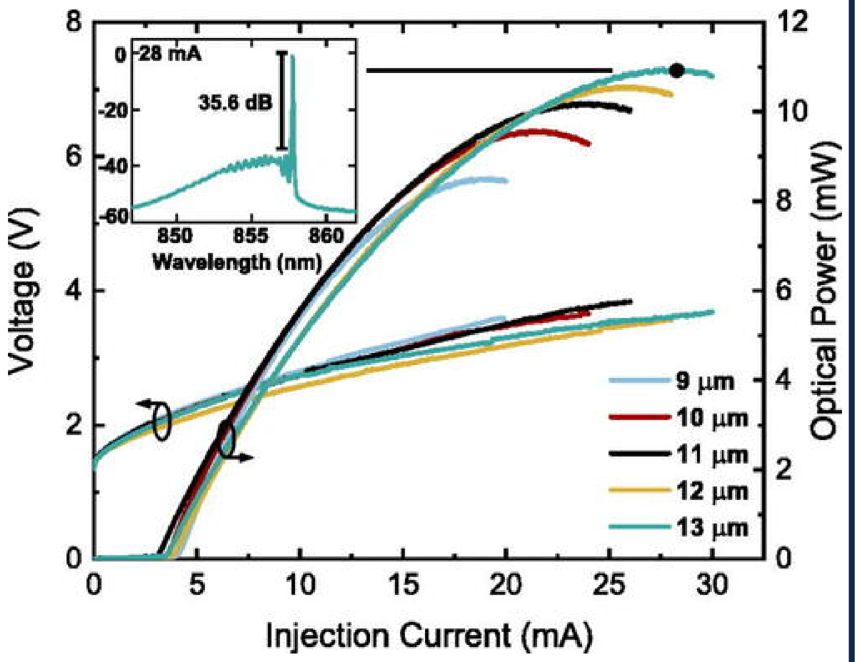
Single-Polarization

- Elliptical IID Apertures
  - **OPSR > 19 dB** for 9x8 and 9x7 μm IID apertures
  - Major ellipticity degrades total output power and thus OPSR



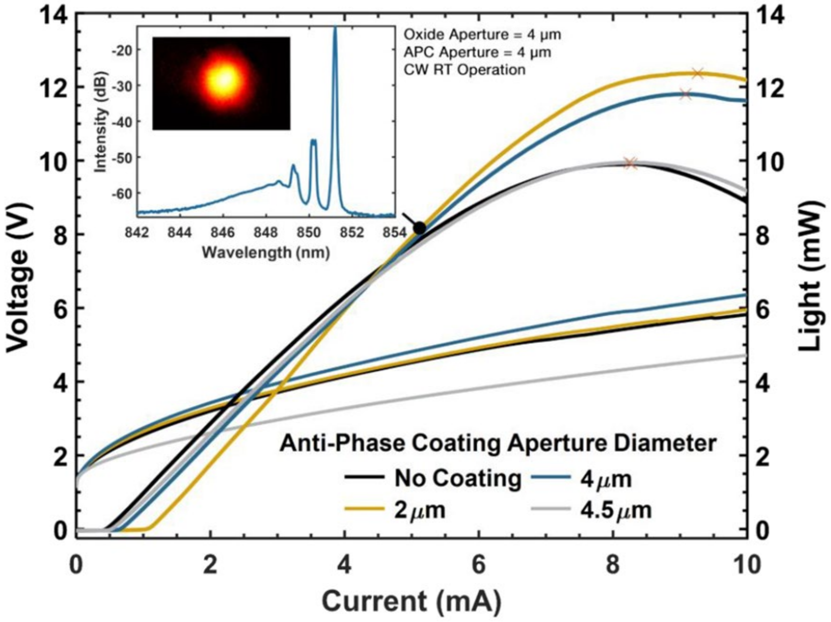
Our Other VCSEL Projects - Data

High-Power Single-Mode *(Impurity-Induced Disordering)*



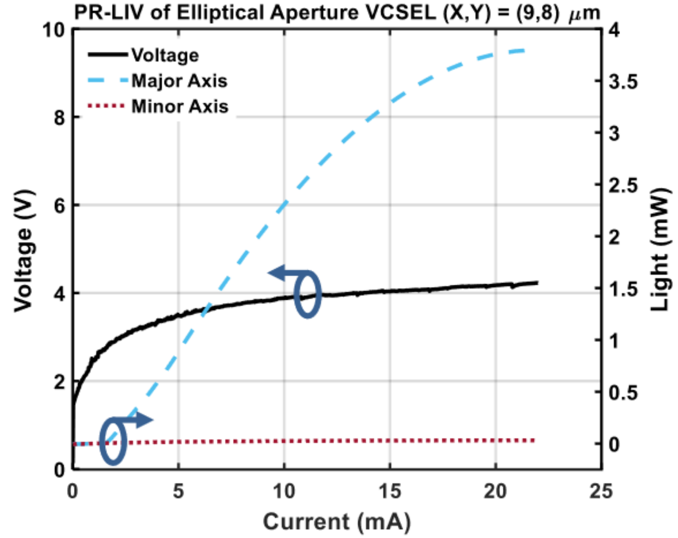
Published: P. Su, K. P. Pikul, M. D. Kraman, and J. M. Dallesasse, “High-power single-mode vertical-cavity surface-emitting lasers using strain-controlled disorder-defined apertures,” Appl. Phys. Lett., vol. 119, no. 24, p. 241101, 2021.

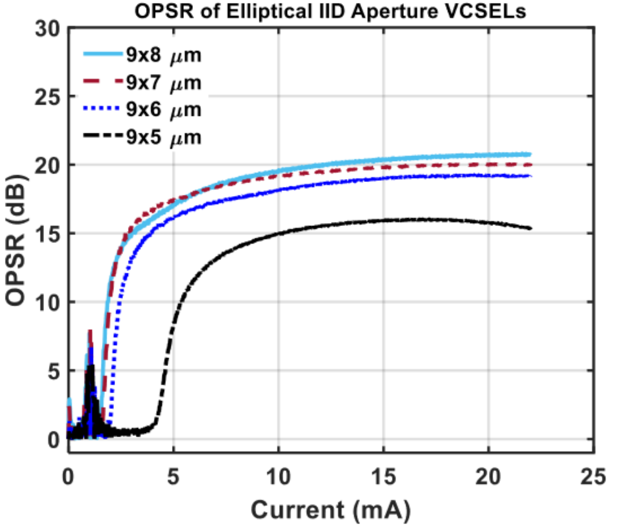
High-Power Single-Mode *(Anti-Phase Coating)*



Publication In-Progress: K. P. Pikul, P. Su, M. D. Kraman, B. A. Kesler, and J. M. Dallesasse, “Utilization of Silicon Anti-Phase Optical Coatings for Transverse-Mode Control in High-Power Oxide-Confined Vertical-Cavity Surface-Emitting Lasers”

Single-Polarization





VCSELs on Silicon: Why Integrate?

Silicon device integration

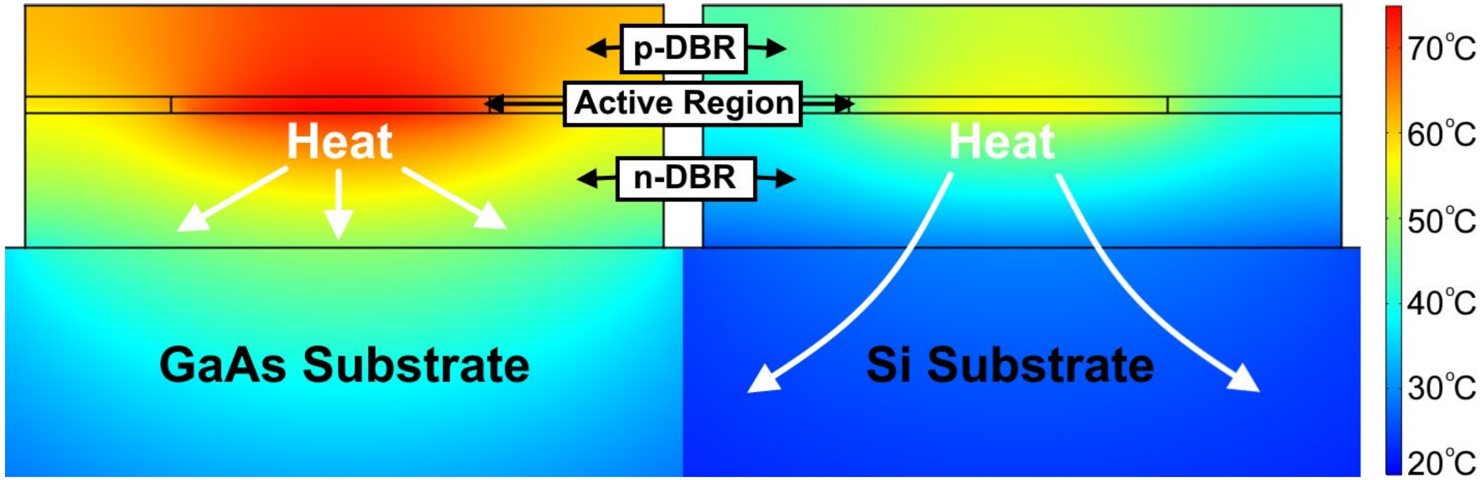
- CMOS imaging arrays
  - LIDAR
  - Facial recognition

Remove chip-to-chip interconnects

- Reduce package size
- Improve performance

Improve thermal pathway

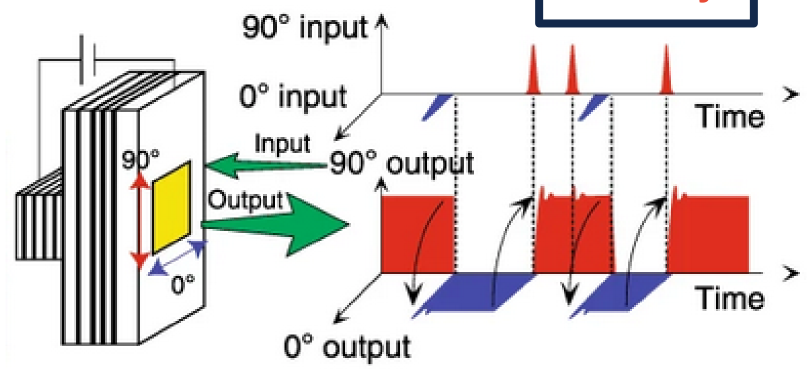
- Reduce power droop
- Improve reliability



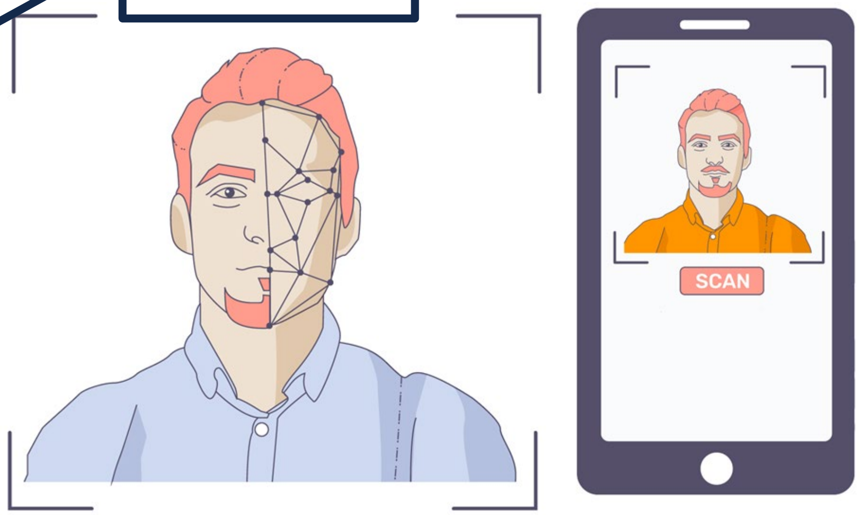
Top Image Source: https://eom.umicore.com/en/germanium-solutions/markets/vcsels/

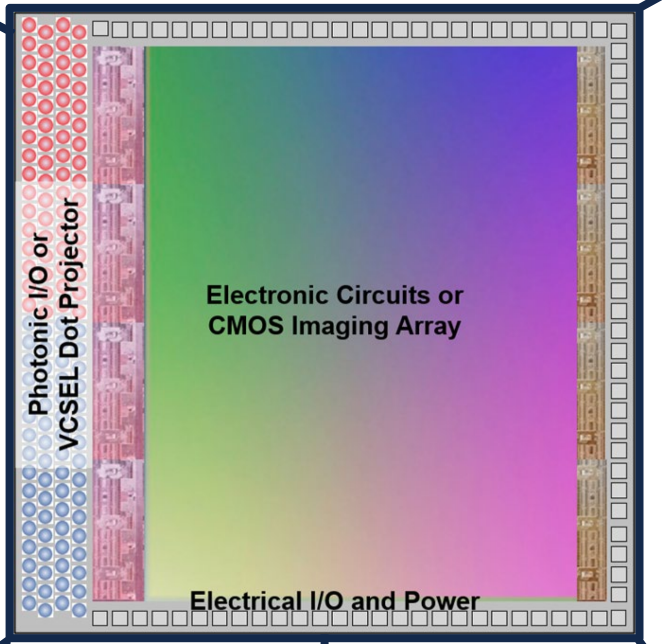
Applications for VCSELs on Silicon

Optical Memory

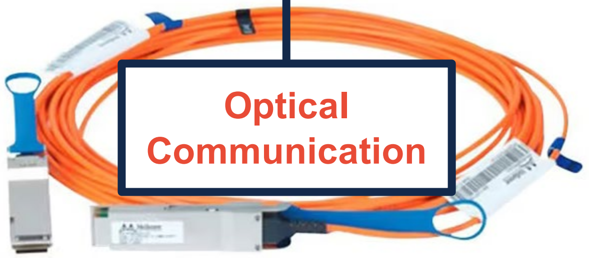


Facial Recognition

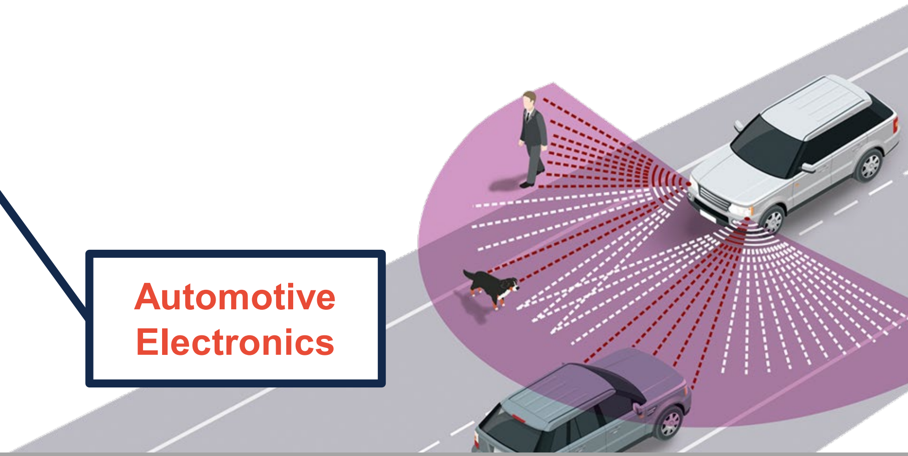




Laser Printer



Optical Communication



Automotive Electronics

Traditional Integration Method: Flip-Chip

Solder Bumps Attach III-V Device to Silicon

- Selectively integrate known-good die
- Alignment of devices restricted to precision of pick-and-place tool
- Worse thermal pathway
  - Worse performance than non-integrated

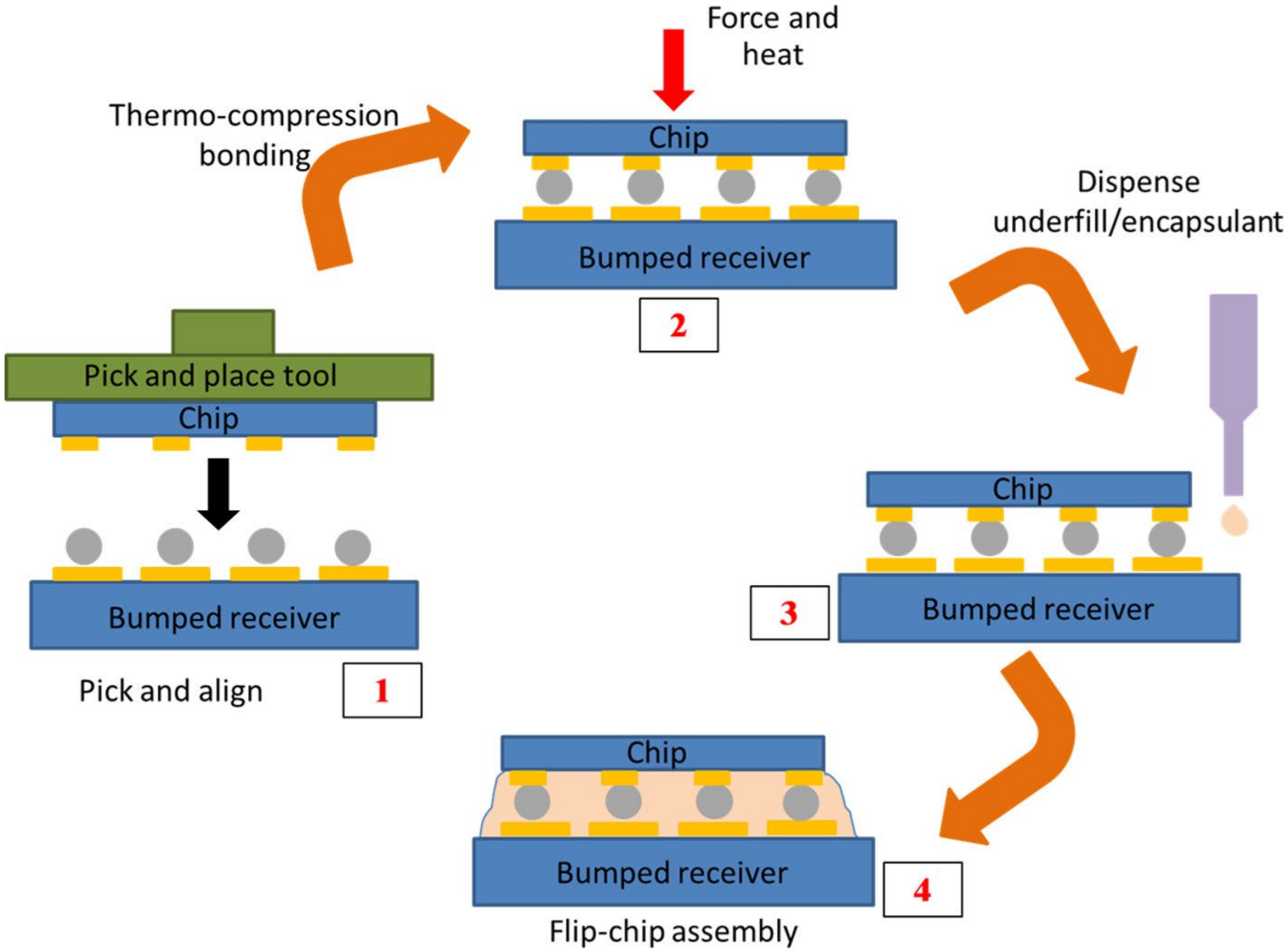
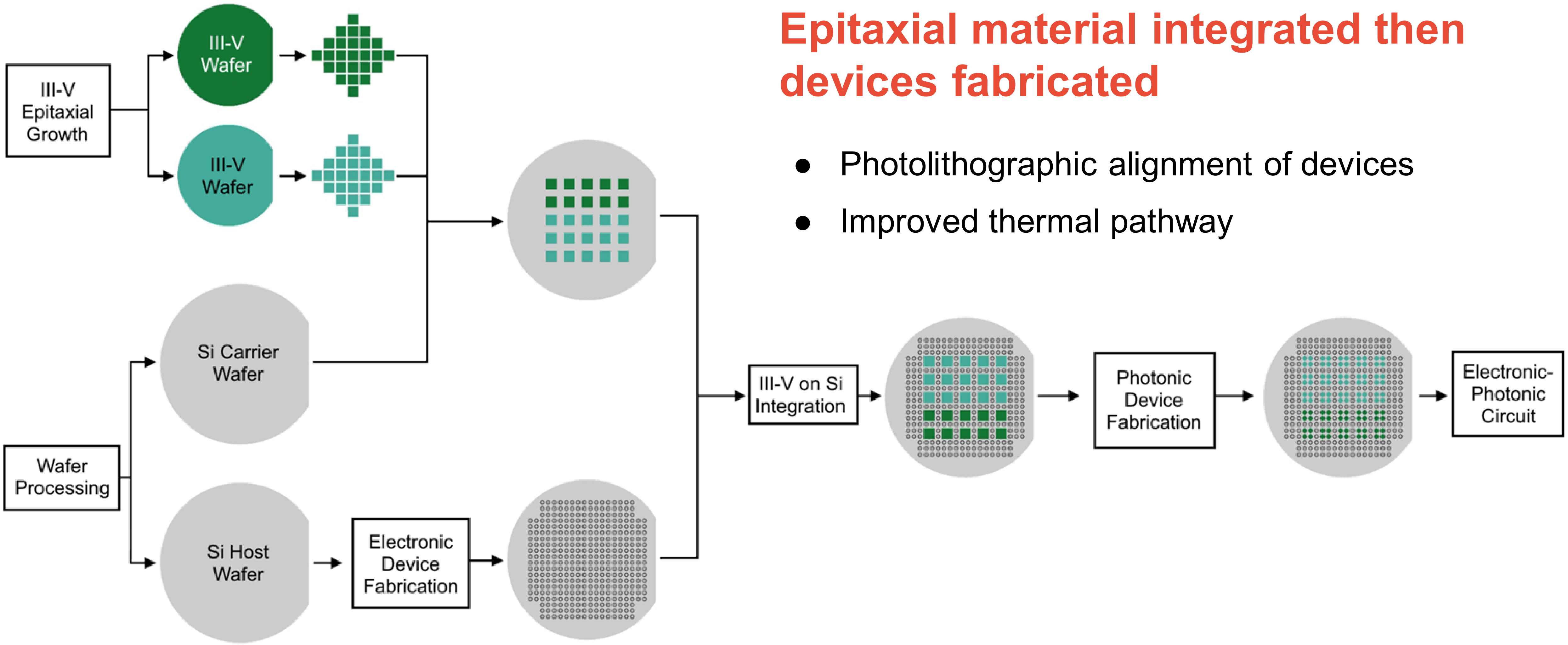


Image Source: Kaur, Kamal S., and Geert Van Steenberge. "Laser-induced forward transfer for flip-chip packaging of single dies." JoVE (Journal of Visualized Experiments) 97 (2015): e52623

Epitaxial Transfer Solves Issues of Flip-Chip Integration



Epitaxial material integrated then devices fabricated

- Photolithographic alignment of devices
- Improved thermal pathway

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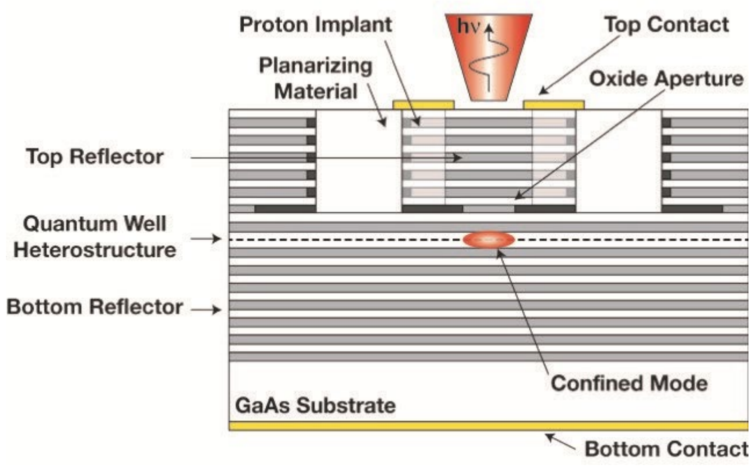
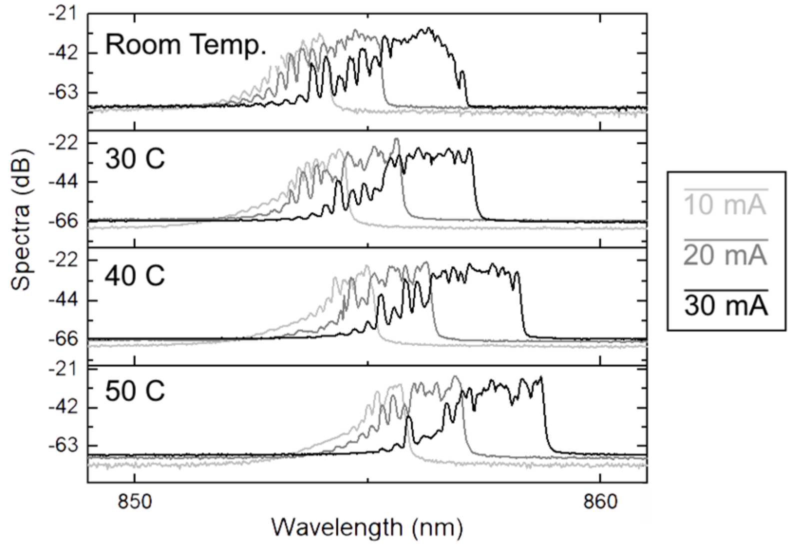


Process

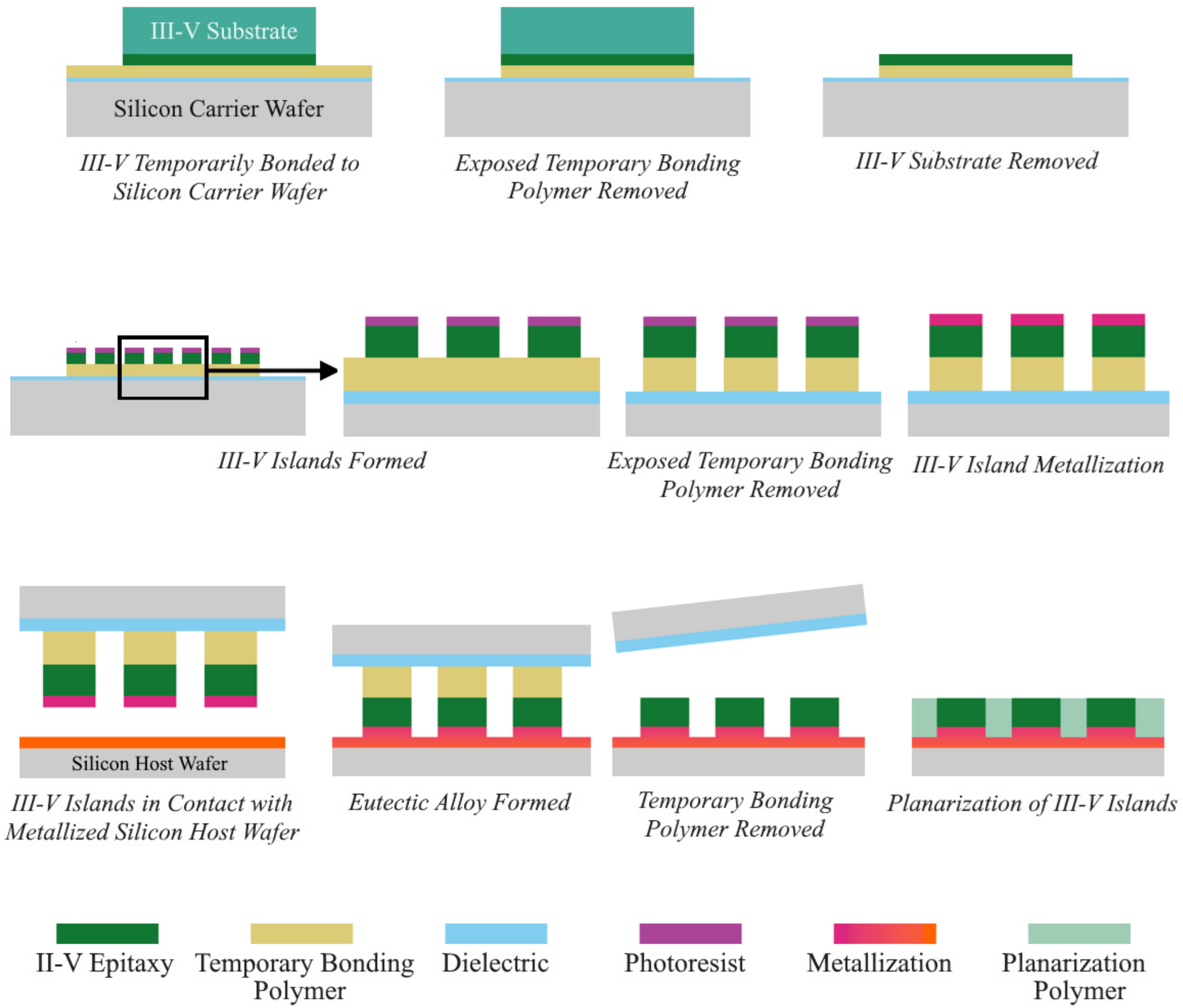
- Integration method
- VCSEL design

Performance

- Reduced spectral shift
- L-I-V



Integration via Epitaxial Transfer



1. **Substrate Removal**
2. **Island Definition**
3. **Eutectic Bonding**

1. Substrate Removal

- 🟩 *III-V Epitaxy*
- 🟨 *Temporary Bonding Polymer*
- 🟦 *Dielectric*
- 🟪 *Photoresist*
- 🟥 *Metallization*
- 🟩 *Planarization Polymer*

a. Temporarily bond III-V epitaxial-side-down to silicon carrier wafer

b. Remove excess polymer

c. Remove Substrate

2. Island Definition

🟩 *III-V Epitaxy*

🟨 *Temporary Bonding Polymer*

🟦 *Dielectric*

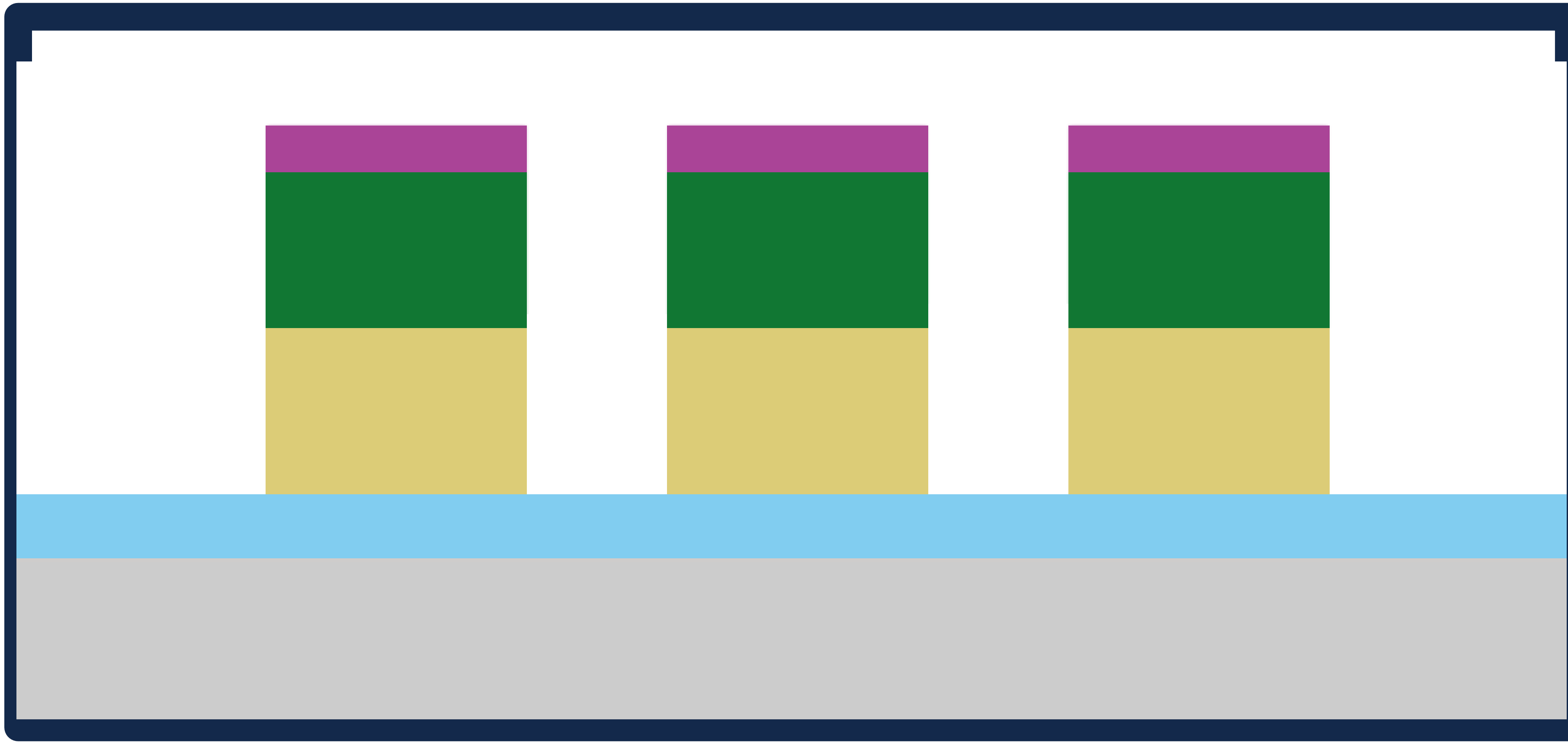
🟪 *Photoresist*

🟧 *Metallization*

🟩 *Planarization Polymer*

a. Mesa etch

b. Excess polymer removal



3. Eutectic Bonding

🟩 *III-V Epitaxy*

🟨 *Temporary Bonding Polymer*

🟦 *Dielectric*

🟪 *Photoresist*

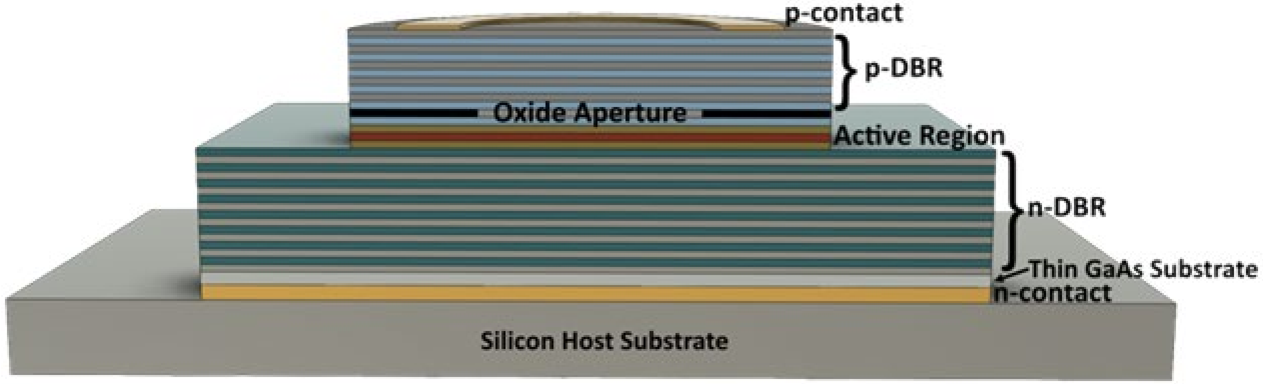
🟥 *Metallization*

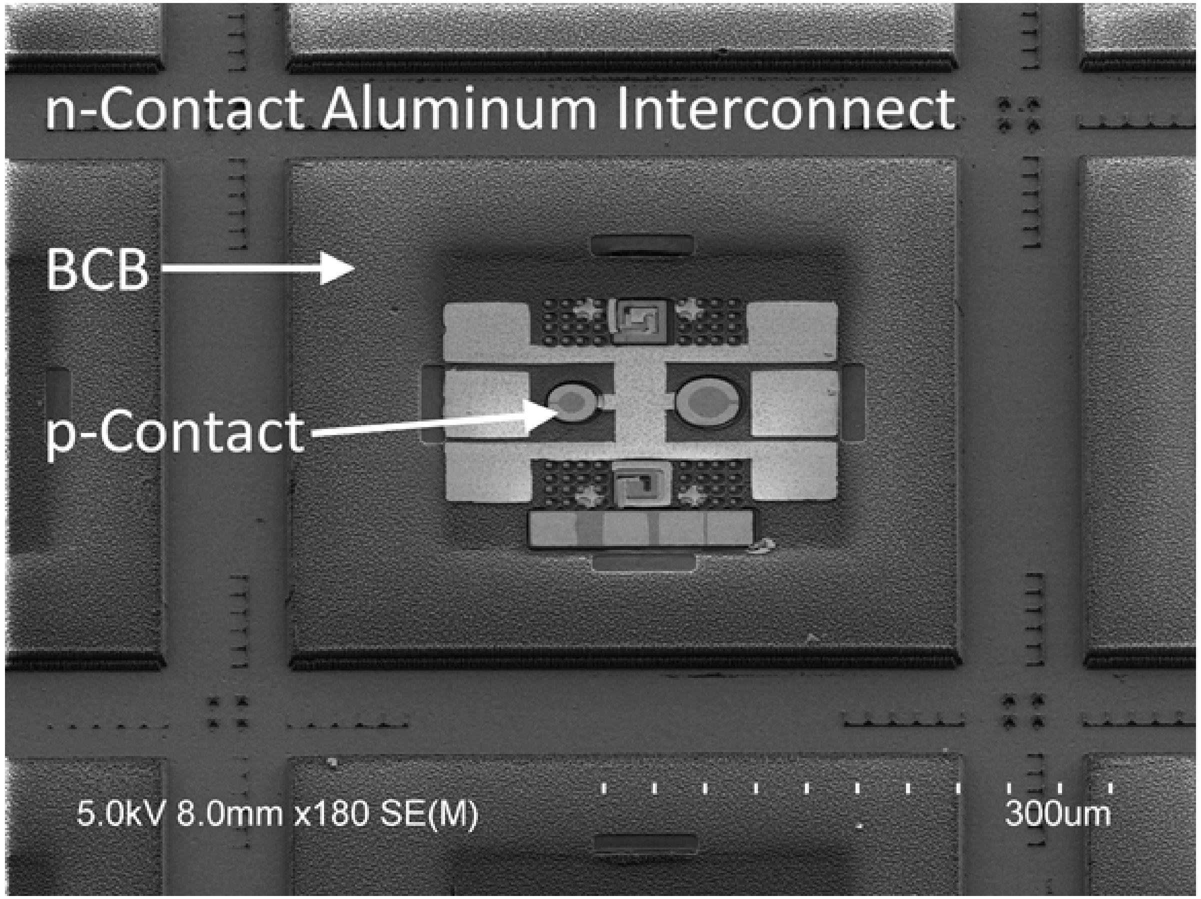
🟩 *Planarization Polymer*

a. Ohmic contact deposition
b. Metallization of silicon host wafer
c. Permanent bonding via eutectic alloy
d. Polymer dissolved
e. Planarization
➢ Device fabrication

Integrated VCSEL Structure

10 µm Oxide-Aperture, AlGaAs-based VCSEL





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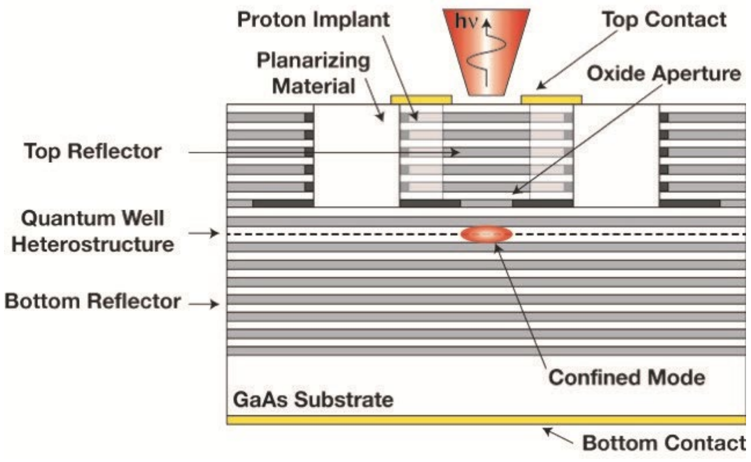
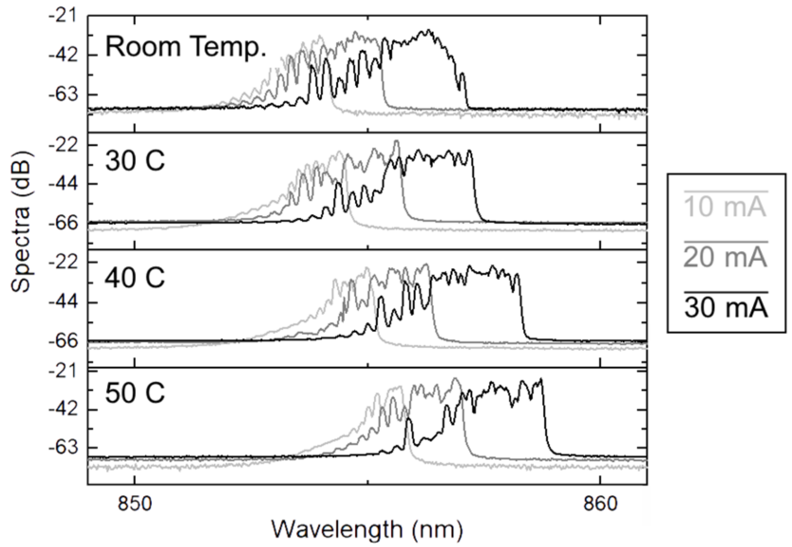


Process

- Integration method
- VCSEL design

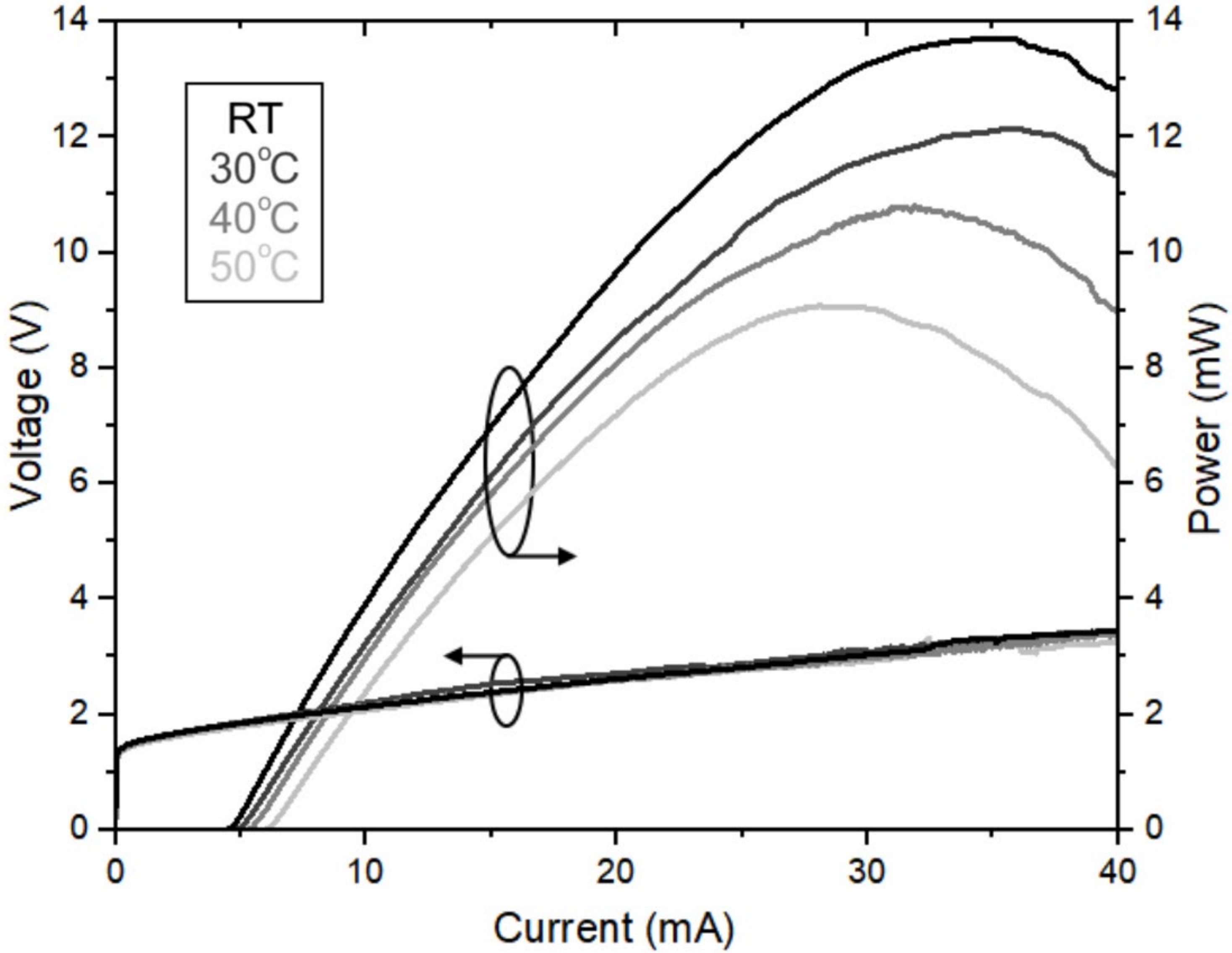
Performance

- Reduced spectral shift
- L-I-V



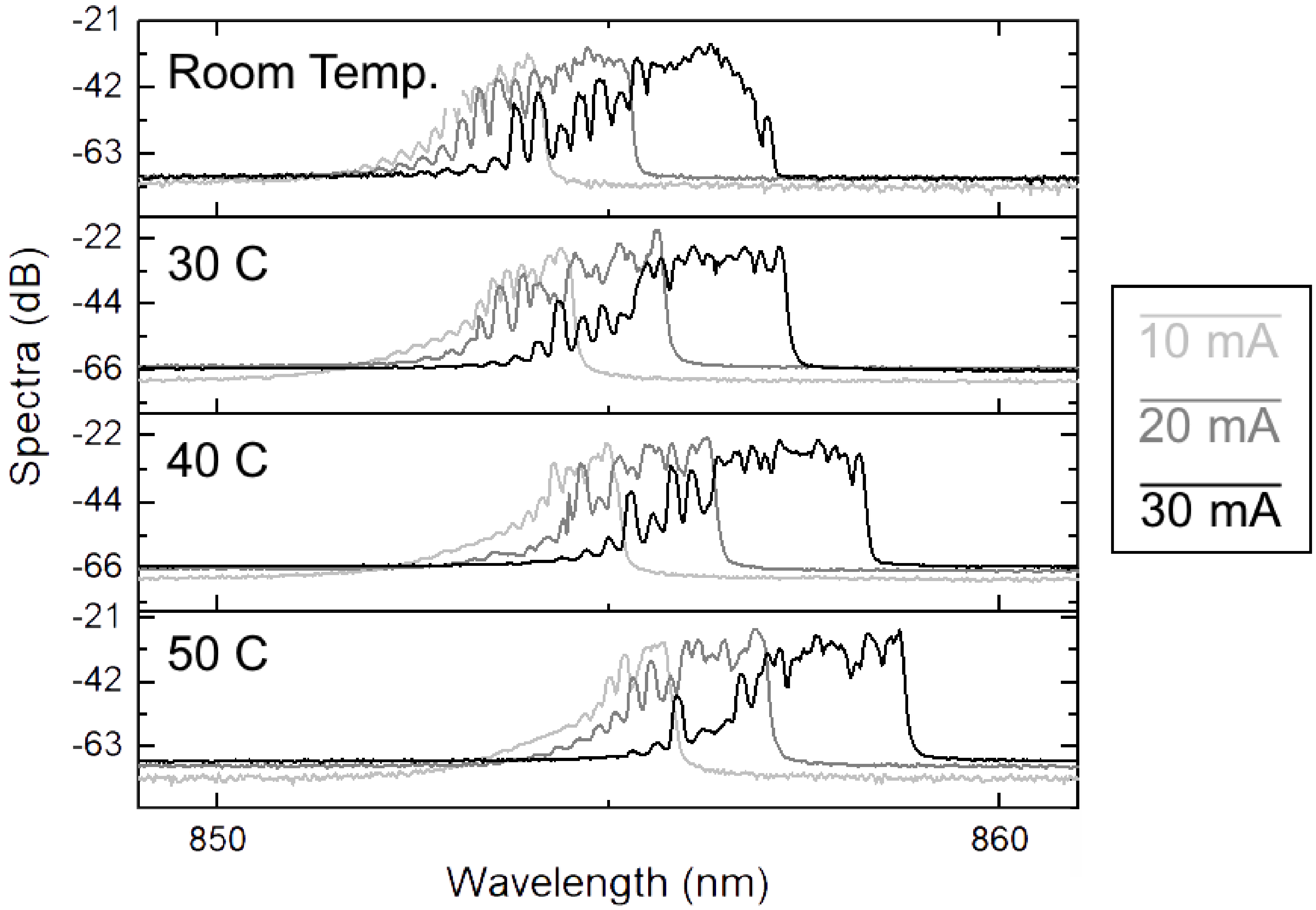
Integrated VCSEL Performance: 13.8 mW Max Power

- **L-I-V (CW)**
- Spectral Shift (Redshift)
- Thermal Resistance (R_{th})
- R_{th} vs literature



Integrated VCSEL Performance: **~0.15 nm/mA** Redshifting Across Temps

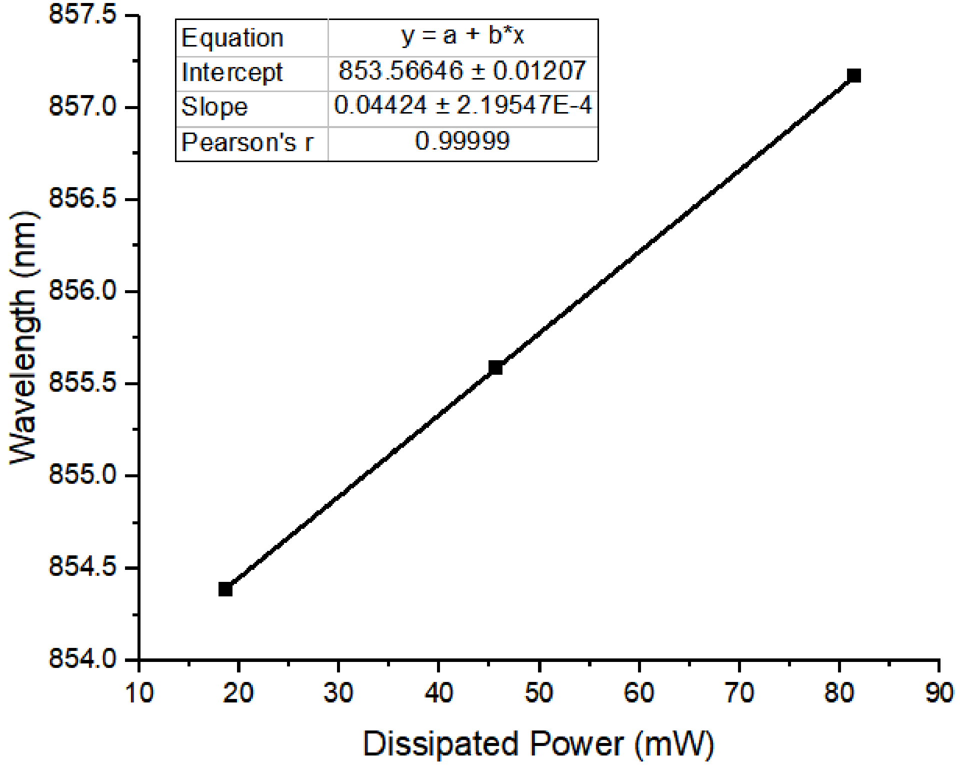
- L-I-V (CW)
- **Spectral Shift (Redshift)**
- Thermal Resistance (R_{th})
- R_{th} vs Literature



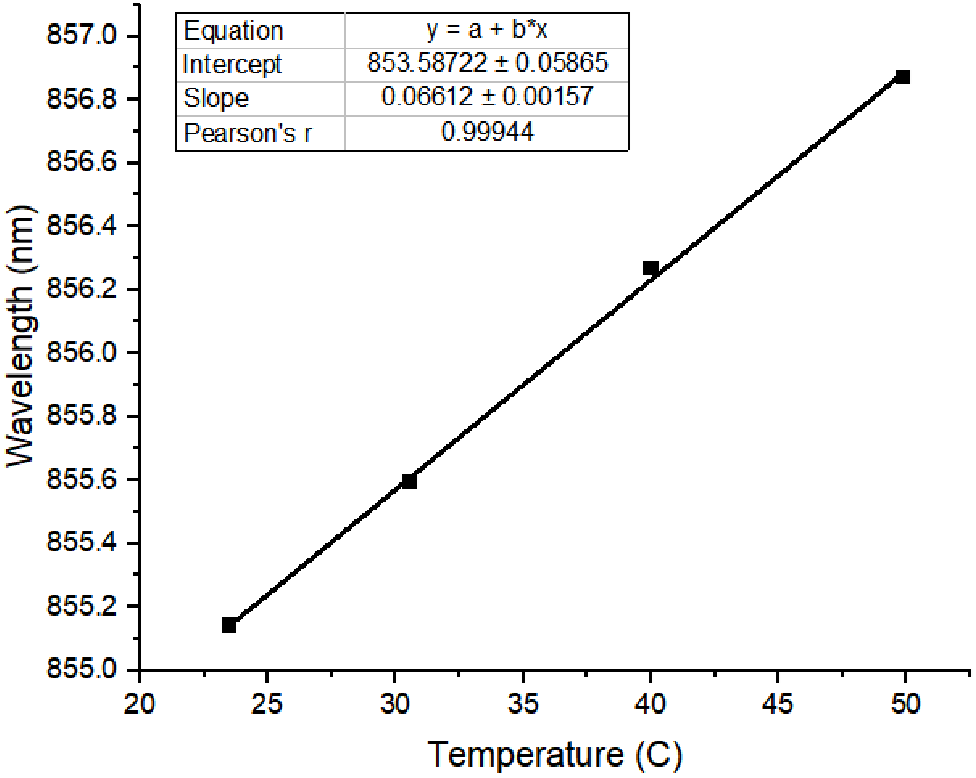
Integrated VCSEL Performance: **0.669 ℃/mW** Thermal Resistance

- L-I-V (CW)
- Spectral Shift (Redshift)
- **Thermal Resistance (R_{th})**
- R_{th} vs Literature

$$R_{th} = \frac{\Delta\lambda/\Delta P_{diss}}{\Delta\lambda/\Delta T} = \frac{.04424\ \mathrm{nm/mW}}{.06612\ \mathrm{nm/°C}} = \mathbf{0.669\ °C/mW}$$



Equation	y = a + b*x
Intercept	853.56646 ± 0.01207
Slope	0.04424 ± 2.19547E-4
Pearson's r	0.99999



Equation	y = a + b*x
Intercept	853.58722 ± 0.05865
Slope	0.06612 ± 0.00157
Pearson's r	0.99944

Integrated VCSEL Performance: vs. 10 μm aperture, GaAs VCSELs from Lit.

- L-I-V (CW)
- Spectral Shift (Redshift)
- Thermal Resistance (R_{th})
- **R_{th} vs Literature**

Integration Methodology	Thermal Resistance (℃/mW)	Comparison w/ Epi. Transfer
Epitaxial Transfer	0.669	1x
Flip-Chip	2.8[1]	4.2x
Flip-Chip	2.6[2]	3.9x
*Flip-Chip**	*1.2*[2]	*1.8x*
-	2.2[3]	3.3x
-	2.02[4]	3x
*-**	*2.0*[5]	*3x*

Italicized = Uses techniques to reduce thermal resistance*

From Literature:

[1] Grabherr, Martin, et al. "Fabricating VCSELs in a high-tech start-up." *VCSELs and Optical Interconnects*. Vol. 4942. SPIE, 2003.

[2] Roscher, Hendrik, and Rainer Michalzik. "Fabrication-Efficient Flip-Chip-Bondable 850-nm VCSELs With an X-Shaped Vertical Cavity." *IEEE Journal of Selected Topics in Quantum Electronics* 19.4 (2013): 1700810-1700810.

[3] Westbergh, Petter, et al. "High-Speed Oxide Confined 850-nm VCSELs Operating Error-Free at 40 Gb/s up to 85C." *IEEE Photonics Technology Letters* 25.8 (2013): 768-771.

[4] Pan, Po-Chou, et al. "Effect of thermal management on the performance of VCSELs." *IEEE Transactions on Electron Devices* 67.9 (2020): 3736-3739.

[5] Al-Omari, Ahmad N., and Kevin L. Lear. "VCSELs with a self-aligned contact and copper-plated heatsink." *IEEE Photonics Technology Letters* 17.9 (2005): 1767-1769.

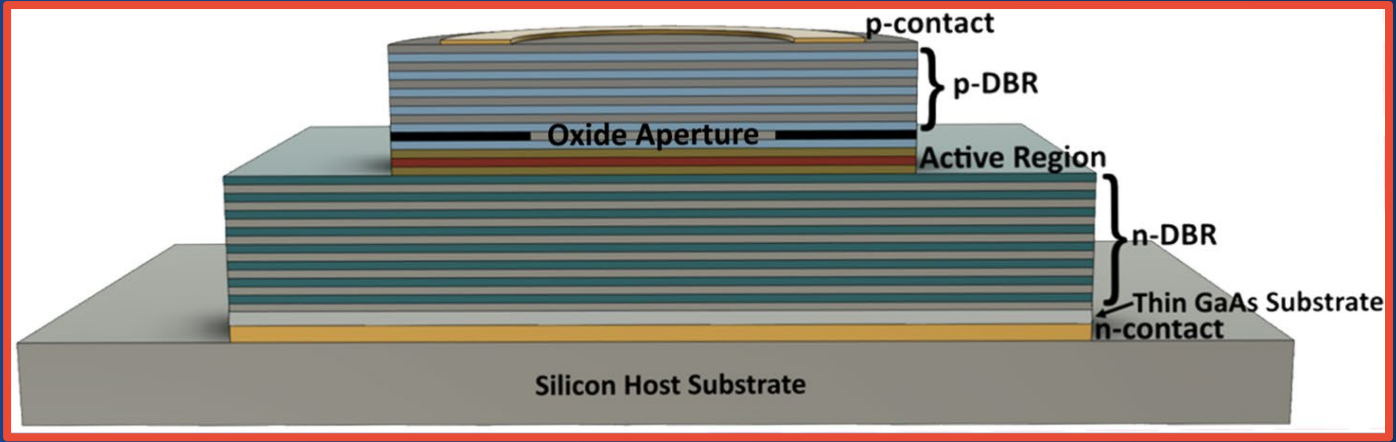
Summary

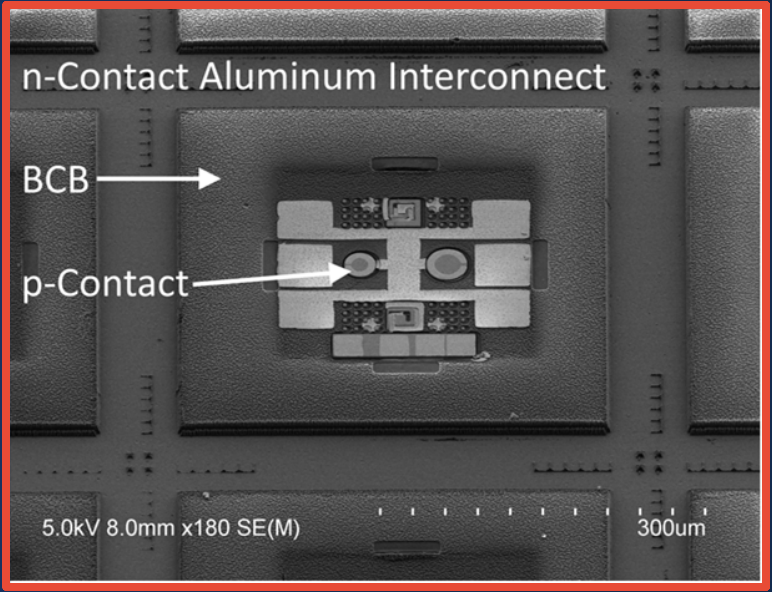
Epitaxial Transfer Integration Creates **Improved Thermal Environment** for GaAs-Based Photonic Devices

- GaAs VCSELs on Silicon have reduced spectral redshifting / thermal resistance

Our Other VCSEL Work

- Impurity-induced disordering allows for high-power single-mode and single-polarization VCSELs
- Anti-phase coating allows for high-power single-mode VCSELs





Acknowledgements & Contact

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- The II-VI Foundation

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