Scaling Manufacture of Compound Semiconductor Devices

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Agenda

- C&D Overview
- Platforms
- Applications
- Challenges
- Systems
- Summary

- Growth with the most productive tool set
  - Product Flexibility/Focus
  - Efficient Capital Utilization
  - Low Cost-of-Ownership

About C&D Semiconductor

- Founded in 1989; Privately Held
- 60+ Employees
  - Corporate HQ – San Jose, CA
    - Manufacturing, Design & Software Engineering, Customer Support, Applications, Sales
  - Engineering Center – Vietnam
    - Customer Support (Asia), Design & Software Engineering
  - Global Sales & Service Offices
- Installed base: 1500+ systems installed
- Vertically Integrated
  - In- house R&D, Machine Shop (Metals, Ceramics, Plastics), Software System Development for Fast-Turn Service & Enhancements
- Systems manufactured in San Jose, CA

Process Systems Platforms

- Global customer base
  - R&D – Low Volume Production → HVM
  - Si, GaAs, InP, GaN, Glass, SiC, $LiNbO_3$ ….
  - IC, Discretes, RF, MEMS, LED, PIC …
- Customer focus
  - Optimize systems based on customer need
  - Optimized HW & SW
  - Continually developing new applications and technologies & functionality

2 inch wafers to 300 mm wafers

Wafer on Tape Frame and HOOP

Wafer Fab and Packaging

P9000 Cluster Platform

P8000 Linear Platform

smartPro P9000

C&D Applications

PR Coat & Develop
- Positive PR
- Negative PR
- DUV
- PMMA
- 25 nm Node
- Thick PR, 150 µm
- Optical Edge Bead Removal
- HVM Configurations

Dry Film Developer - Cu Bump and Pillar
- Thick Resist Develop
- Dry Film Develop

Thermal Process
- Alloy for Compound Semi
- Low temp RTP w/o lamps
- $LiNbO_3$, GaAs - Compounds

Planarization (SynchroSpin™)
- Positive PR
- Polyimide
- BCB
- SOG
- Thick Films, 150 µm

Packaging - Wafer
- Interposer Fabrication
  - Si
  - 100 µm Glass
- Molded wafer
- RDL
- PR Coat & Develop
- Metal Lift-Off
- Bonding TSV Reveal

Life Science – Sensor Manufacturing
- Peptide Synthesis
- DNA Synthesis

Metal Lift-Off
- Positive PR / Negative PR
- DUV
- 25 nm Node
- HVM Configurations
- PR Stripping Post Etch

Spray Coating
- 4:1 Aspect Ratios
- Combine with planarization
- Combine with std coating

Frame Track
- HOOP Process
- Frame Processing
- Dice Protect Layer Coat
  - Saw, Laser, Plasma
- Post Dice Clean/Strip
- HVM Configurations

CS Fab Challenges

Category	
Substrate Sizes	2”, 3”, 4”, 5”, 6”, 8”
Substrates thickness	100 µm to 1,500 µm
Materials	GaAs, InP, SiC, GaN, GaSb, InSb, GaNSi, SiN, $LiNbO_3$,$LiTaO_3$
Device Types	Circuits, PICs, VCELS, Waveguides, SWIR……..

- Small Wafer sizes: 2 to 4 inch
- Combo wafers sizes: 3 + 4 + 6 + 8 inch, in the same production line
- Pyrophoric substrates and coating materials
- Thin and Thick substrates in the same production line
- Foot print restrictions: Expansion or Invasion vs. New Facility
- Foot print and capital optimization
- Mixed lithography techniques: Mask Aligner, Stepper, E-beam
- Performance Evaluation: Electrical, Optical, Mechanical, Mixed in many fabs
- Multiple Layer/Application Systems
- Single Layer/Application Systems (performance/Cost-of-Ownership/Footprint/Flexibility)

Cross Section of Customers

Customer	Wafer Sizes	Substrates	Type	Devices	Applications
A (25+)	4/6/8	GaAs, GaN, SiC, III-V	IDM Foundry	pHEMT, HBT, BiHEMT, Analog, Mix Signal, BAW, MEMS, SAW,WLP	Laminate Develop, Bonding Coater, Alloy, Dice Protect
B (5)	4/6/8	SiC, GaN, GaAs, GaSb	R&D/Pilot	GaN MMIC, FET MMIC	Coat & Develop, Lift-off, Synchrospin®
C (20+)	4/6	GaAs, SiC, GaN, $LaTaO_3$	IDM	HB-LED, GaN HBT, Power, pHEMT, FET, GaN LED, HEMT	Coat & Develop, Flood Expose, Alloy,
D (1)	3/4	InP, GaAs	IDM	Laser Chips	Integrated P9000/Mask Aligner
C (7)	4/6	InP, GaAs, GaN, InGaP, III-V	Foundry	HBT, RF, pHEMT	Coat & Develop, Alloy, Lift-Off
E (1)	4/6/8	GaAs, InP, InSb, GaSb	R&D/Pilot	IR Sensors	Integrated P9000/Mask Aligner
F (7)	3	GaAs, InP	IDM	Discrete, FET, HBT, Analog, Mix Signal	Coat & Develop, Alloy
G (15+)	6	GaAs	Foundry	HBT, pHEMT, mHEMT, RF, VCSEL, MMIC GaN HEMT	Coat & Develop, Alloy, Dice Protect
H (10+)	6	GaAs	Foundry	HBT, pHEMT, VCSEL, RF	Coat & Develop, Alloy, Lift-Off
I (15)	4	Sapphire, GaAs, InP, GaN, SiC	Foundry	GaN HEMT, GaAs HEMT, InP HEMT, InP HBT, MMIC	Coat & Develop, Upgrade to P9000

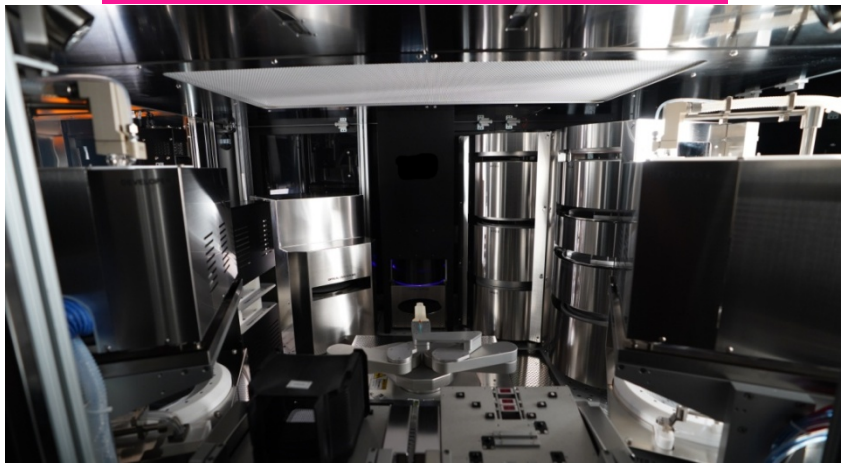
Broad Application Range System

Multiple Functionality

4/6/8 Inch Wafers, 2 Coat Modules, 1 Develop Module, 1 Lift-off Module, Optical EBR, 4 Pumps, 4 Syringe Pumps, Alloy Module, 4 HPO, 4 Chill Plates

smartPro P9000

Manual Module – Metal Lift-Off

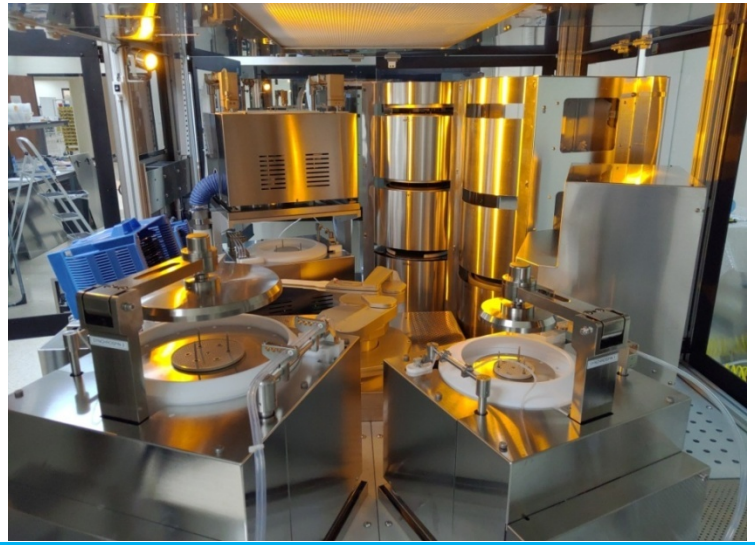


4/6/8 System: 2x Coater, 2x Developer, 1x Mask Aligner, Optical Centering, Optical EBR, 5x HPO, UV Flood Expose, 2x Chill, 1x VP

Si, Ge, InSb, GaAs, GaSb, Sapphire, Mounted wafers

Industrial/Gov't: R&D → Low Volume Mfg

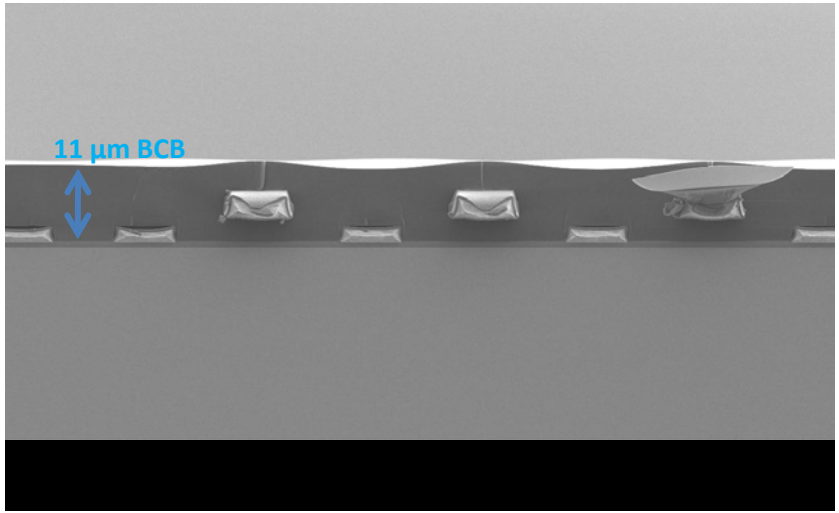
Production Coat & Develop Systems

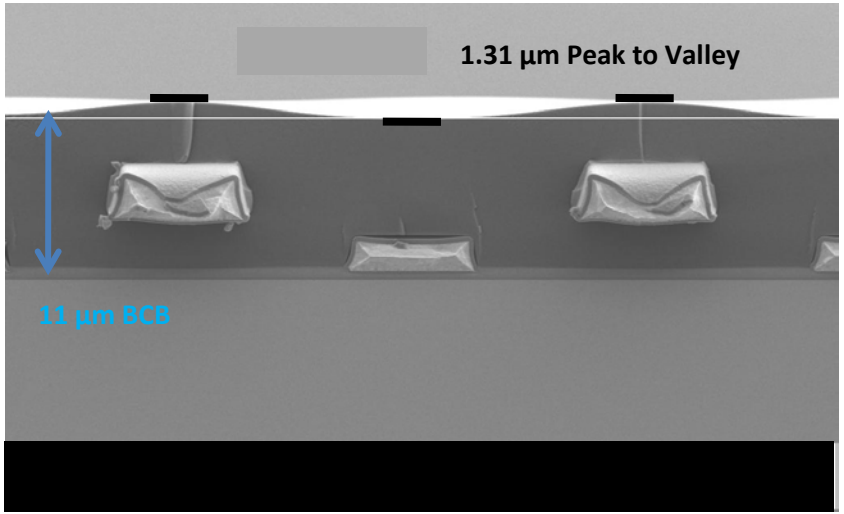


4/6/8 System: 2x Synchrospin®, 1x Coater, 1x Developer, 1 VP, 3 HPO, 1 Chill, Optical Centering
Substrates: Si, SiC, InP, GaAs
Users: Universities, Industrial, Government
Academia → R&D → Low Volume Mfg

3 & 4" System: Coater, Developer, 4x HPO, Optical Centering, 2x Chill, Vapor Prime, Mask Aligner
Substrates: InP, GaAs
HVM: Reduced wafer handling, reduced cycle time, reduced operator time

Synchrospin® Planarization Results





- Overburden of 10% or less
- Good under fill of Metal 2 lines, no voids
- Minimal post coating planarization required

HVM: Application Specific

Laminate Develop

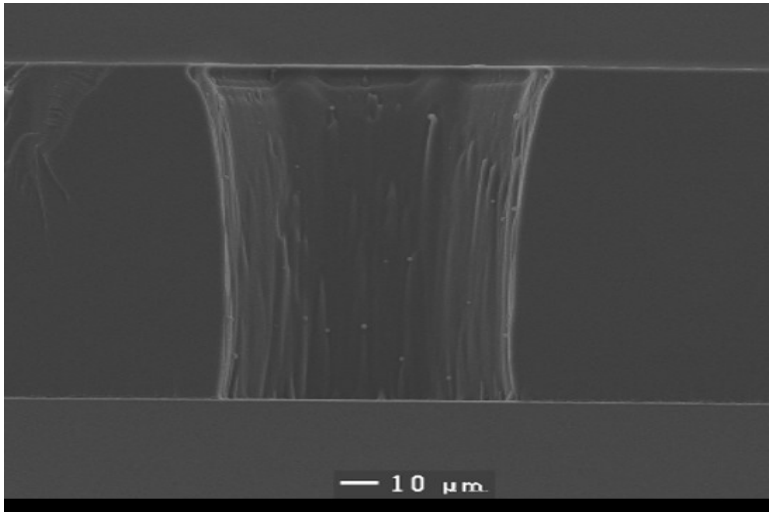
8” System: 5x Laminate Develop Modules, 5x CTD (Recirculating), Nozzle Temperature Control

smartPro P9000

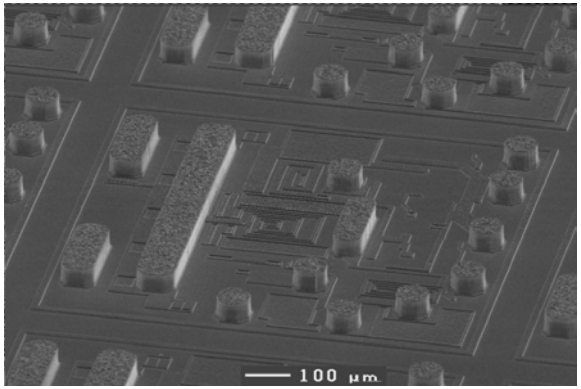
Temporary Bonding Material Coater

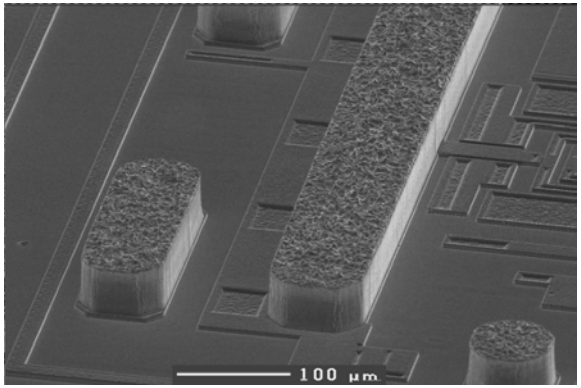
4/6/8 System: 2 Coaters, 10 HPO, 4 Chill
Substrates: GaAs, Mounted Wafer
Wafer Thinning: Application of temporary bonding material and carrier cleaning

Laminate Resist Develop - Bump



Post Develop Cross Section





Post Plating Results

Uniform Bumps (within die, die to die, wafer to wafer
Higher Yield
Tighter Product Performance
Improved yield + lower cost

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Metal Lift-Off & PR Strip

- Dry in/Dry Out, entire process in single module no wet wafer handling
- Soak step in recipe to replace dip tank
- High pressure spray - mechanical energy
  - Precision pressure control, a recipe parameter
  - Configurations: 2000 PSI max, 4000 PSI max
- Solvent Systems
  - **Acetone**, **NMP**, **DMSO**, **MR-REM 700**
- PR Strip – Difficult to remove PR, post etch or implant

4/6 System: 4x Lift-Off Modules, 4x High Pressure Pump, Optical Centering
Substrate: GaAs

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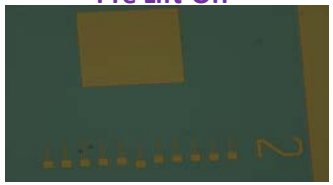
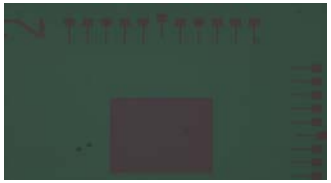
Pre Lift-Off



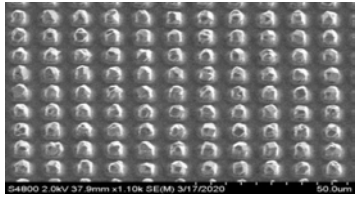
Post Lift-Off

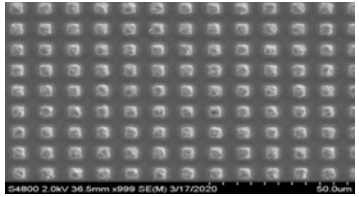


HfO_2 Lift-Off

Pre Lift-Off

Post Lift-Off

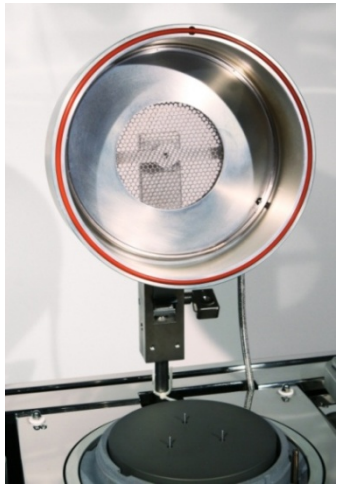




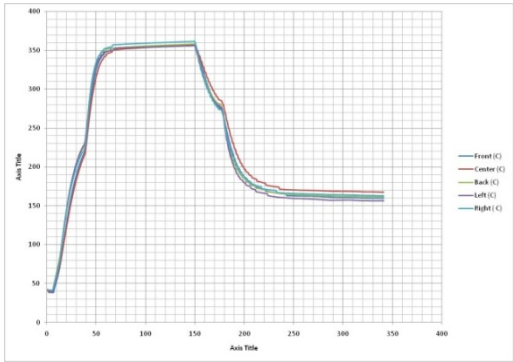
In Bump Metal Stack Lift-Off

Alloy & Anneal

- Low temperature anneal, up to 500 °C
- Metal Alloy
- Metal Anneal
- P7000, staple in many CS Fabs
- High throughput with low cost-of-ownership
    - No consumables
    - No bulbs to replace
- Multiple Gases (N_2, Ar, Forming Gas…)
- Active Wafer Cooling
- Available in P9000 and P8000 formats
- Large installed base



RTA Temp Profile



Alloy Temp Profile

smartPro P9000

Summary

- Growth with the most productive tool set
  - Product Flexibility/Focus
  - Efficient Capital Utilization
  - Low Cost-of-Ownership

- Optimized System Configuration
- Proven Field Performance – Process and Hardware
- Low Cost-of-Ownership
  - Few Consumables
  - High reliability
  - High Availability
  - Minimal scheduled down time
  - Short MTTR

- High value system with low cost-of-ownership