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SCREEN Laser Annealing Technology

For The Next Generation of Si and SiC Power Devices

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SCREEN Semiconductor Solutions Co., Ltd.

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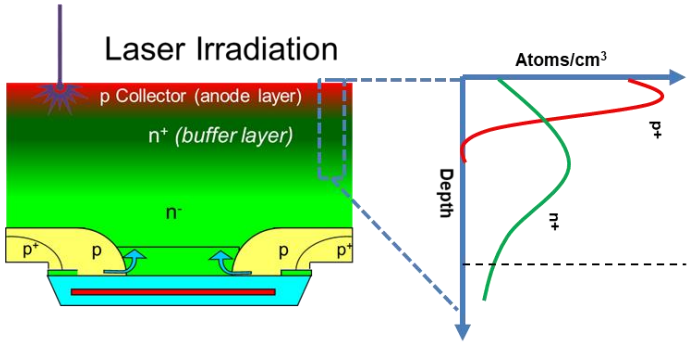
Motivations for laser annealing solution

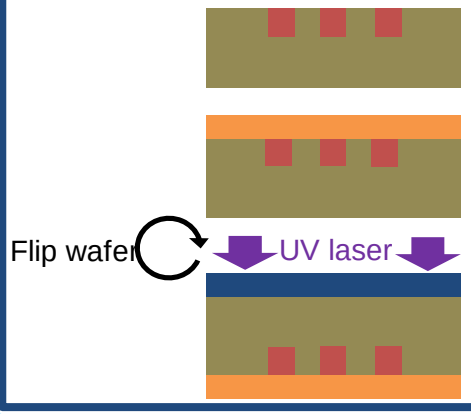
Si IGBT



- **Single step activation of p/n junction**
- **Buffer layer :**
  - Rp up to 5µm

SiC MOSFET

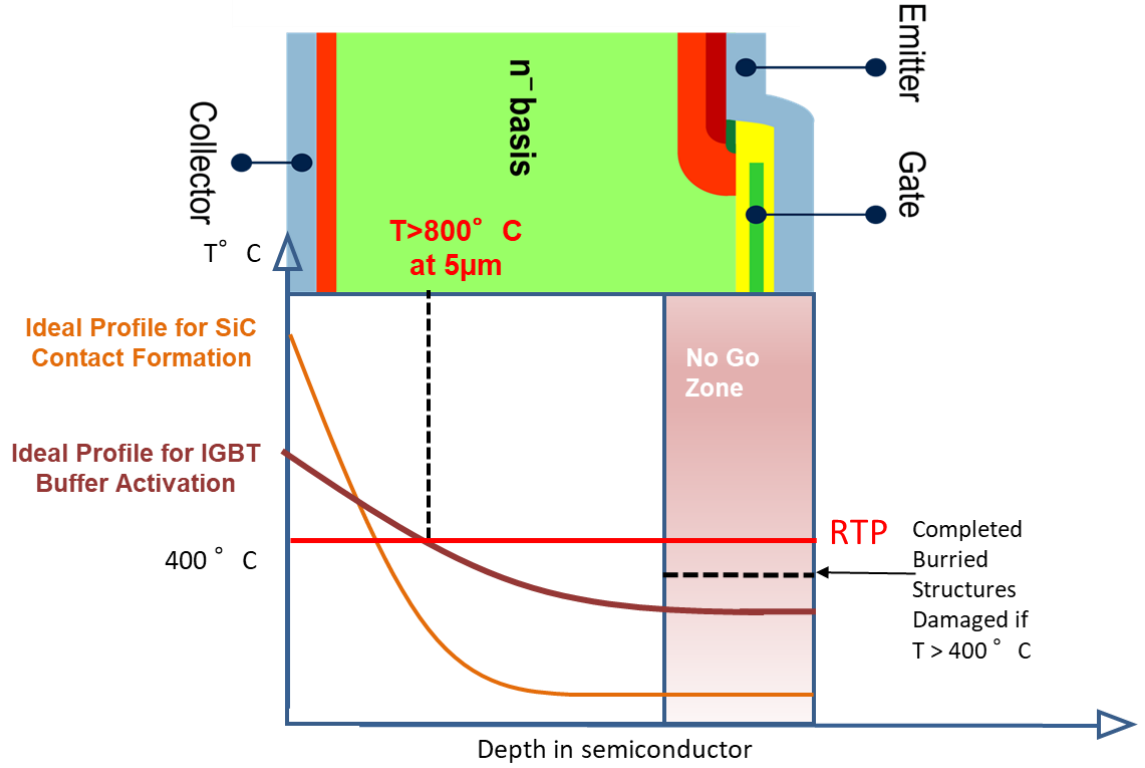
Flow with UV-LA for backside metallization on SiC



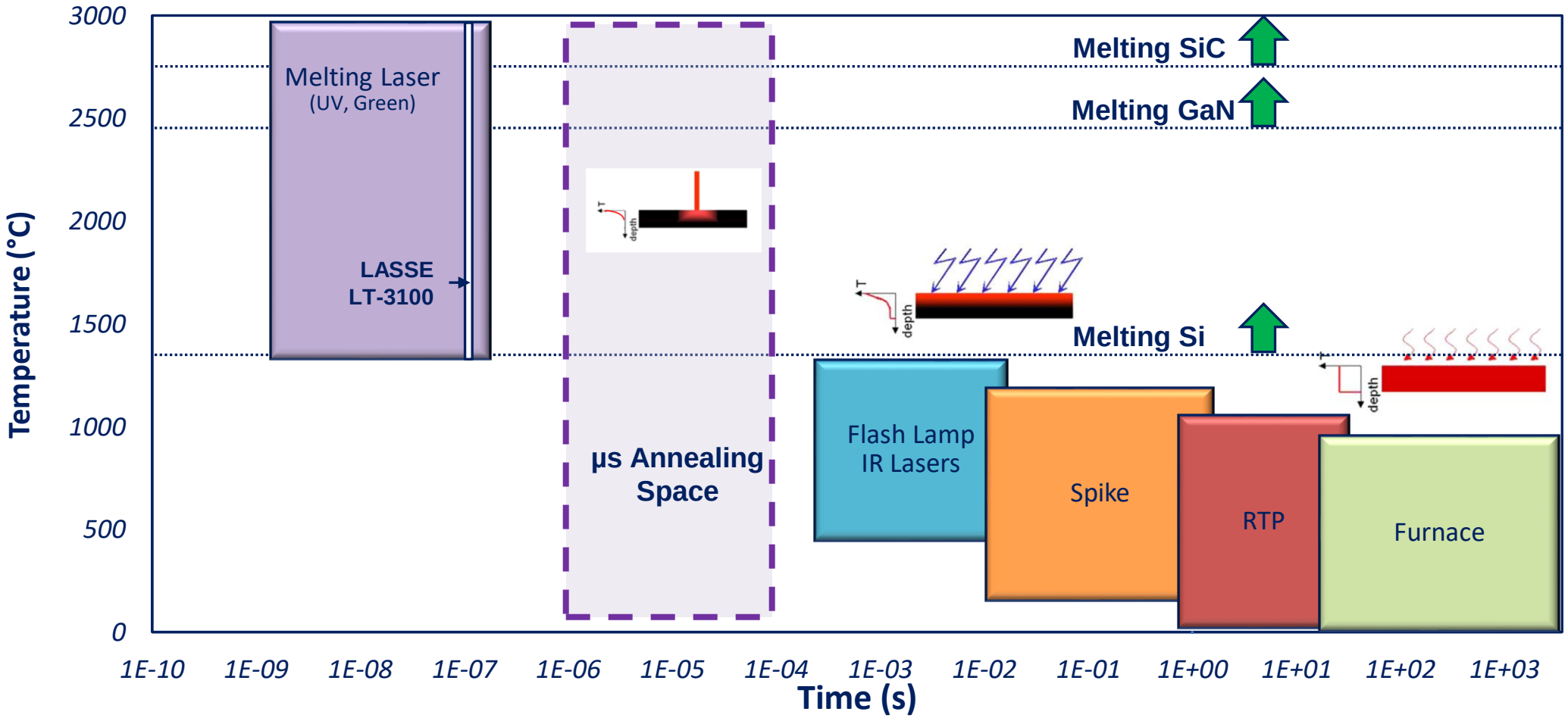
- **Backside ohmic contact formation:**
  - Uniform and controlled alloy phase
- **Dopant activation:**
  - Good crystal quality and high dopant activation ratio

Need to develop a flexible laser annealing technology which can fulfill requirements of both technologies:

➔ **Ultimate control of thermal Budget**

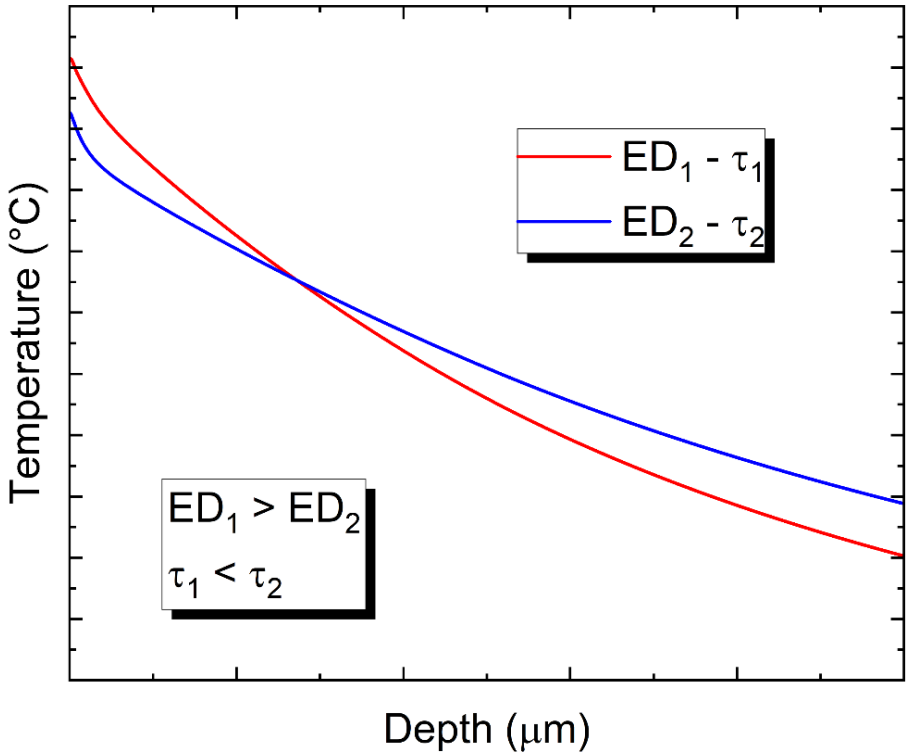


Screen solution for surface-localized annealing



Screen annealing solution combines the advantages of both longer submelt annealing and laser selective annealing

Thermal budget control

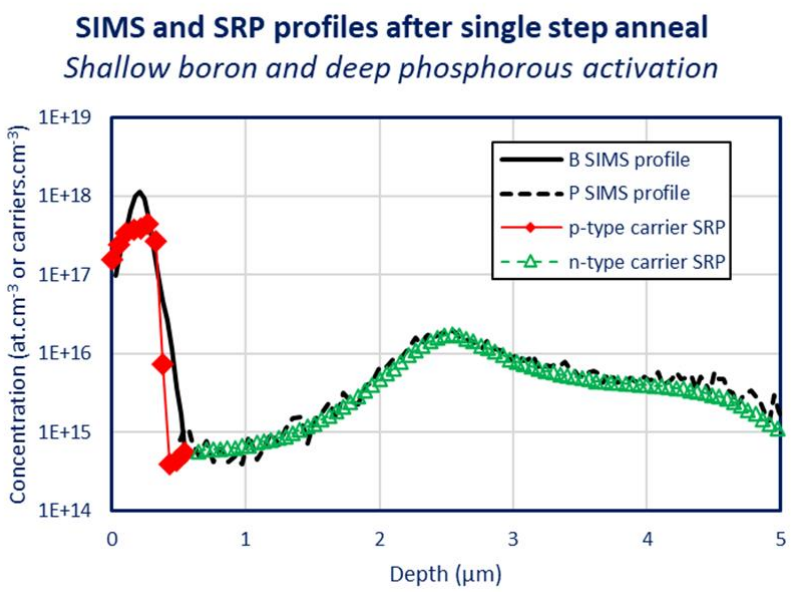


Ultimate control of temperature profile:

- *UV Wavelength*
- *Laser Energy Density (ED)*
- *Irradiation Time (τ)*

Platform highlights

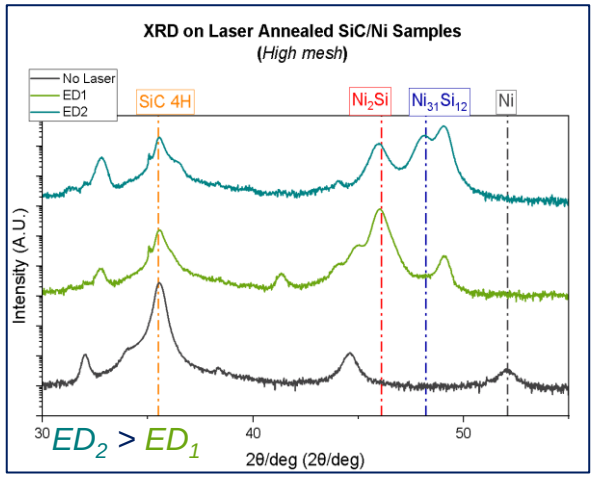
Si IGBT

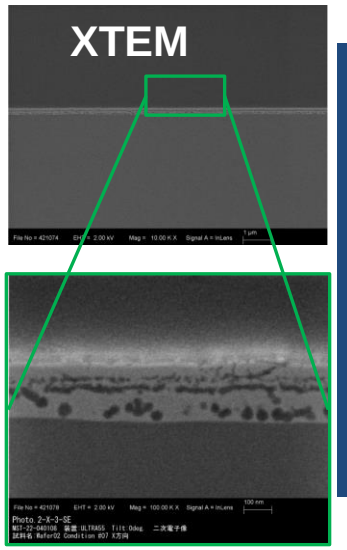


µs UV-LA benefits:

- Single step activation of deep p/n junction, with carriers profiles matching post-implantation SIMS profiles
- Suitable for all kinds of profiles up to 5 µm.
- Shallow absorption of UV ➔ compatible with thin wafers

Backside contact formation for SiC MOSFET



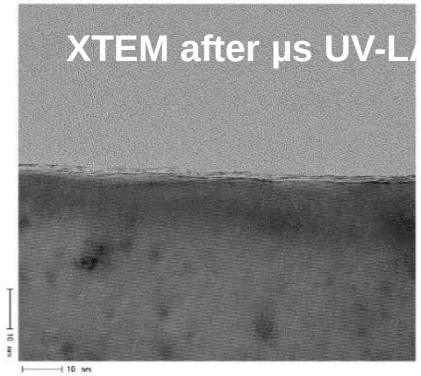


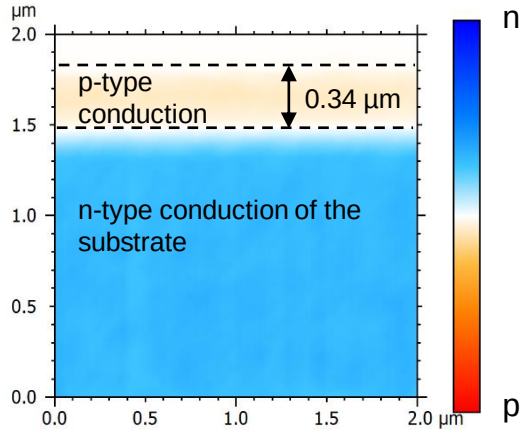
µs UV-LA benefits:

- Formation of Ni_2Si with progressive disappearance of pure Ni
- Continuous film with low roughness (< 10 nm RMS)

Raynal et al., ICSCRM 2022

Dopant activation for SiC MOSFET





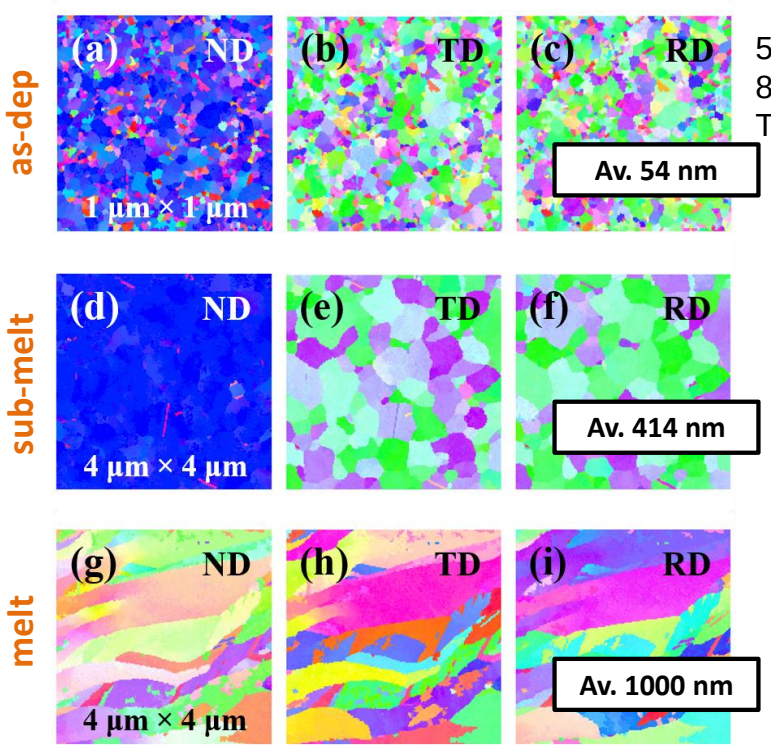
µs UV-LA benefits:

- Crystal curing
- Al activation

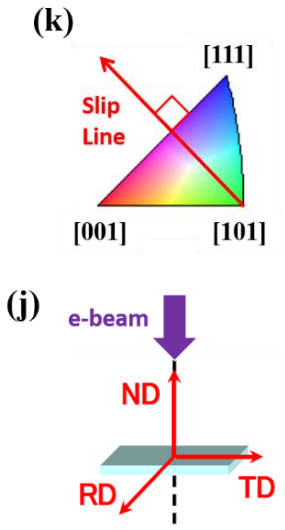
Rozé et al., ICSCRM 2022

Key achievements for advanced metal interconnections solutions

Cu grain enlargment



50-nm-thick sputtered-Cu on 8 nm-thick Ta/5 nm-thick TaN/100 nm-thick SiO_2/Si



T. Tabata et al. IITC 2021

µs UV-LA benefits for Cu lines:

- In sub-melt regime:
  - **4x** increase of grain size compared with 600C furnace anneal
- In melt regime:
  - **10x** increase of grain size compared with 600C furnace anneal

Ru grain size enlargment

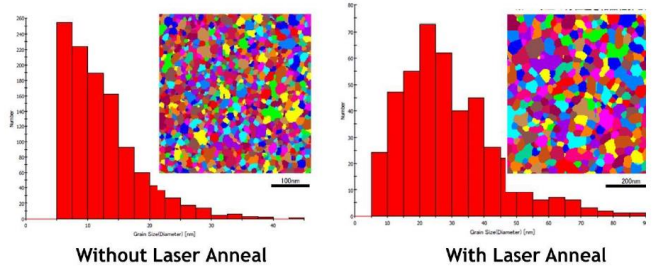


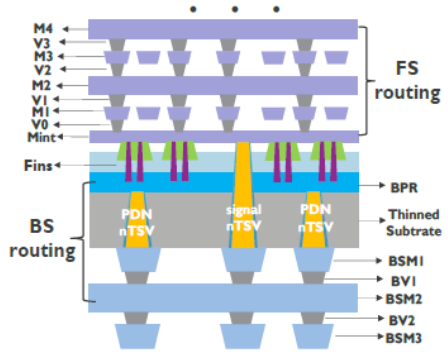
Fig. 9. EBSD showing Ru grain growth by ns-laser anneal preferentially for small grain populations.

T. Nogami, et al., VLSI 2022

µs UV-LA benefits for Ru lines:

- 30% sheet resistance decrease compared with state-of-the-art as deposited level

Backside contact formation for advanced interconnect



Chen, R., et al., IEDM 2021

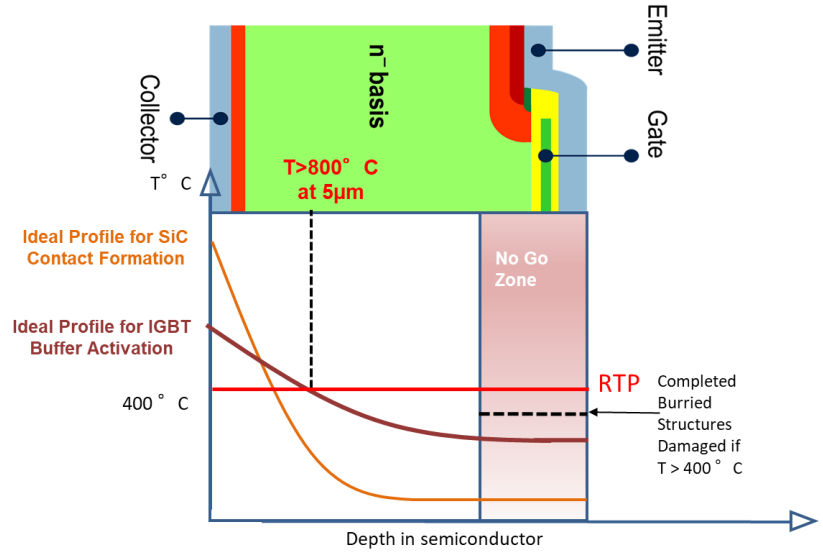
Low thermal budget backside contact formation is required for Buried Power Rail (BPR) integration schemes

Screen solution for surface-localized annealing: highlights

Ultimate control of thermal budget enabled by control of:

- *Temperature*
- *Time*
- *Depth*

Applications to Si and SiC power devices



- ✓ **Single step activation of p/n junction**
- ✓ **Backside ohmic contact formation**
- ✓ **Dopant activation**

Applications to metal interconnects

- ✓ **Cu grain size increase by x4 in submelt regime and by x10 in melt regime**
- ✓ **Ru grain size increase and sheet resistance enhancement by 30%**
- ✓ **Low thermal budget backside contact formation is required for Buried Power Rail (BPR) integration schemes**

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