Revolutionizing Architecture and Components for New Generation Energy-Efficient High-Density Photonic Integrated Coherent Transceivers

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Network Evolutions Toward 2030's

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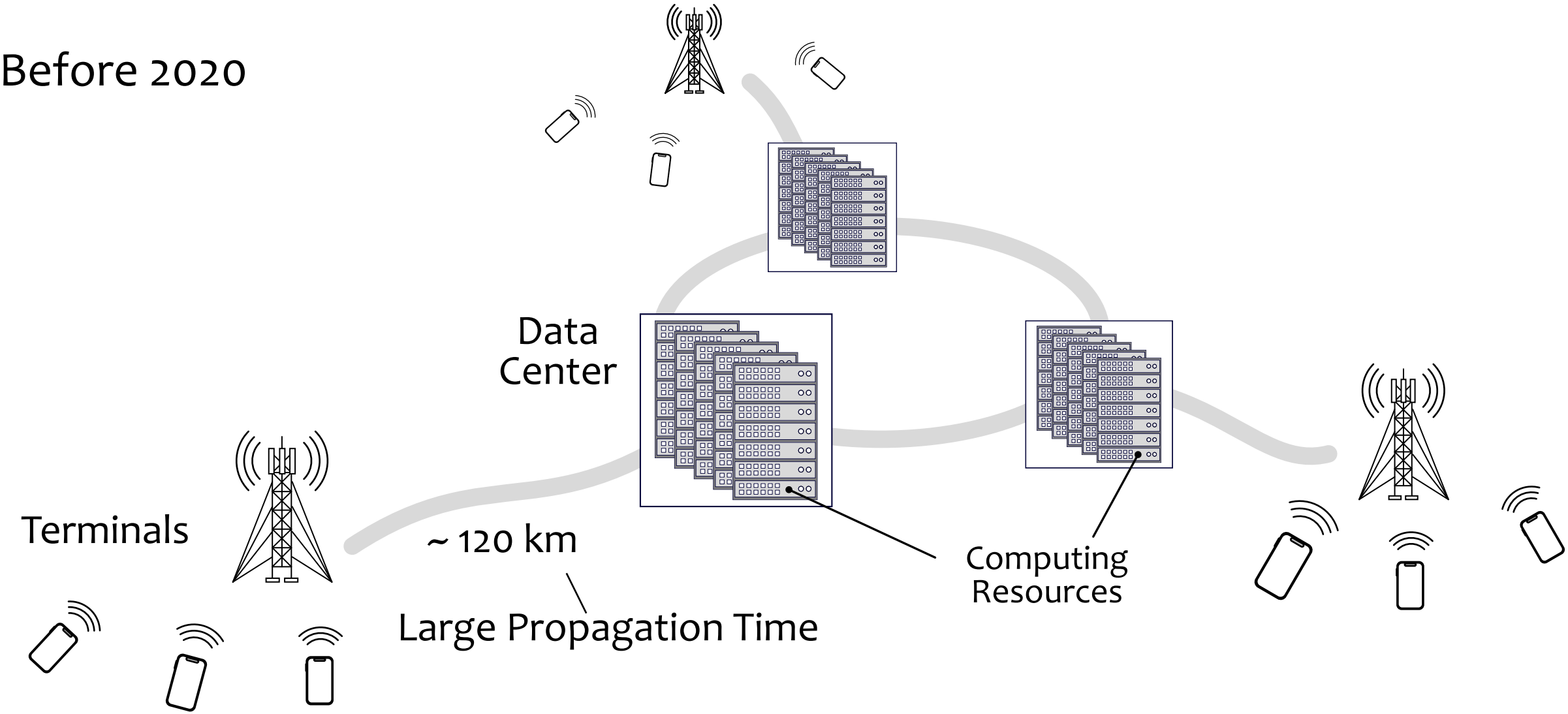
Before 2020



Limits Applications to OnlyThose Tolerating Large Latency

Network Evolutions Toward 2030's

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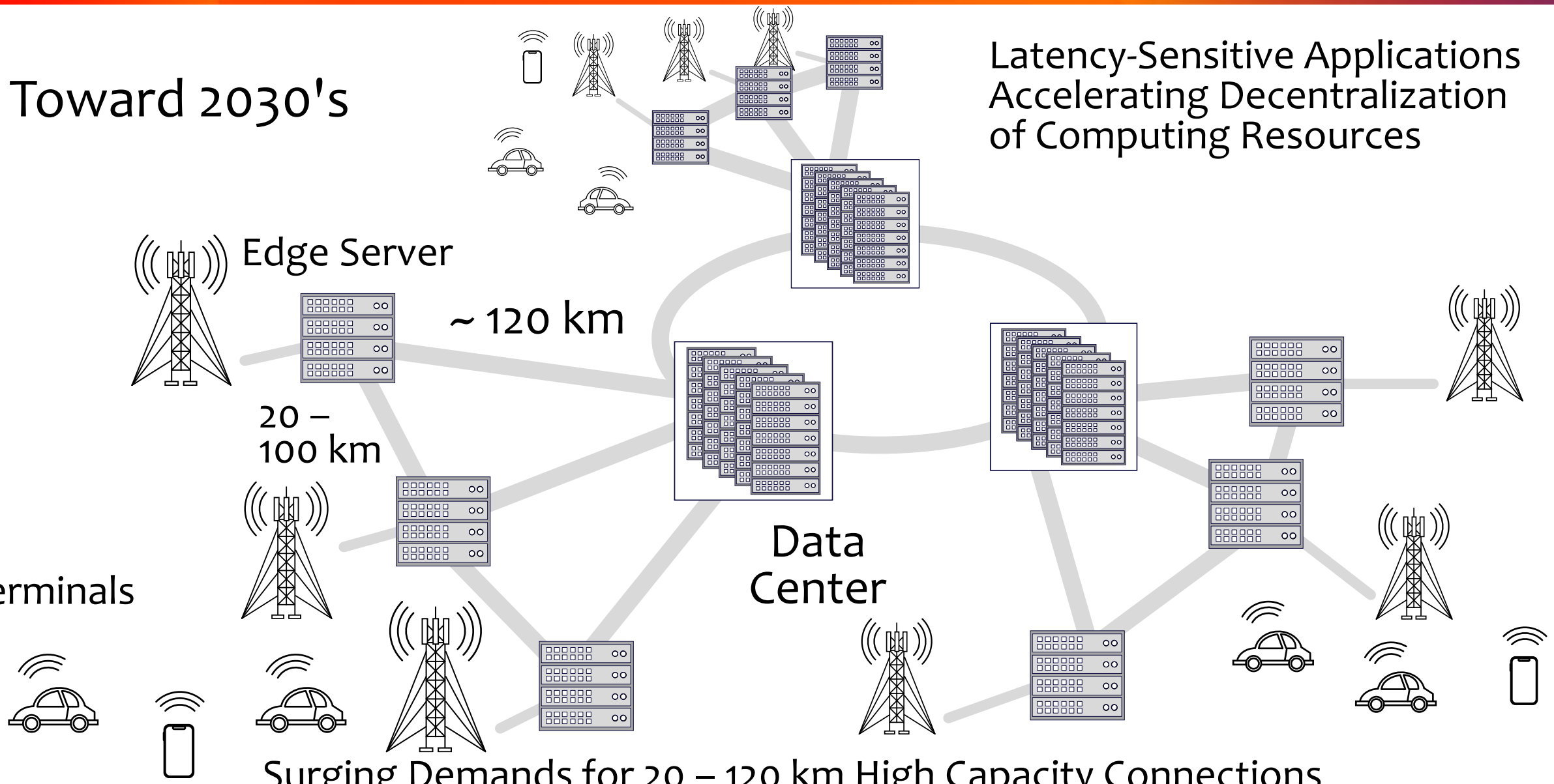
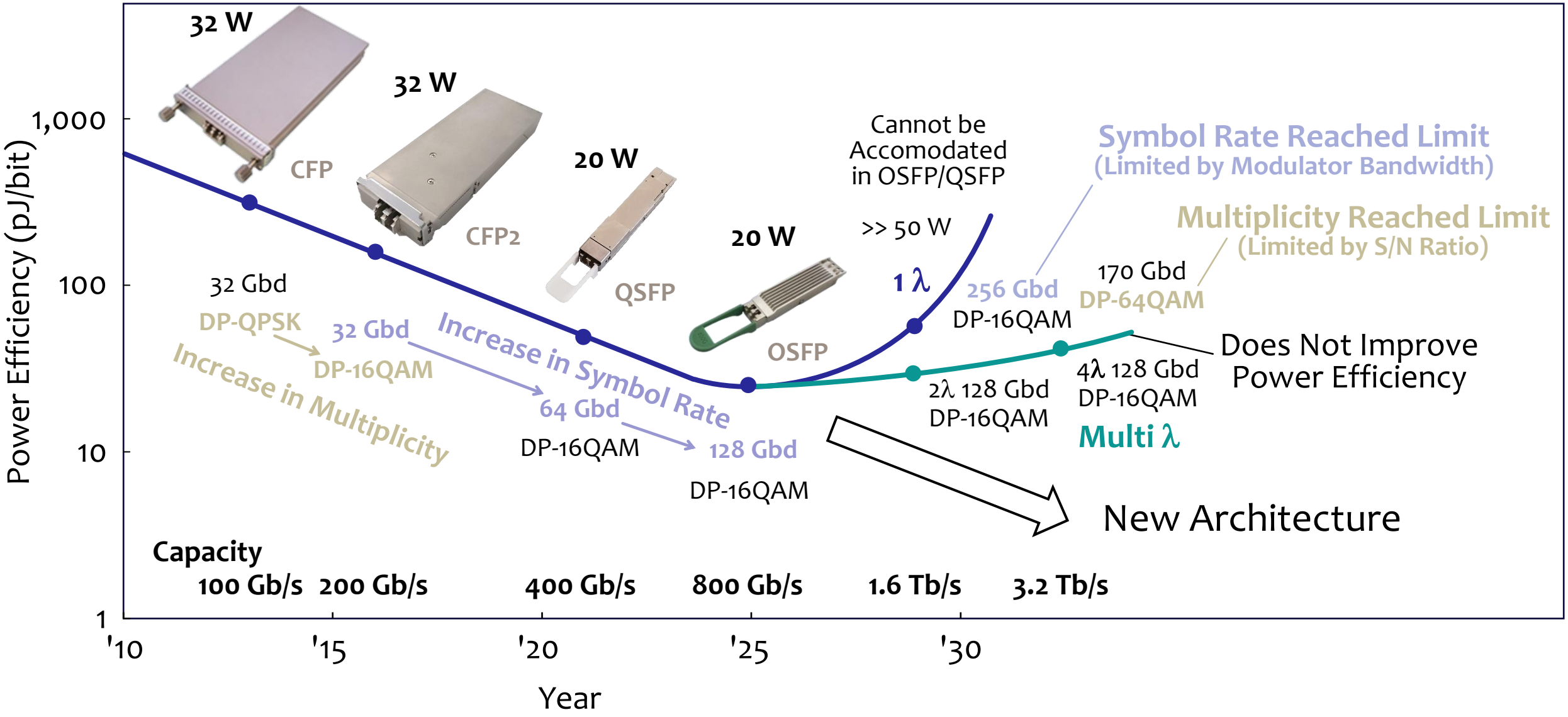
Toward 2030's

Latency-Sensitive Applications
Accelerating Decentralization
of Computing Resources



Surging Demands for 20 – 120 km High Capacity Connections

Trend of Pluggable Transceiver Power Efficiency



New Generation Transceiver Architecture

New Generation Transceiver Architecture

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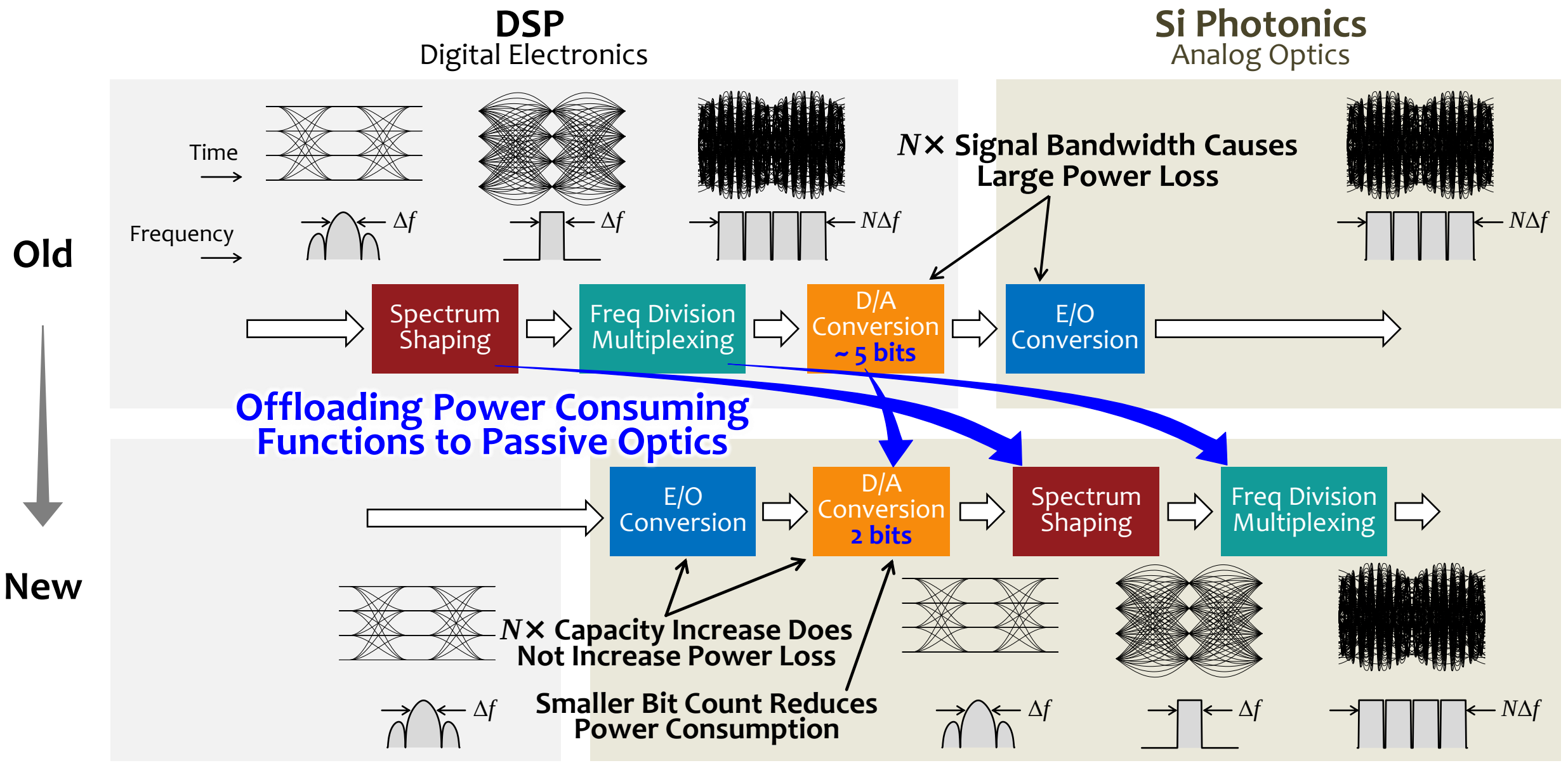

New Generation Transceiver Architecture

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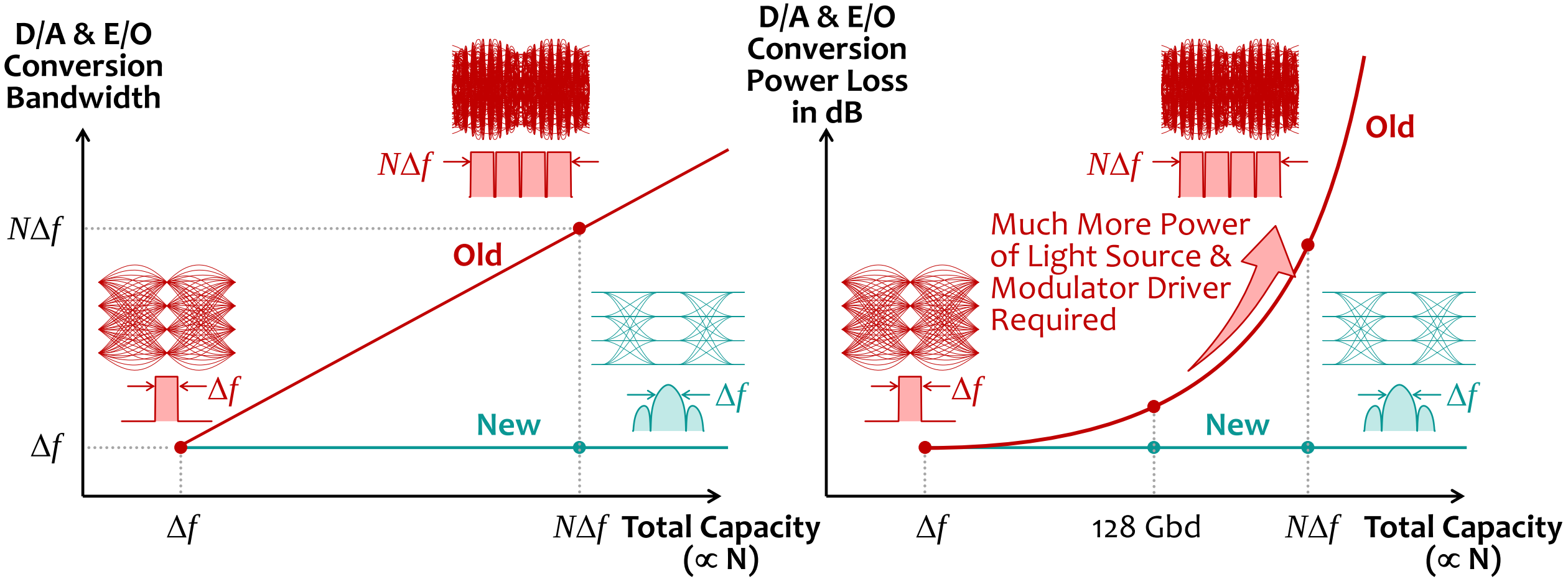
Benefits : Drastic Reduction of Power Consumption

D/A & E/O Conversion Loss↓ ⇒ Light Source & Modulator Driver Power↓



New Generation Transceiver Architecture

PETRA FUJITSU

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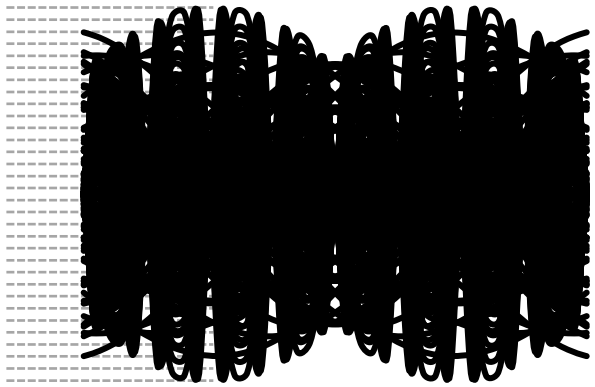
DAC Bit Count, N↓ 5 → 2 ⇒ DAC Power Consumption↓ 1/8x ($\propto 2^N$)

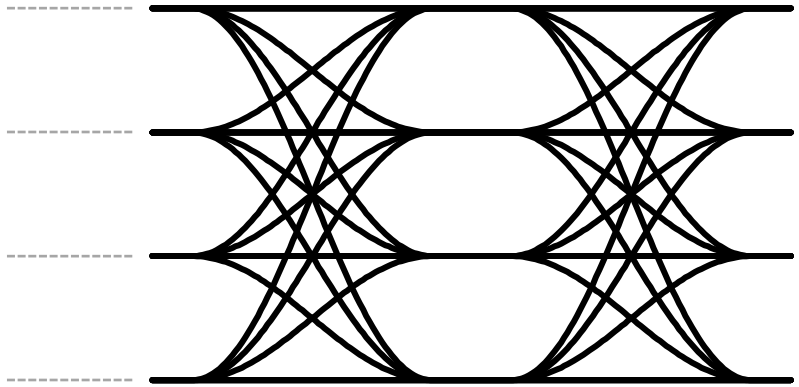
Old

~ 32 Levels
(~ 5 Bits)



New

4 Levels
(2 Bits)



New Generation Transceiver Architecture

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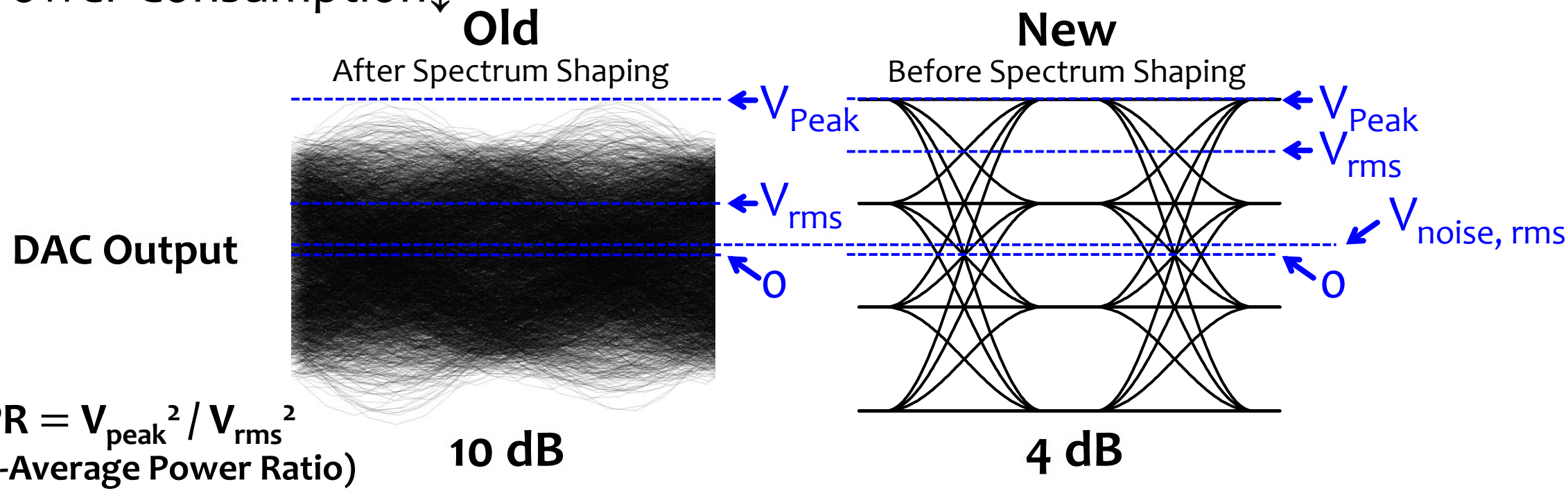
DAC PAPR↓ 10 → 4 dB ⇒ DAC S/N↑ +6 dB ⇒ ADC Noise Margin↑ ⇒ ADC ENOB↓ ⇒ ADC Power Consumption↓



PAPR = V_{peak}^2 / V_{rms}^2
(Peak-to-Average Power Ratio)

New Generation Transceiver Architecture

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Power Consumption for Electrical Spectrum Shaping Eliminated

New Generation Transceiver Architecture

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Power Consumption for Electrical Spectrum Shaping Eliminated

Concerns to be Addressed :

Loss↑ by Optical Spectrum Shaping ⇨ Compensated by DAC Loss↓ (PAPR↓)
(+ Only Slight ↑ of Light Source & Driver Power)

Loss↑ by Optical (De)Multiplexing ⇨ Loss↓ by CAT Technology

Novel Technologies Developed for New Generation Transceiver Architecture

E/O & D/A Conversion (Optical DAC)

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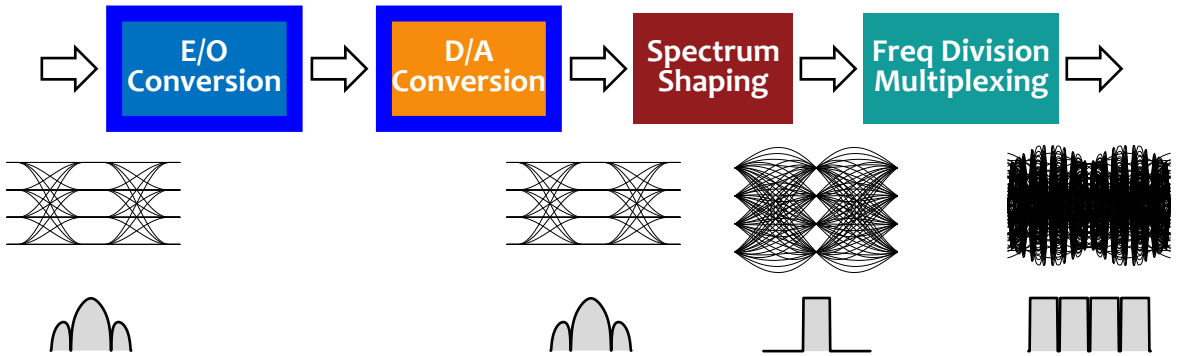
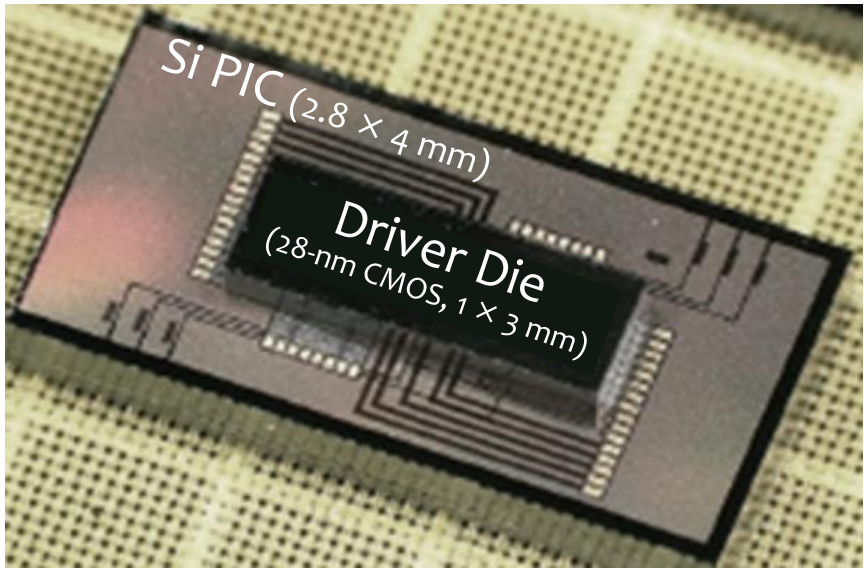
Transmitter





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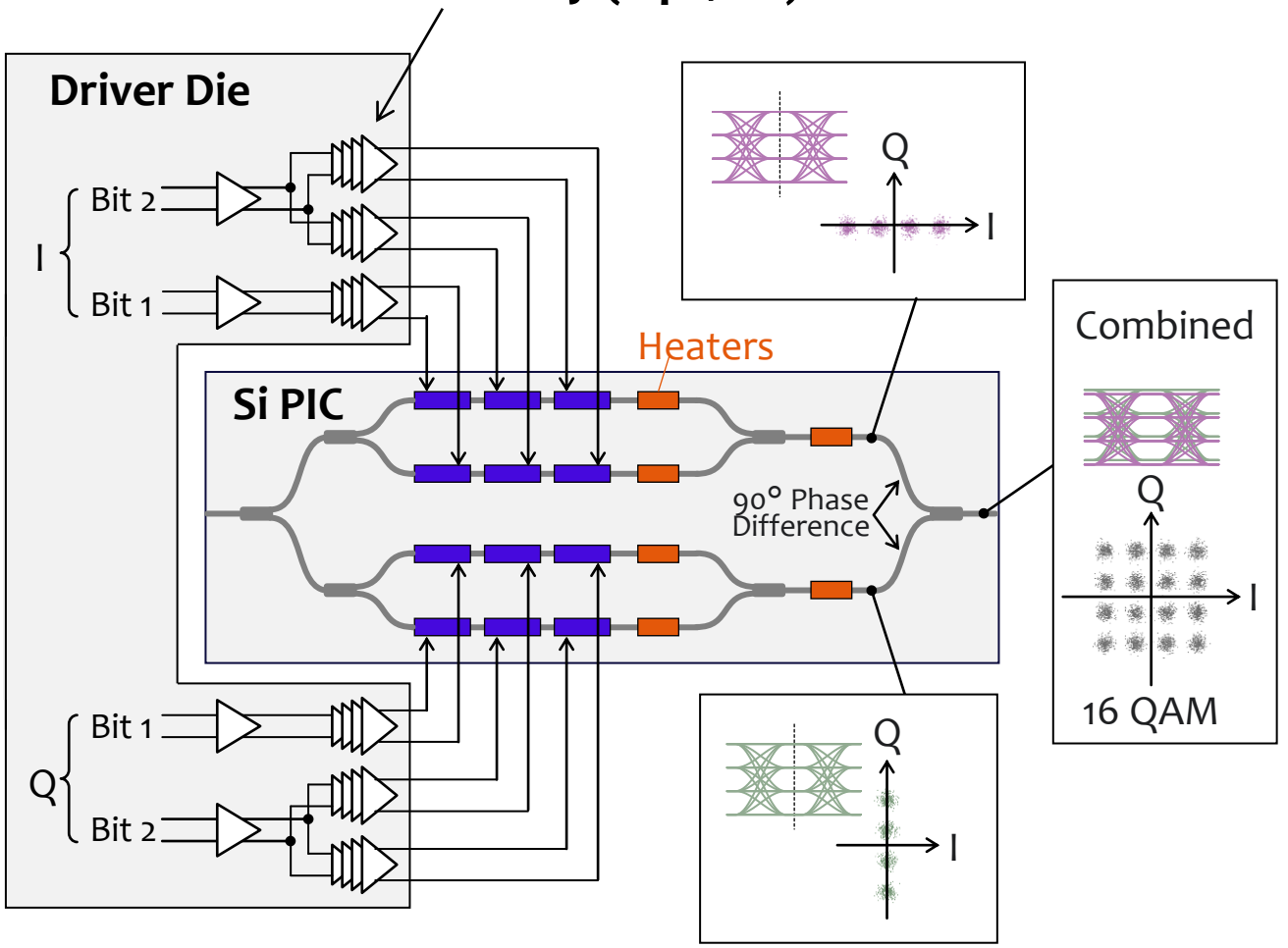
DOI : 10.1364/OFC.2022.M1D.4

CMOS Binary Drivers Used for Power Efficiency (2 pJ/bit)



Spectrum Shaping & Multiplexing

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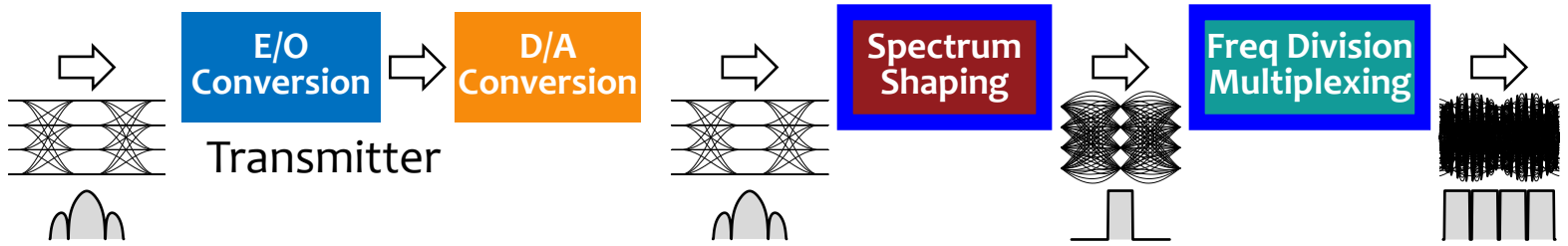
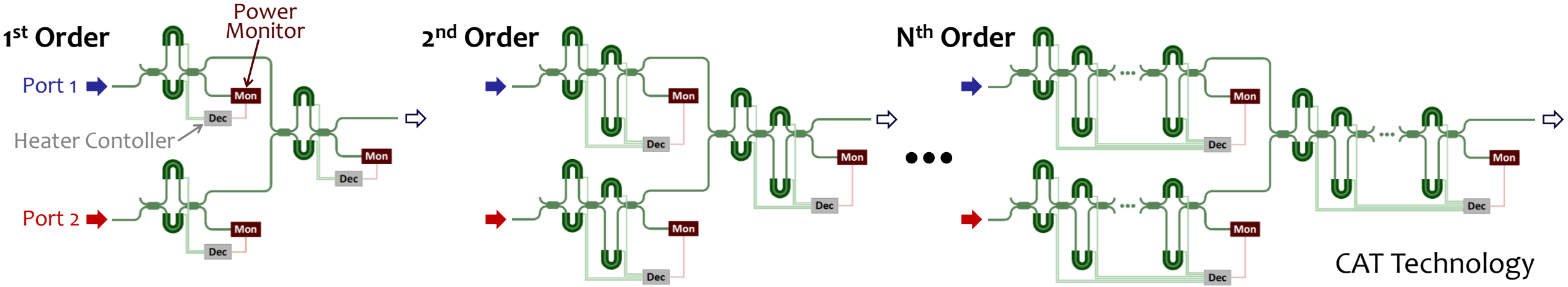
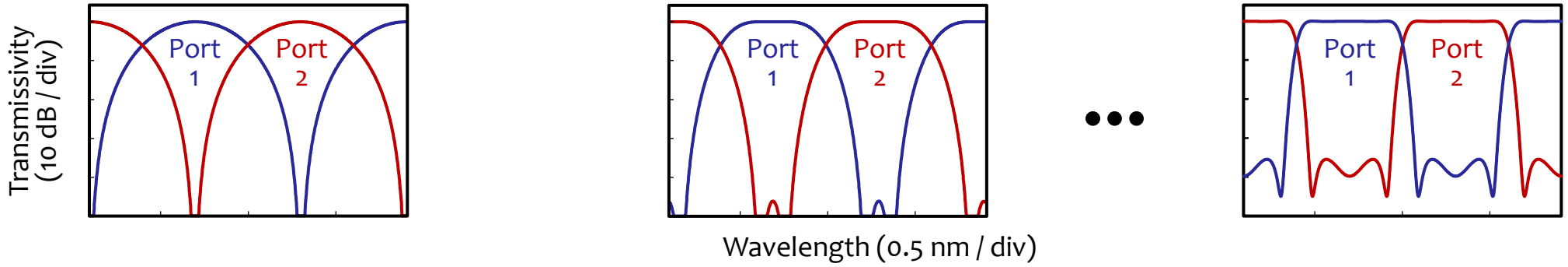


Autonomous Correction of
Fabrication Error Intrinsic to Si Photonics



CAT Technology



After Error Correction
(Simulation)

Nyquist(-like) Shaping with Reduced DAC Bit Count (5 → 2) for Drastic DAC Power Reduction (1/8 x)
Drastically Reduced Multiplexing Loss (6 → 2 dB for 4 Ports, 9 → 3 dB for 8 Ports, Compared to Couplers)

Demultiplexing

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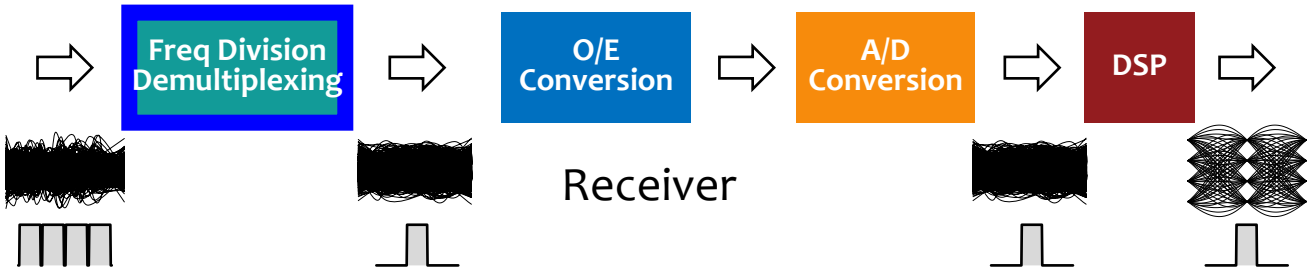

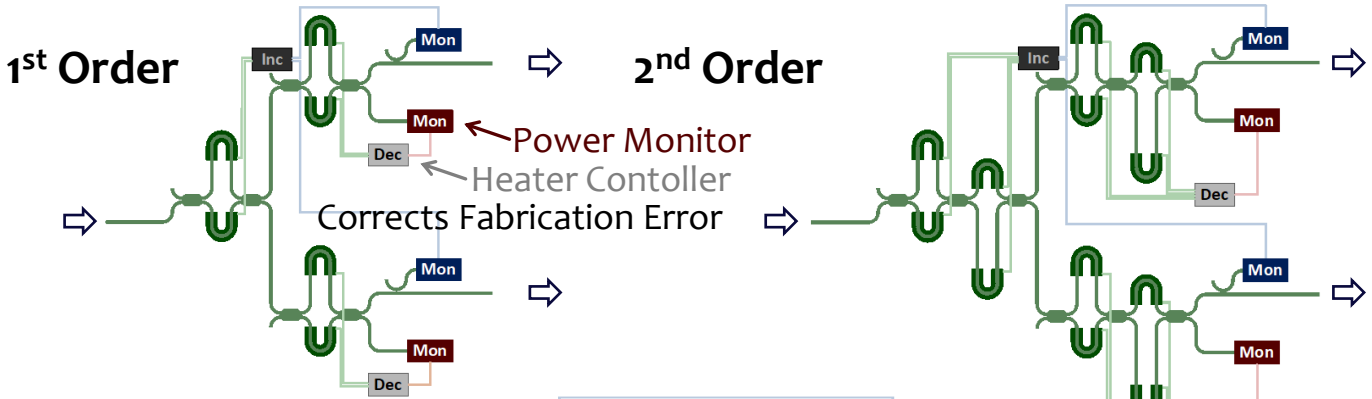

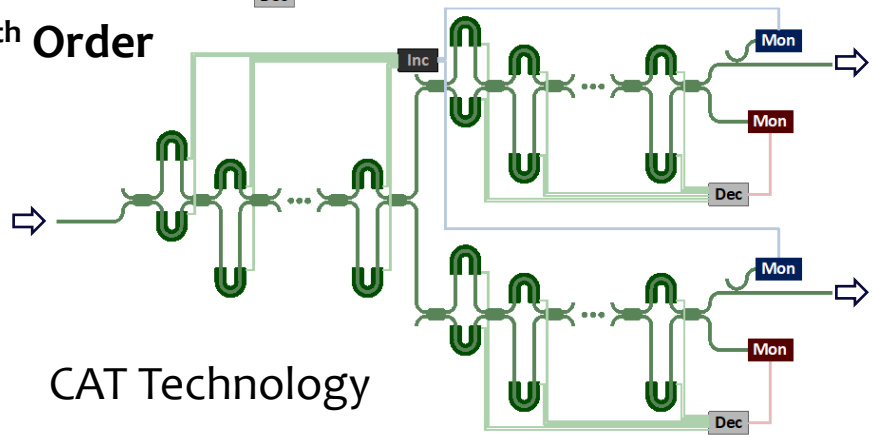

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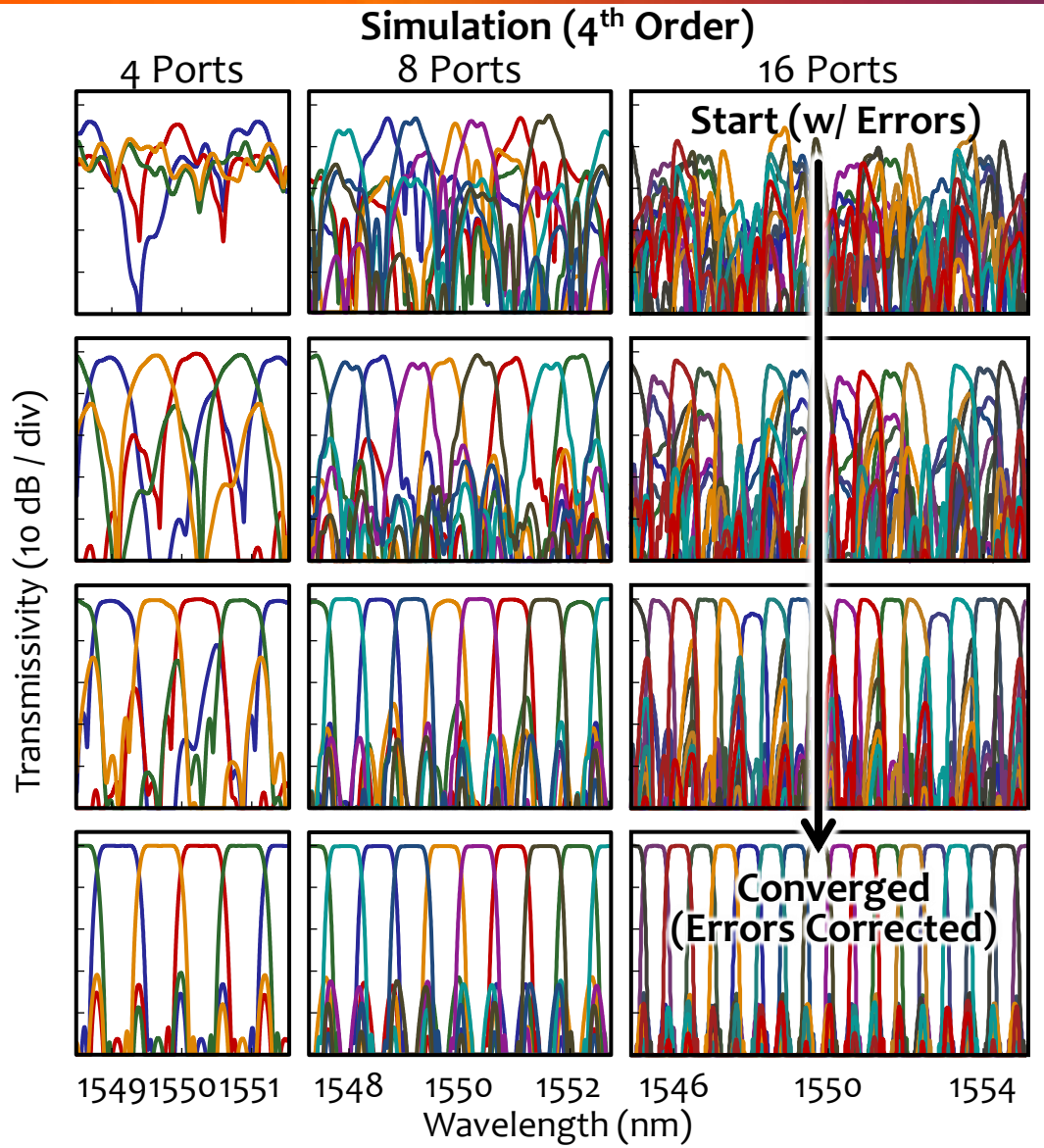
DOI : 10.1364/OE.410379



Drastically Reduced Demultiplexing Loss (6 → 2 dB for 4 Ports, 9 → 3 dB for 8 Ports, Compared to Couplers)

Demultiplexing

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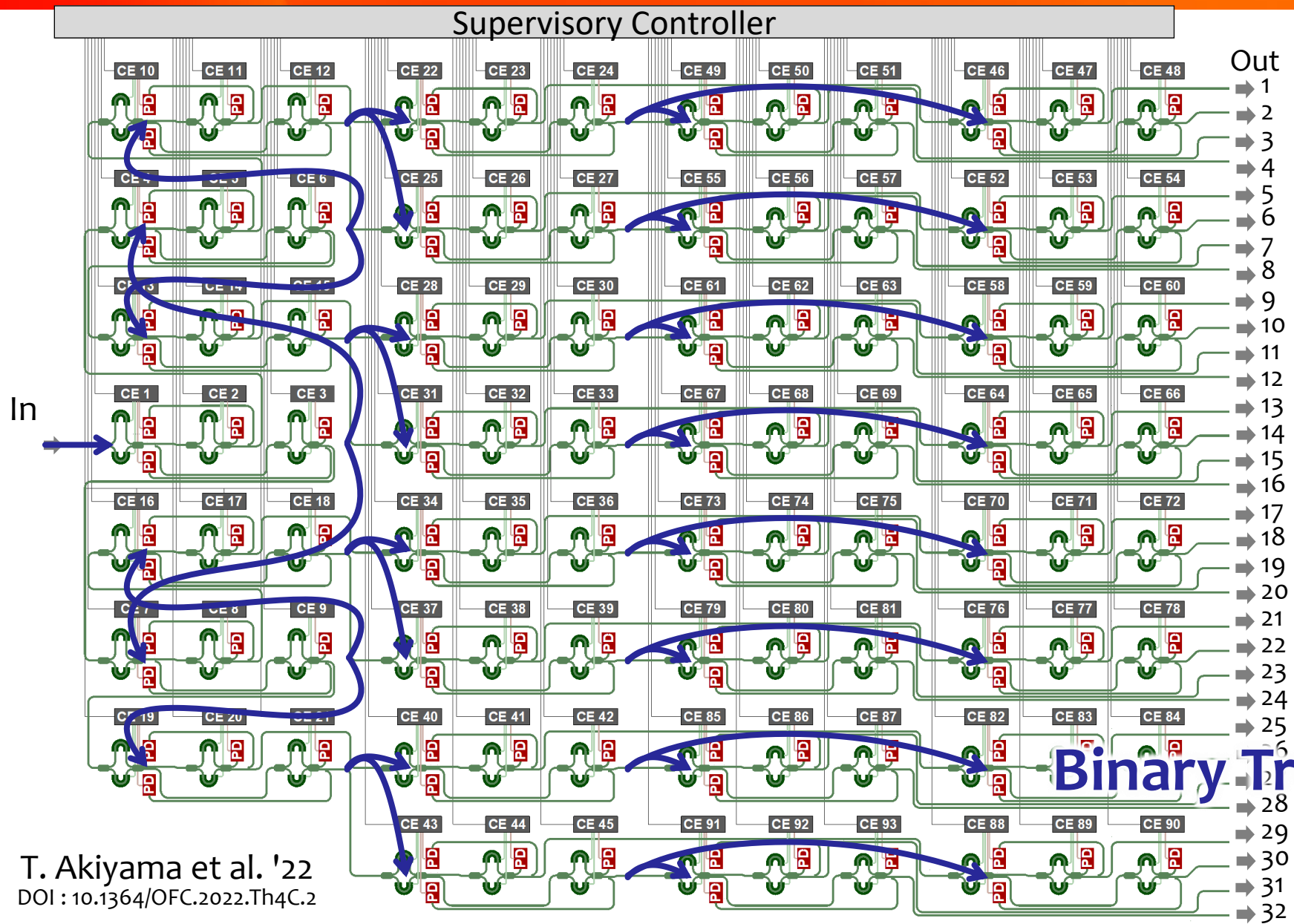

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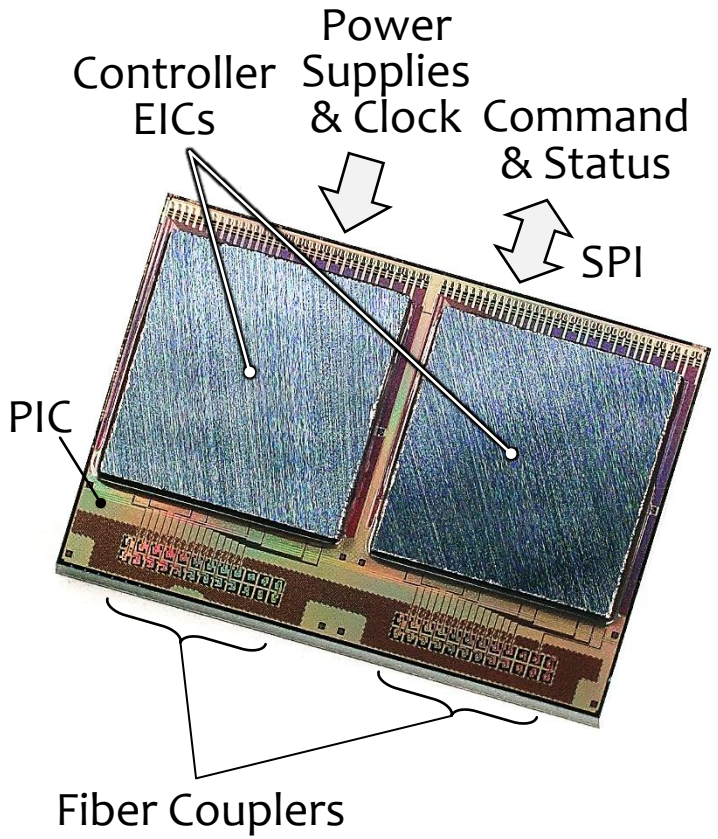
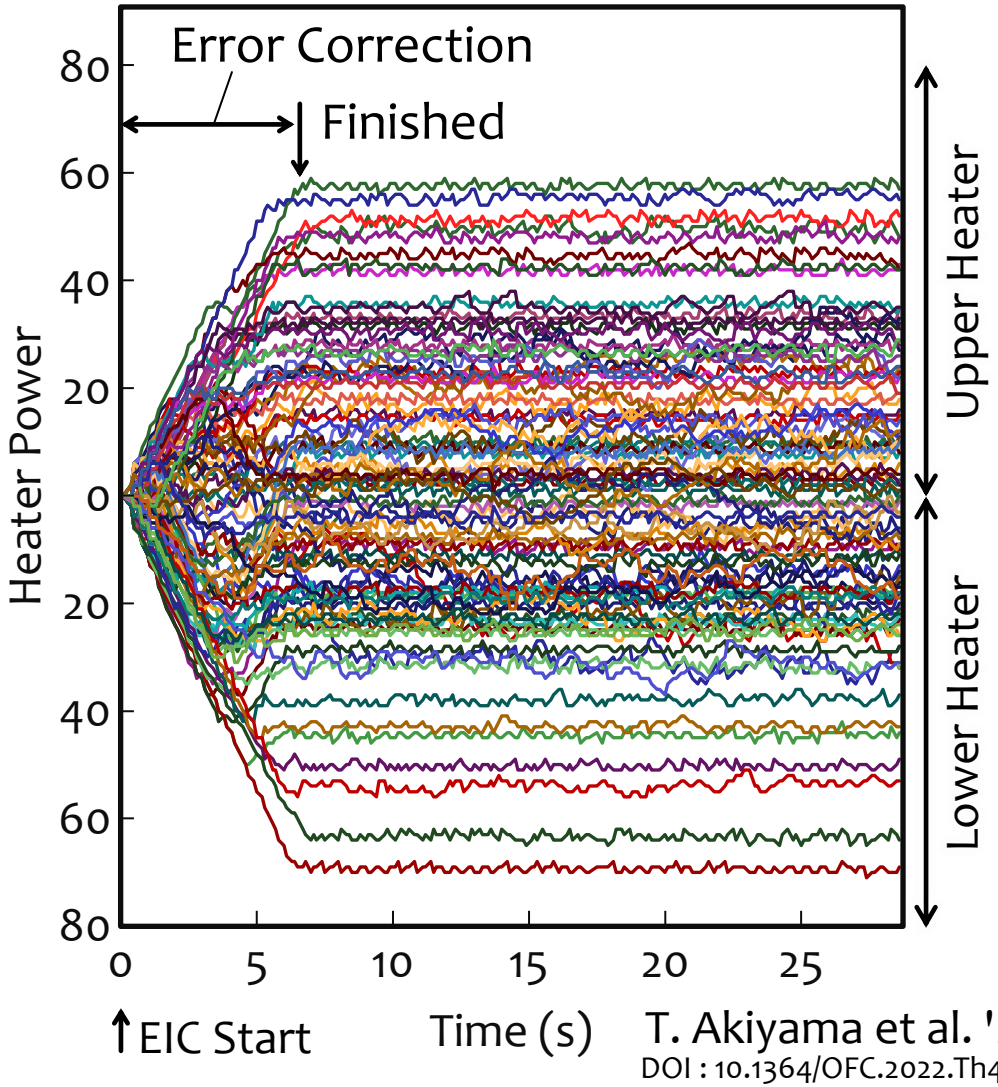
PIC+EIC Assembly



An Example for 1st Order 32 Ports for Low Spectrum Efficiency in O-band WDM

Demultiplexing



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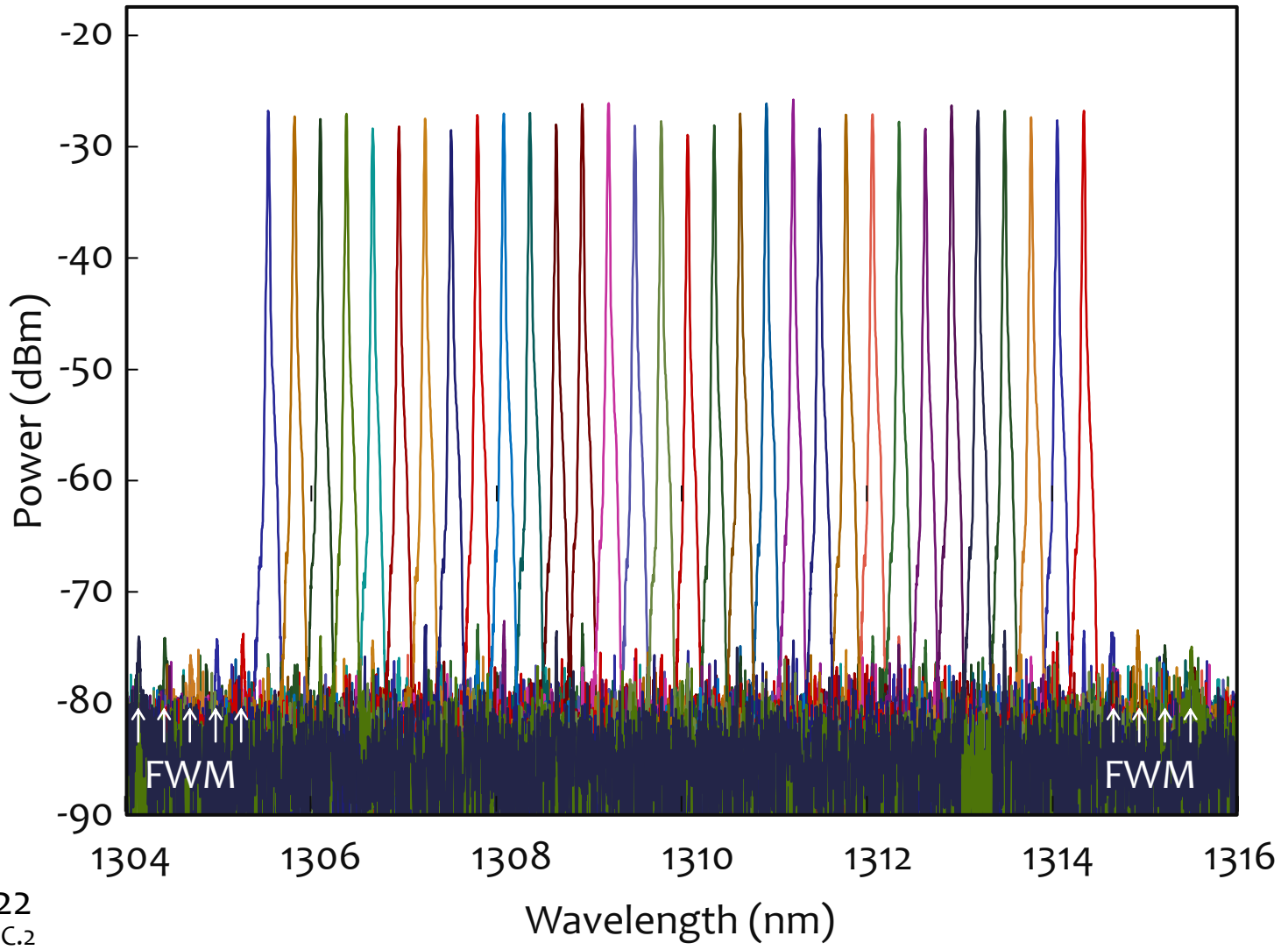

An Example for 1st Order 32 Ports for Low Spectrum Efficiency in O-band WDM

Summary

New Generation Transceiver Architecture Based on Optical DAC and CAT Technology for Capacity Scaling Toward Discentralized Computing Era

1 Use of Parallelism to Reduce Light Source & Driver Power Consumptions

D/A & E/O Conversion Losses Reduced
Combining & Splitting Losses Reduced by CAT Technology

2 Offloading DSP Spectrum Shaping into Optics by CAT Technology to Reduce DAC & ADC Power Consumptions

DAC Bit Count↓ 5→2 ⇒ DAC Power Consumption↓ 1/8x
DAC Noise↓ -6 dB ⇒ ADC Power Consumption↓ (ENOB↓)
Loss Compensated by PAPR↓ 10→4 dB & Only Slight↑ of Light Source & Driver Power

3 Power Efficient Optical D/A Converter

Acknowledgment

This presentation is based on results obtained from a project, JPNP16007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO).