Speeding VCSEL Feedback

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CS International Conference

April 17th 2024

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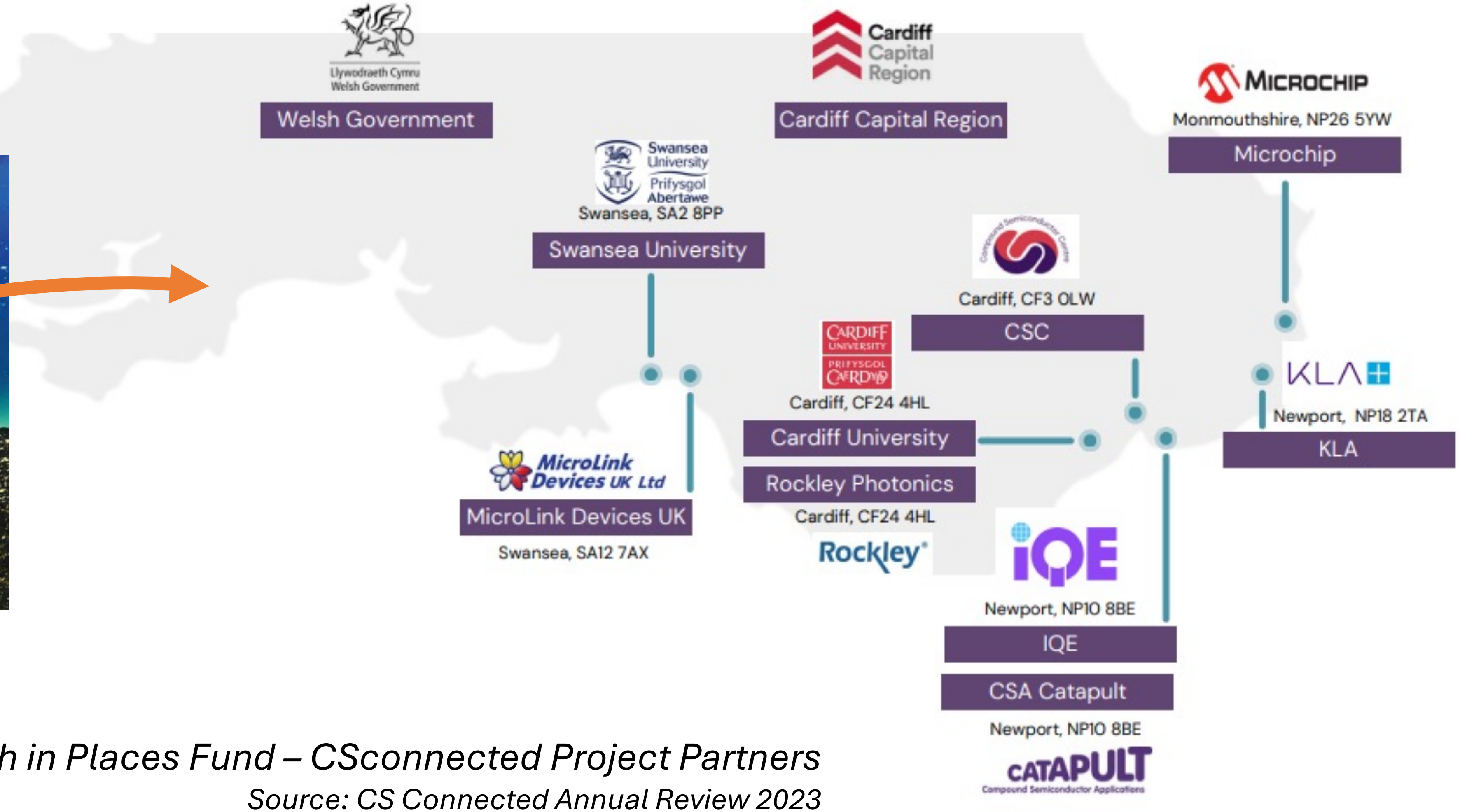
South Wales CS Cluster

Source: *Photonics Leadership Group (PLG), UK Photonics 2023*



Strength in Places Fund – CSconnected Project Partners

Source: CS Connected Annual Review 2023

Institute for Compound Semiconductors

- Housed at Cardiff University's Translational Research Hub
- 12 process engineers/technicians
- Open access facility
- 200 mm (8-inch) capability
- 1350 m^2 clean room
- Bridging the gap between R&D and industry

Outline

- Motivation
- Quick VCSELs (QuickSELs)
- Device Qualification
- Wafer-Scale Analysis
- Conclusion

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VCSEL Product Development Cycle

Epi-layer design
- Active region
- DBRs
- Oxidation layer
- Doping
- Interfacial grading
- Modelling
- Optimisation

Epitaxial growth
- Substrate
- MOVPE calibration
- Test structure growth
- Full VCSEL growth
- Post growth:
  - FP & PL characterisation
  - Defect scanning & destructive characterisation

Wafer processing
- Reticle design & mask taping
- Contact metallisation
- Annealling
- Mesa etching
- Selective oxidation
- Passivation & planarisation
- Back-end

Testing & characterisation
- Assembly/packaging
- Wafer-level test
- Sampling
- Characterisation
  - PIV-spectra
  - Beam quality
  - Linewidth
  - Bandwidth

Reliability & chip qualification
- Full package assembly
- Stress conditions
- Thermal testing
- Mechanical testing
- Failure analysis
- Lifetime analysis

Feedback

Cycle of roughly 8 months*

**Adapted from: VCSEL Industry: Communication and Sensing, First Edition. B. D. Padullaparthi, J. A. Tatum and K. Iga. Published 2022 by John Wiley & Sons, Inc. Image Copyright© Photonics Components DFM Ltd.*

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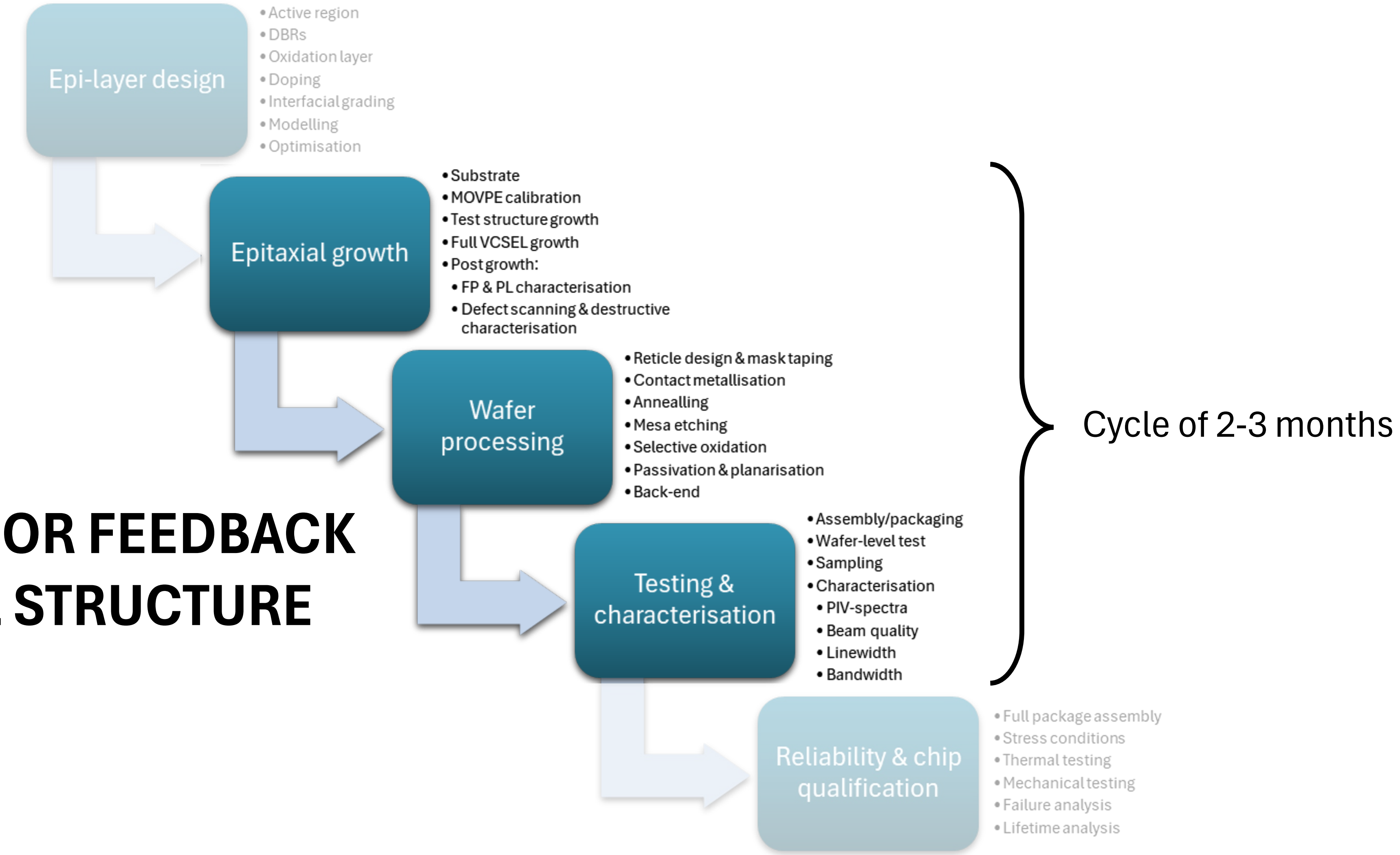
VCSEL Product Development Cycle



2 – 3 MONTHS FOR FEEDBACK ON EPITAXIAL STRUCTURE

VCSEL Product Development Cycle

Need for a Quick-VCSEL structure which reduces processing time whilst preserving device performance

Assess quality & uniformity of epitaxial material through wafer-scale testing of QuickSELs

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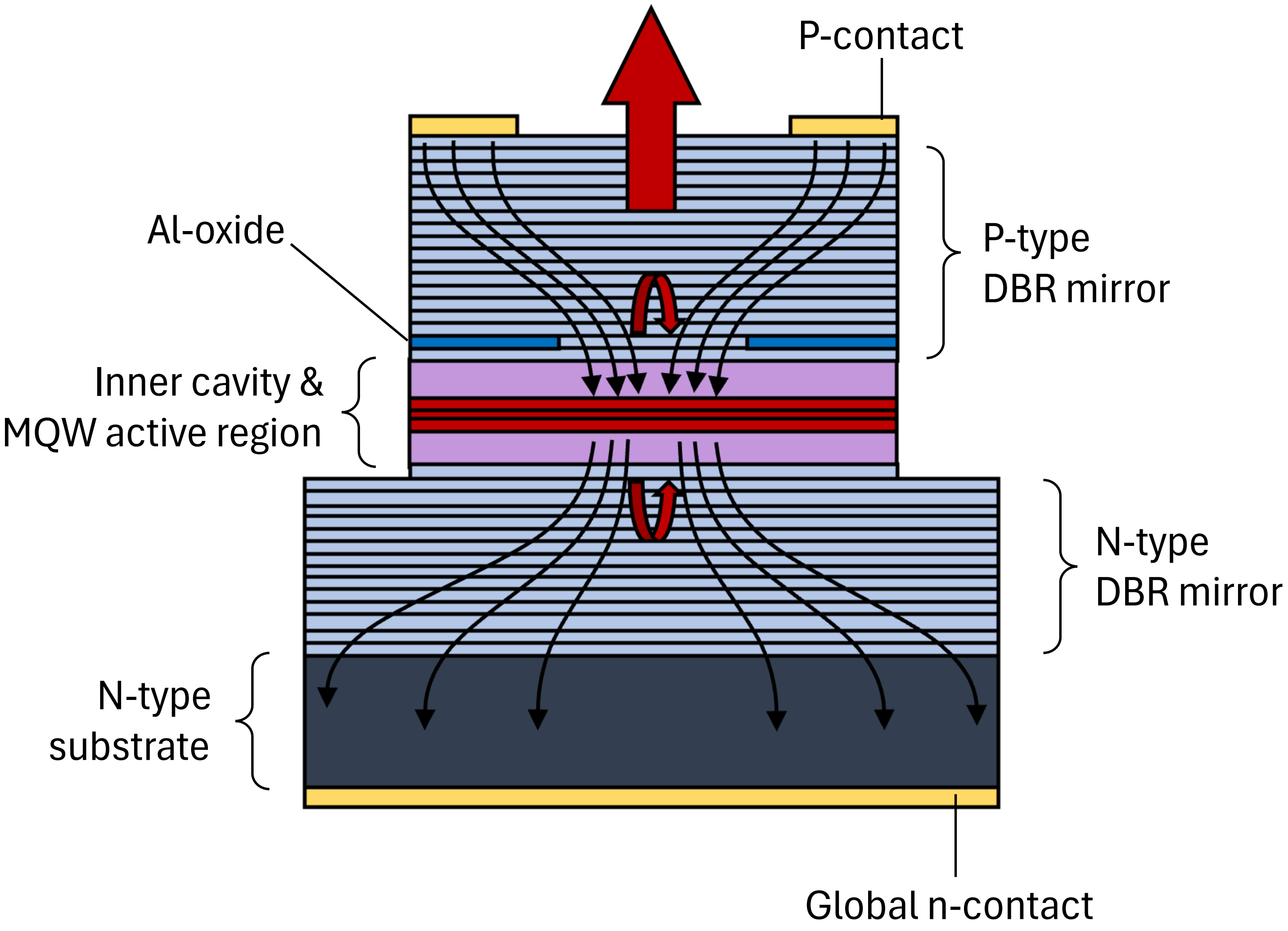
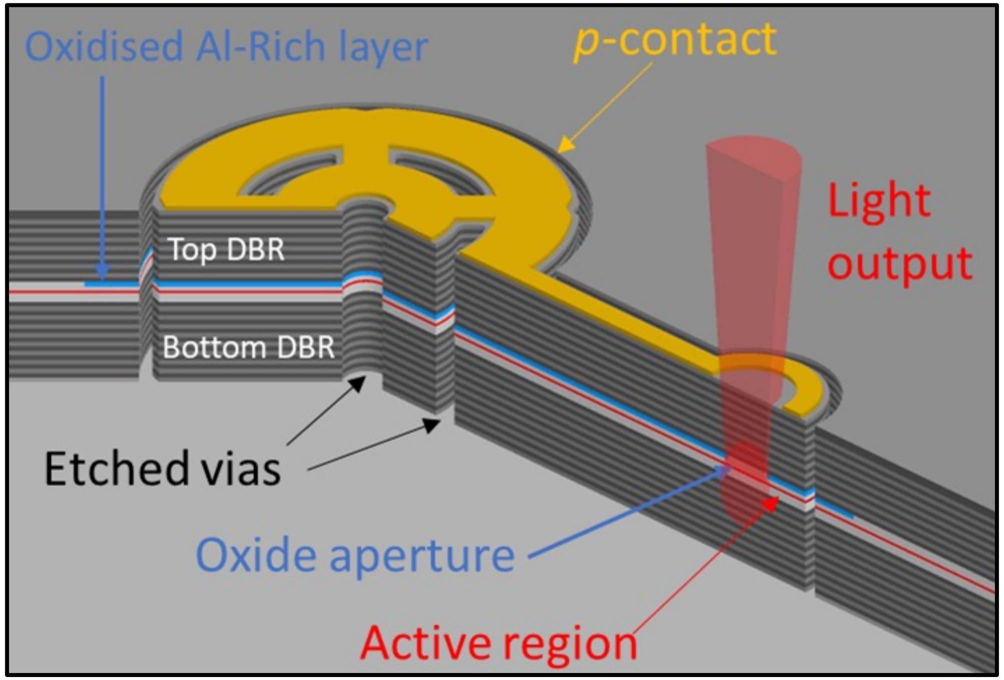
Typical VCSEL Structure



The QuickSEL



Total processing time – 24 hours

(vs 24-36 hours per mask layer for a full high performance VCSEL = up to 16.5 days for some structures)

"VCSEL Quick Fabrication for Assessment of Large Diameter Epitaxial Wafers," IEEE Phot. J, 14, 3, 1-10, (2022), doi:10.1109/JPHOT.2022.3169032.

QuickSEL Device Variations

Market	Requirements	Growth	Device	Where?
Sensing/LiDAR	High-power	Doped substrate	Global N	[1]
Atomic clocks/magnetometers	Single-mode Narrow linewidth	Anti-phase cap	Phase Cap-Etch	This work
Datacom	High-frequency modulation	Semi-insulating substrate	Co-Planar N	This work

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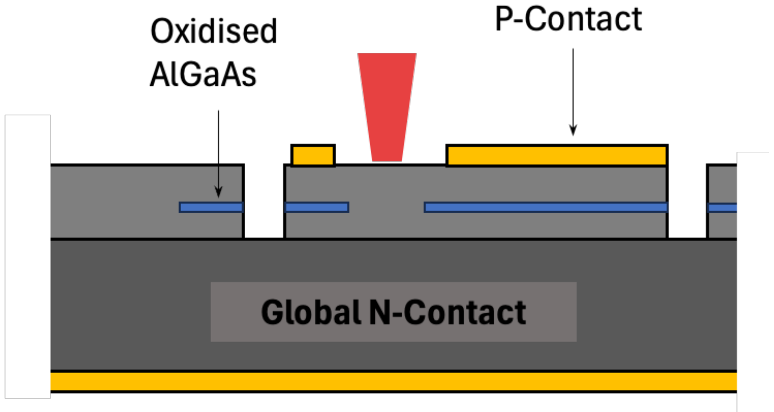
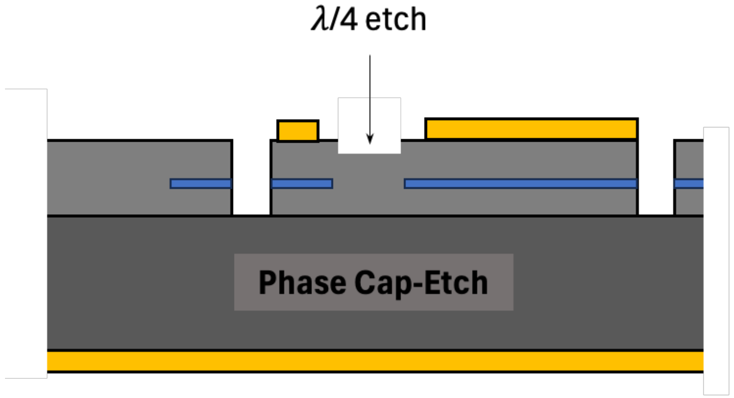
QuickSEL Device Variations

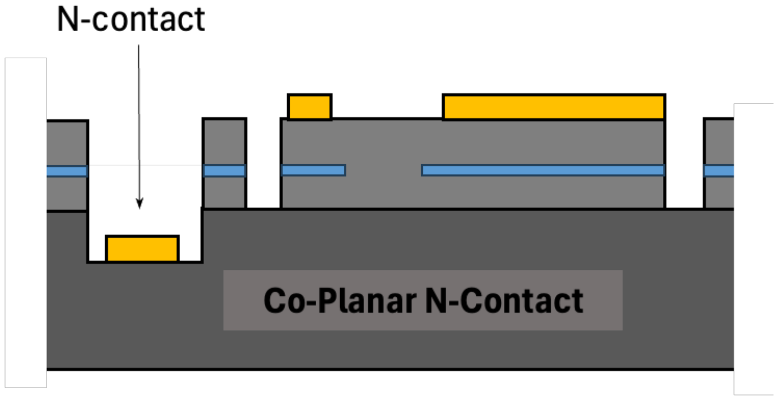
3D Sensing/LiDAR



Atomic Clocks/Magnetometers



Datacom



Device	Processing Time (Hours)
Global N-Contact	24
Phase Cap-Etch	28
Co-Planar N-Contact	30
Full High-Performance Datacom	**264***

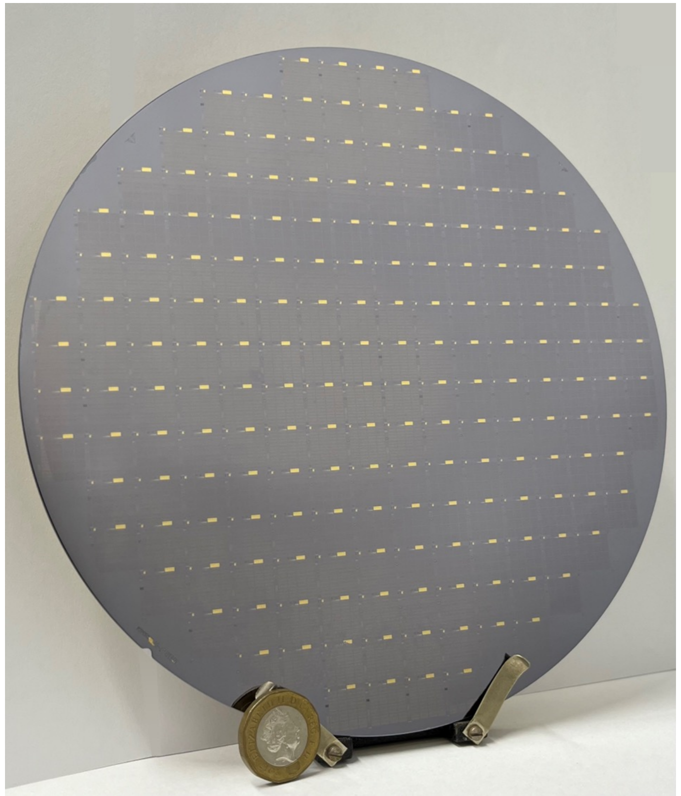
*Assumes 11 mask layers and 24 hours per mask layer as detailed in *VCSEL Industry (2022)*

Wafer Diameters

100 mm (4-inch)

150 mm (6-inch)

200 mm (8-inch)



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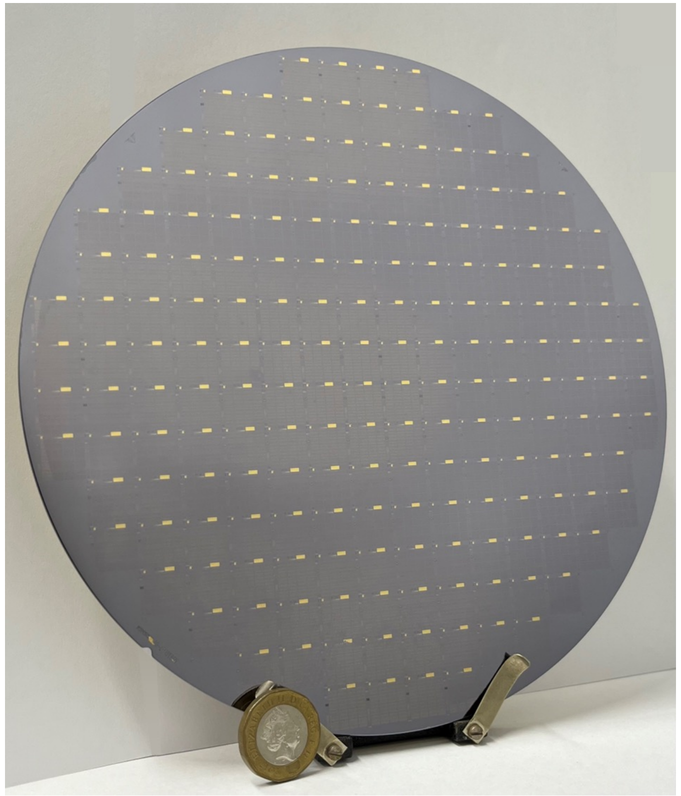
Wafer Diameters

Datacom/Atomic Sensing

100 mm (4-inch)

150 mm (6-inch)

200 mm (8-inch)



3D Sensing/LiDAR

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Outline

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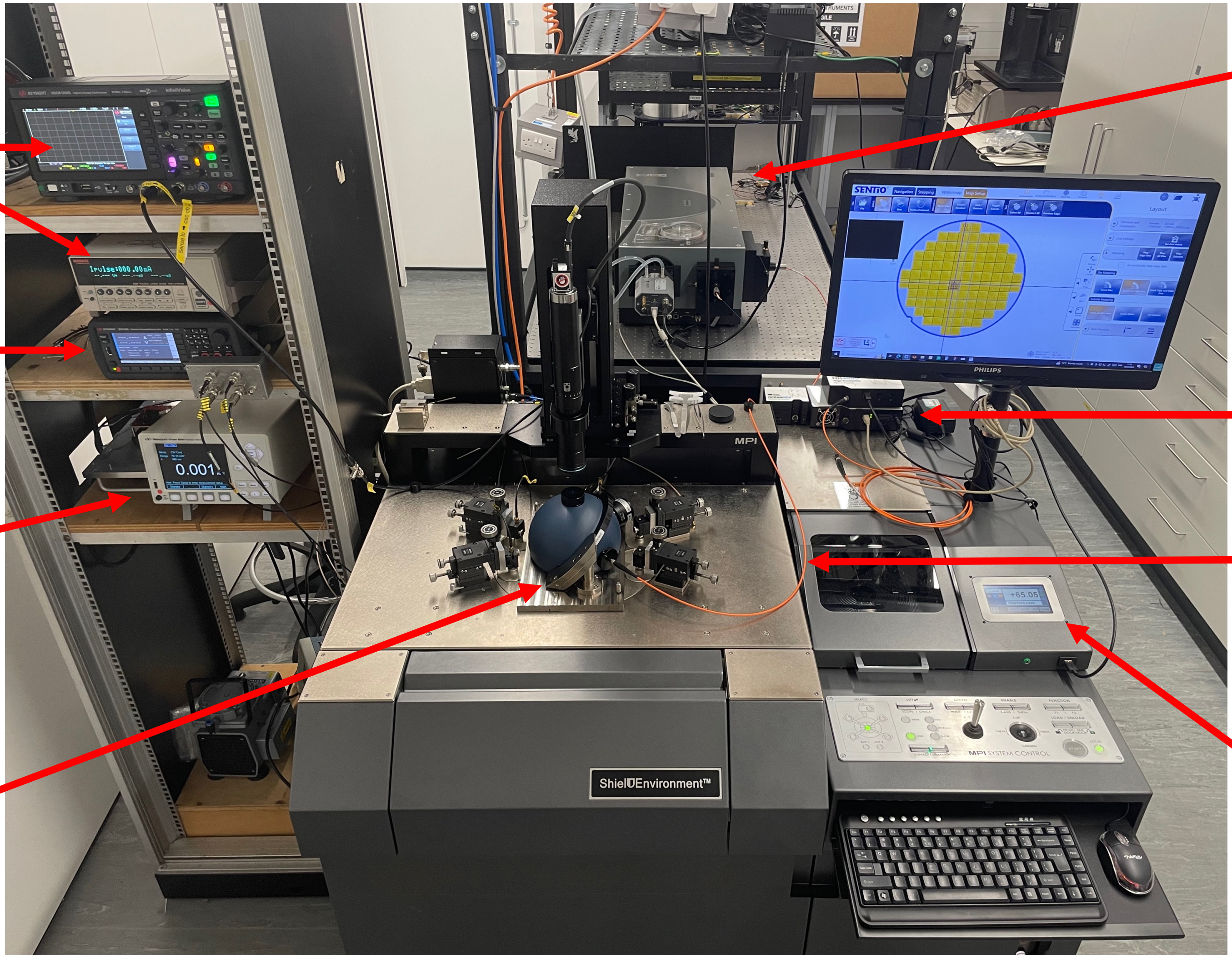
Test Setup

Pulsed current source & oscilloscope

CW source-measure unit

Calibrated power meter

Integrating sphere



Low noise spectrograph

High-resolution spectrometers

Fibre tap

Chuck temperature control (up to 200°C)

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Device Qualification

Adapt QuickSEL device structure **to allow wafer-scale analysis** of anti-phase structures and structures on semi-insulating substrates

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QuickSEL Device Variations

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Atomic clocks/magnetometers	**Single-mode Narrow linewidth**	**Anti-phase cap**	**Phase Cap-Etch**	**This work**
Datacom	High-frequency modulation	Semi-insulating substrate	Co-Planar N	This work

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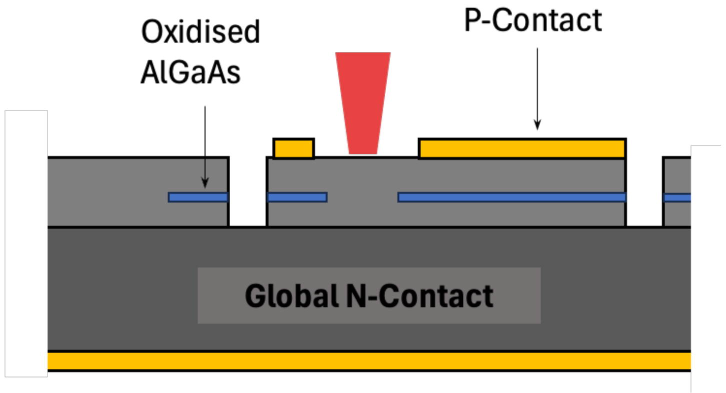
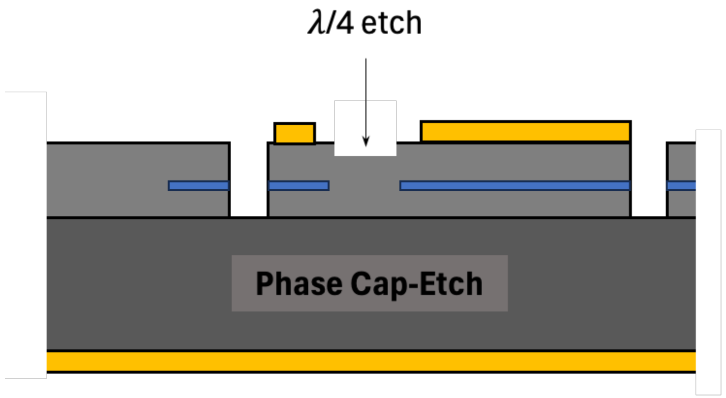
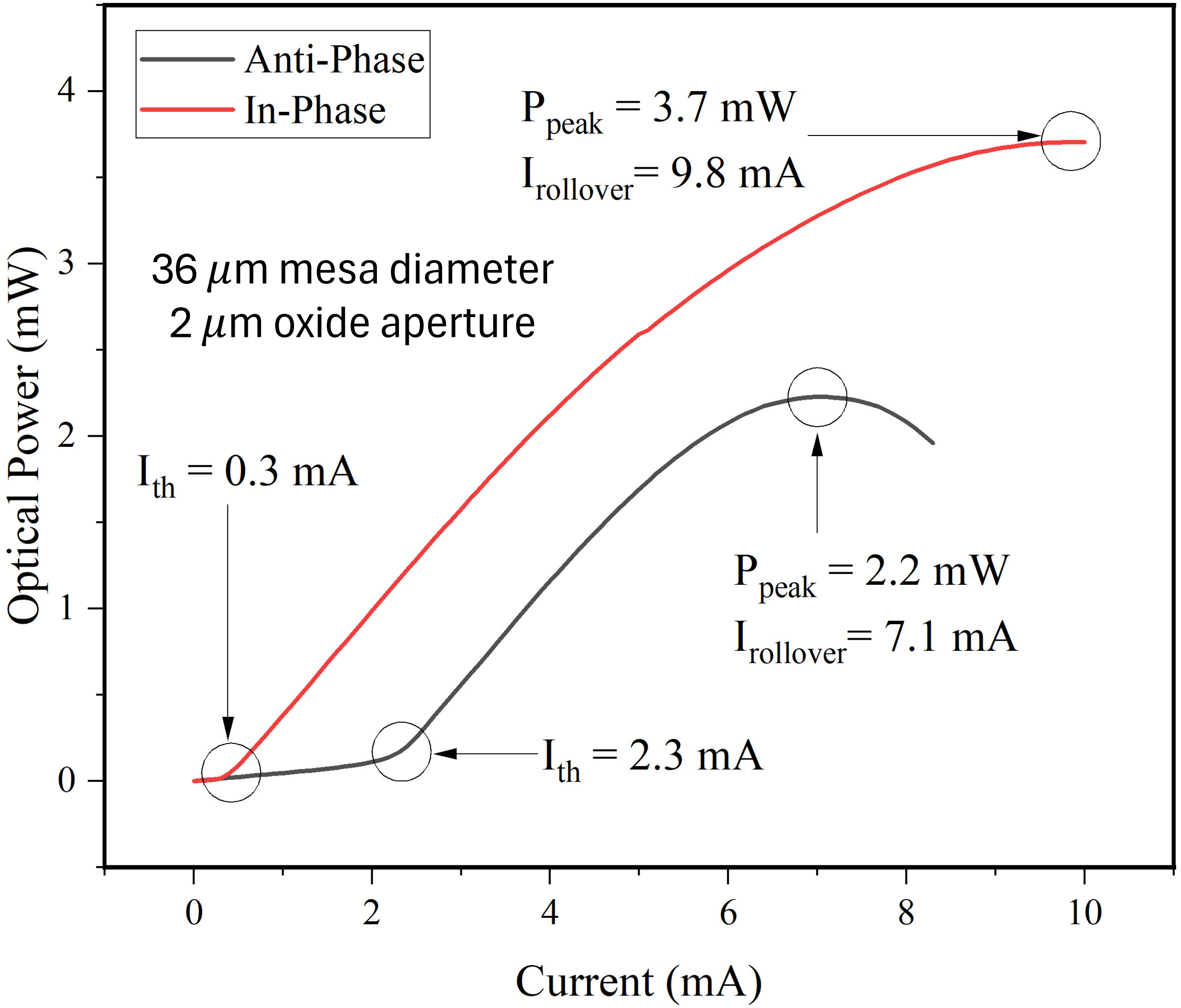
Phase Cap-Etch QuickSEL



VS





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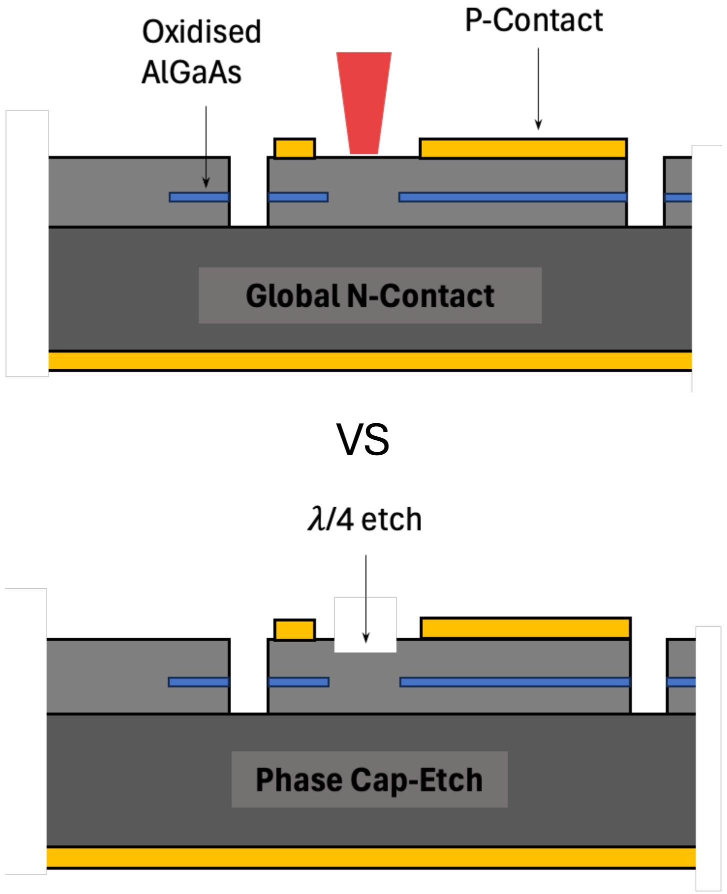

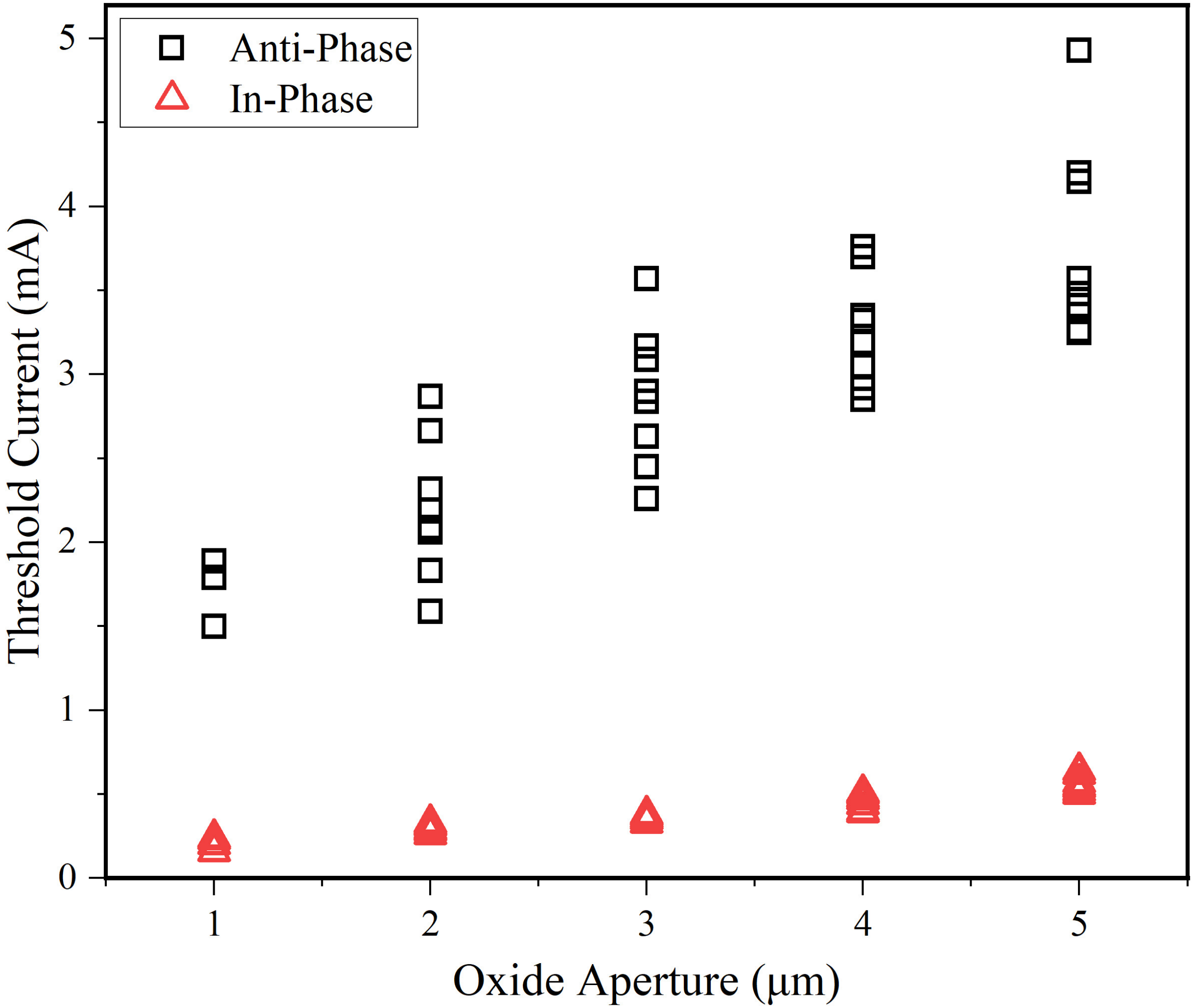

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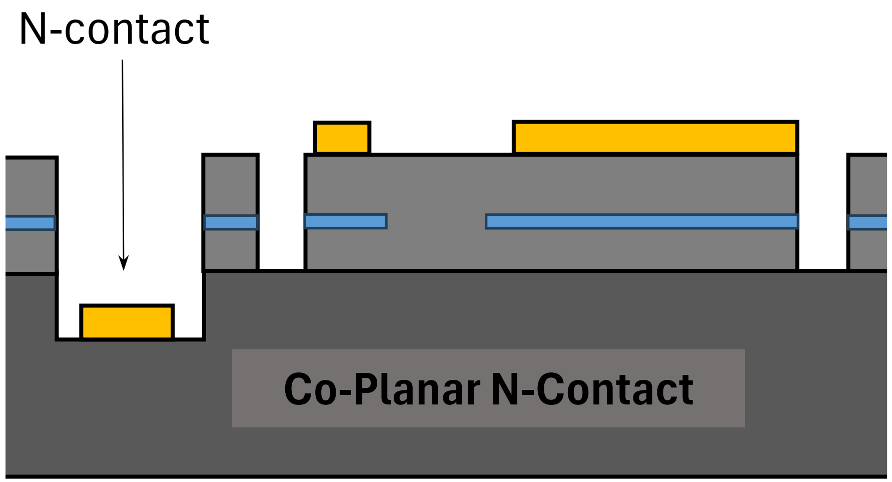
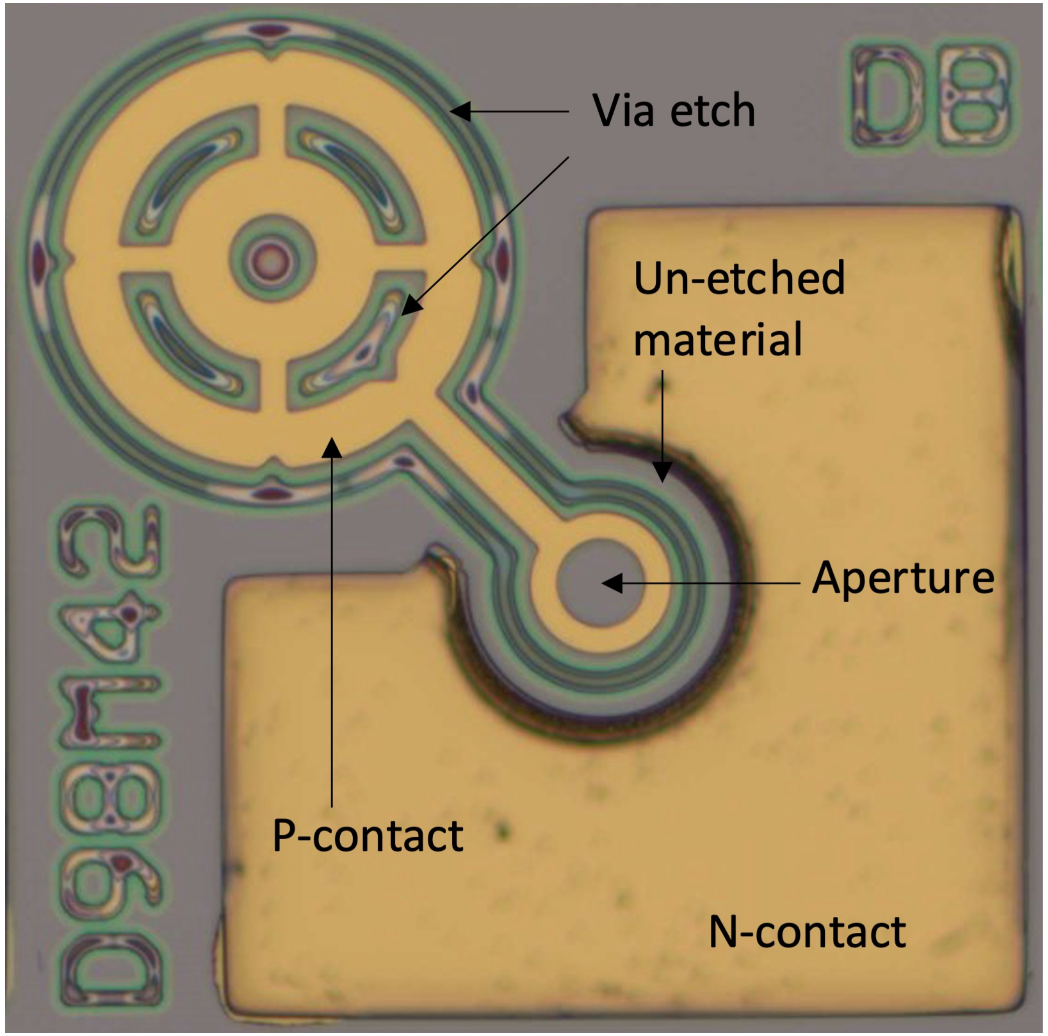
Co-Planar N-Contact QuickSEL





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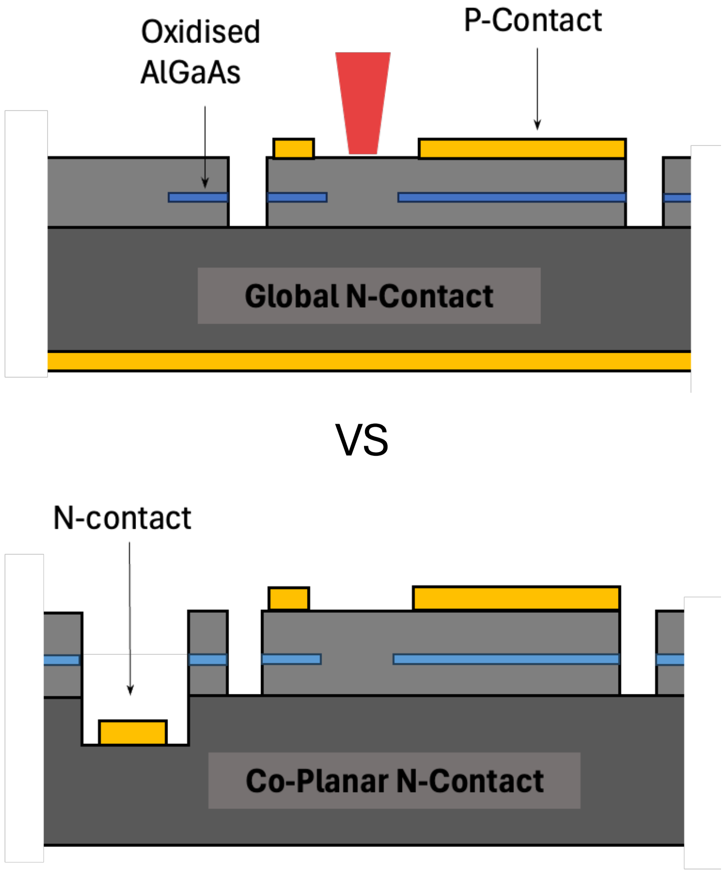

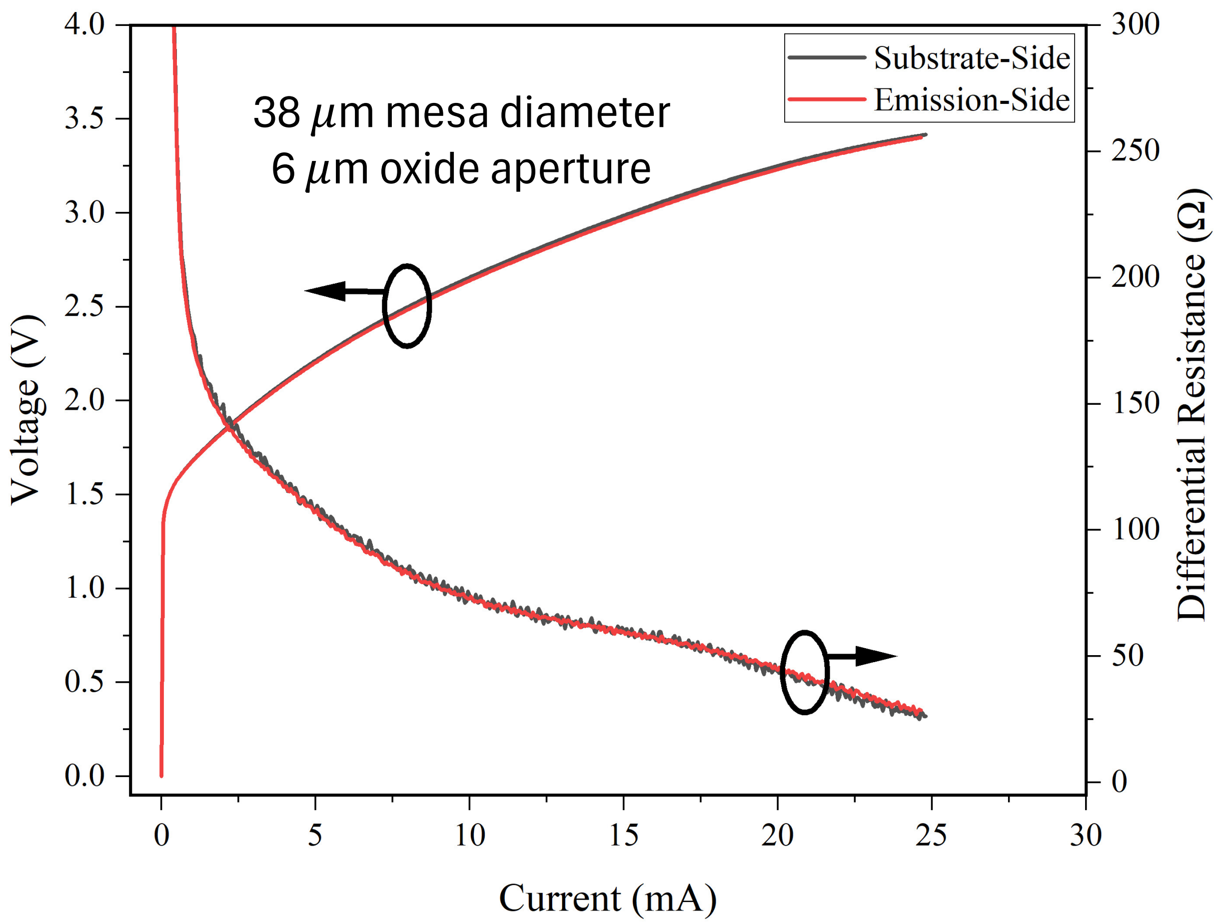

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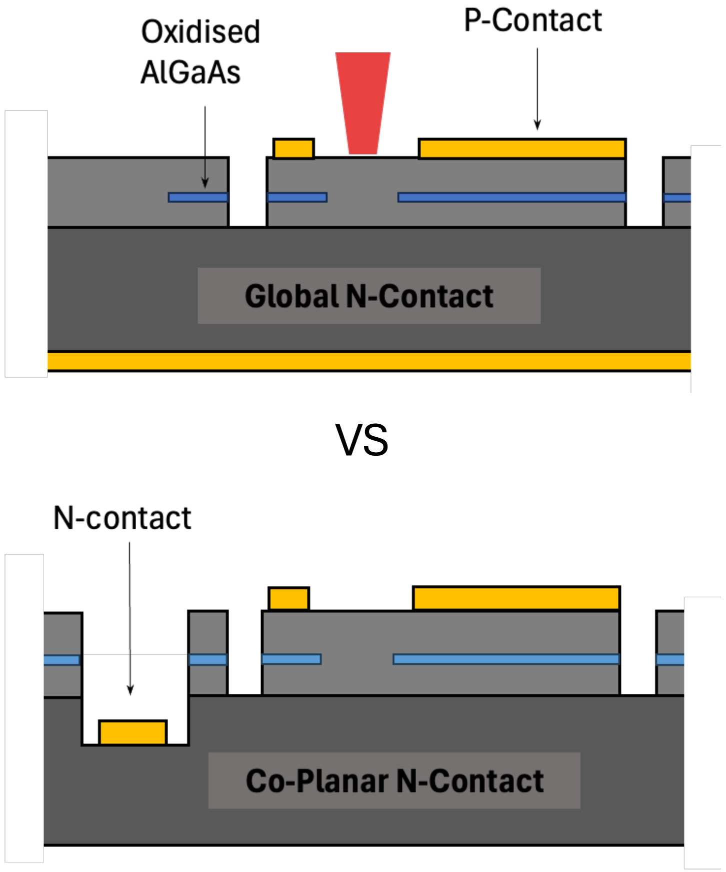
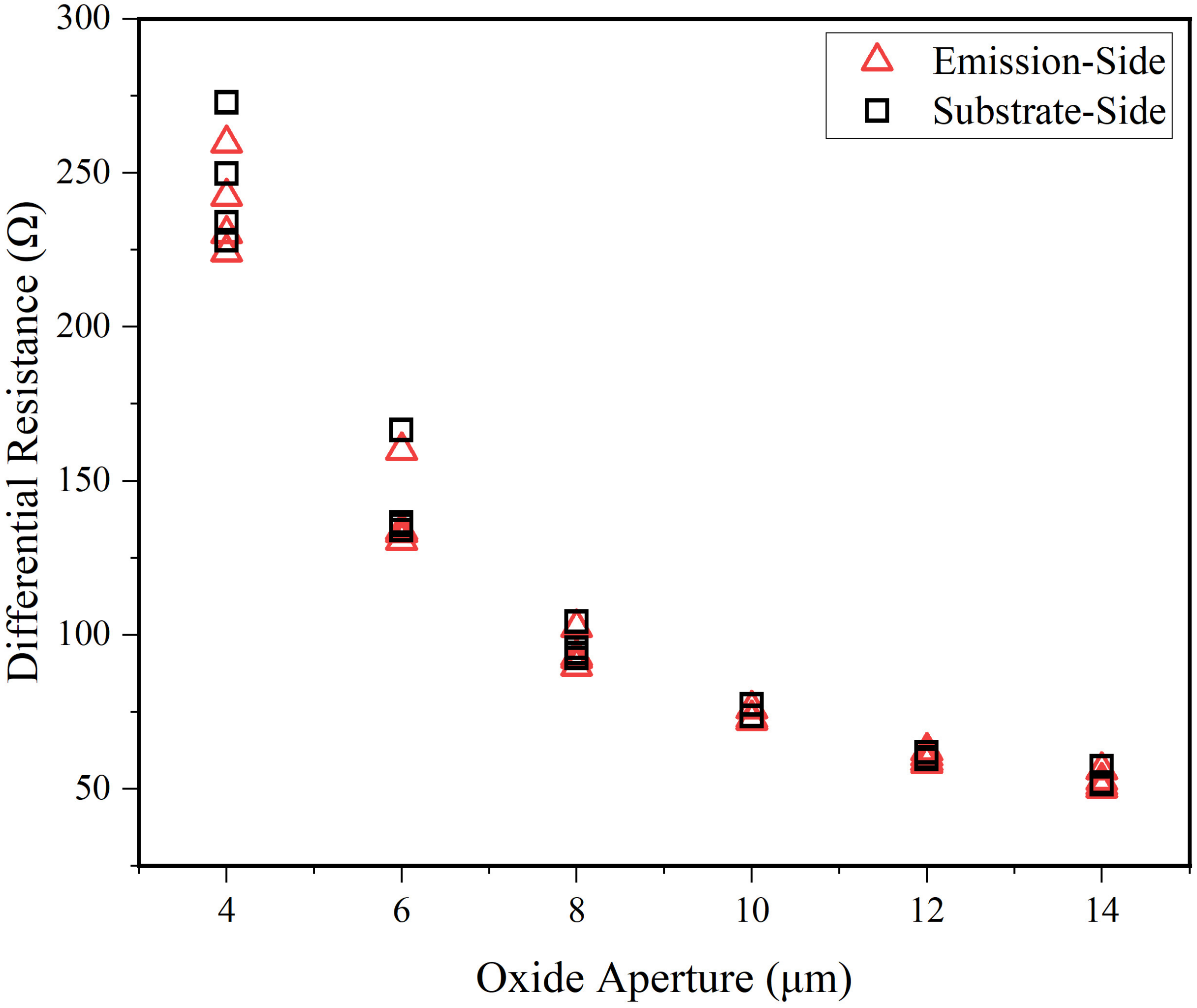
Co-Planar N-Contact QuickSEL





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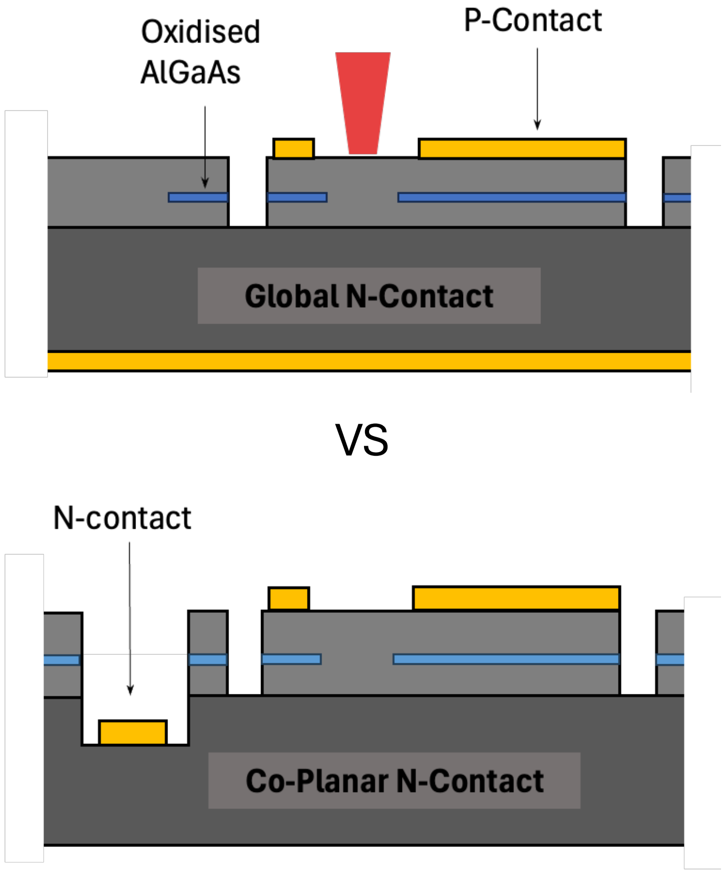

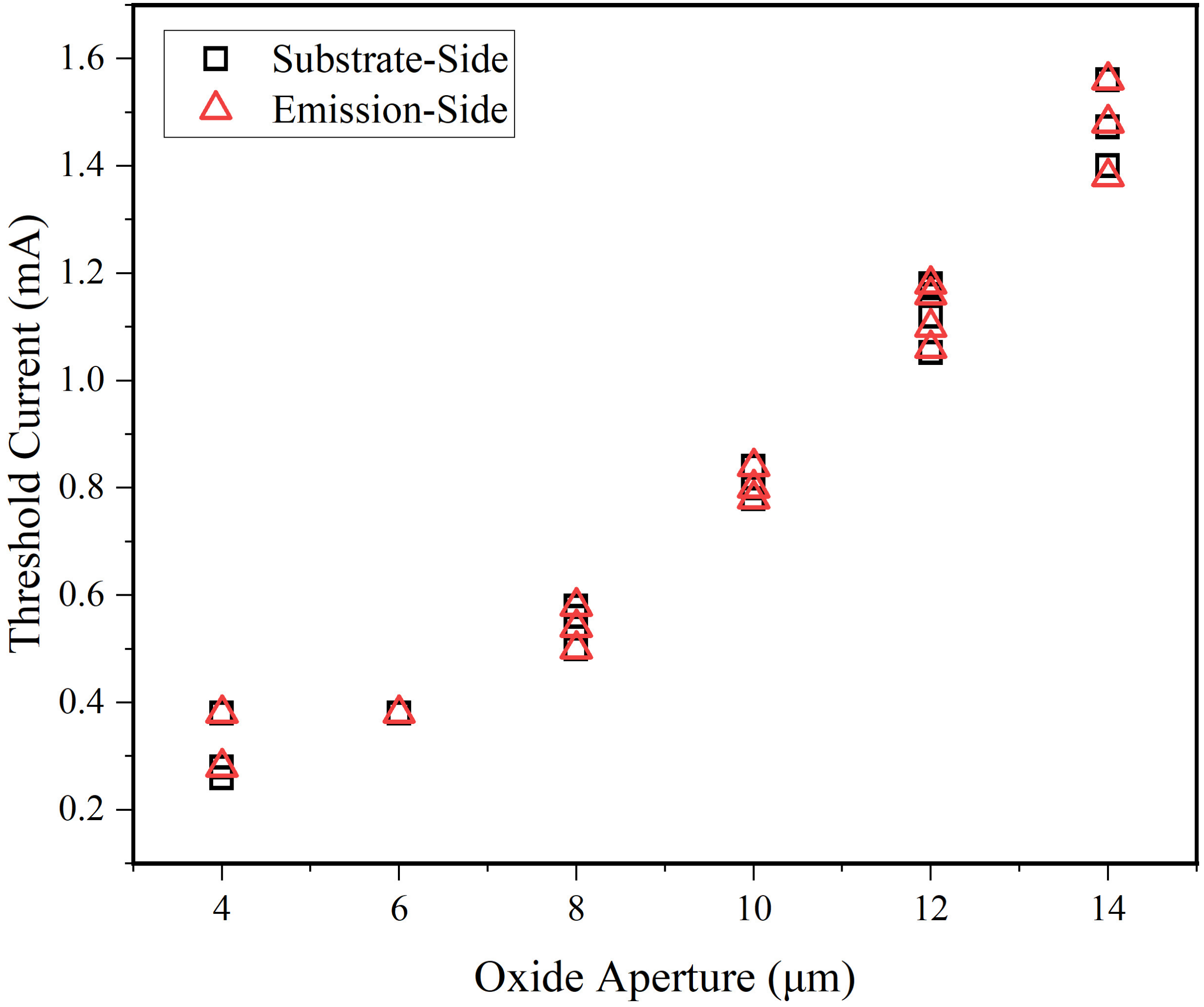

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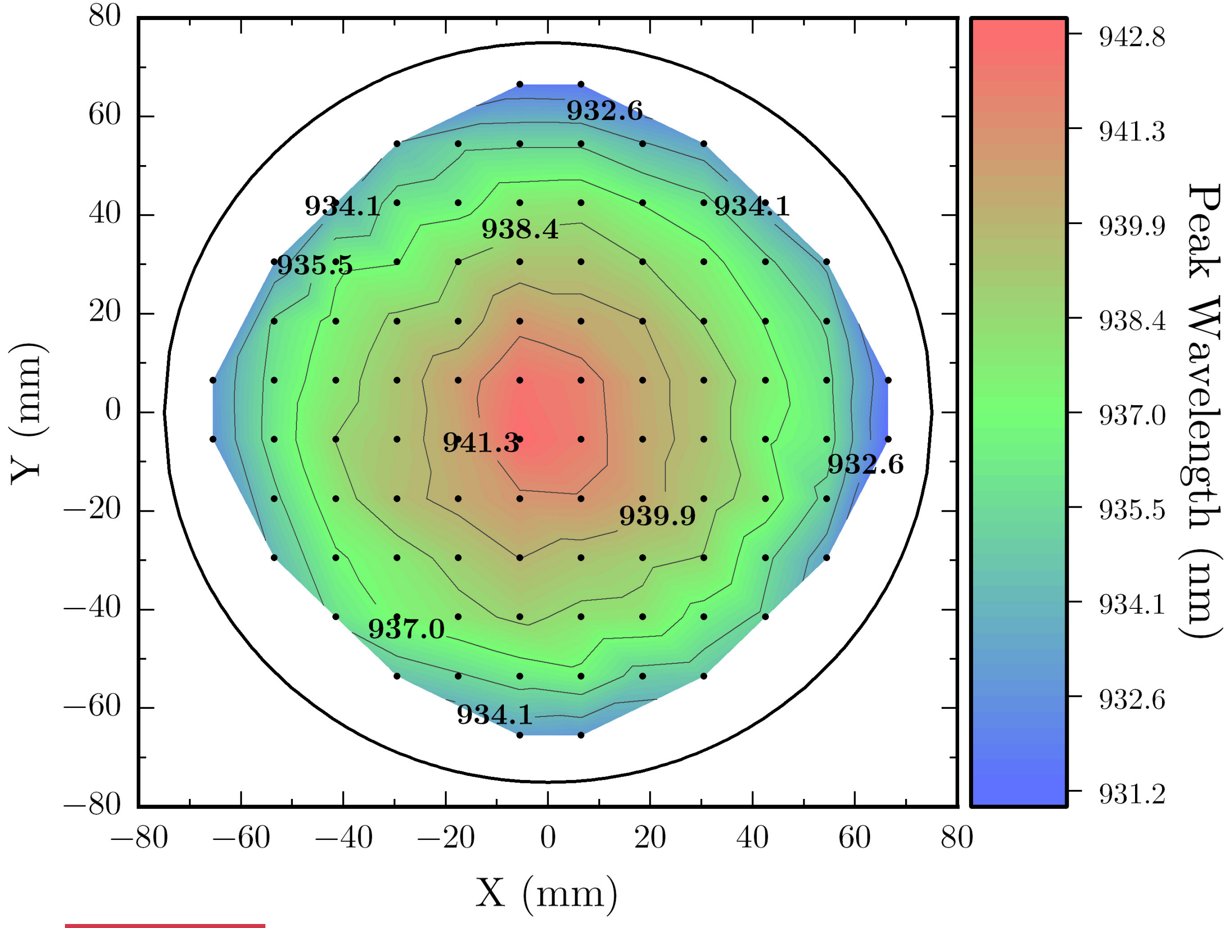
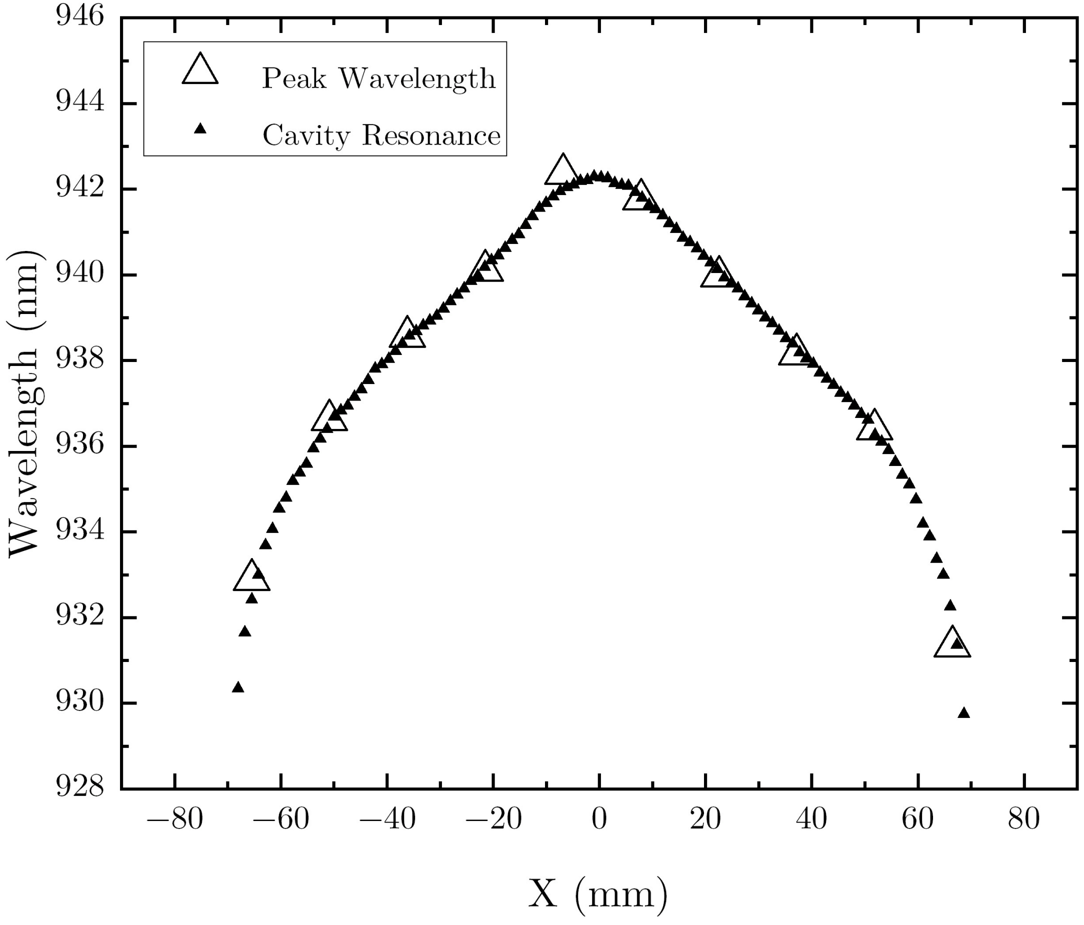
Wafer-Scale Analysis – λ





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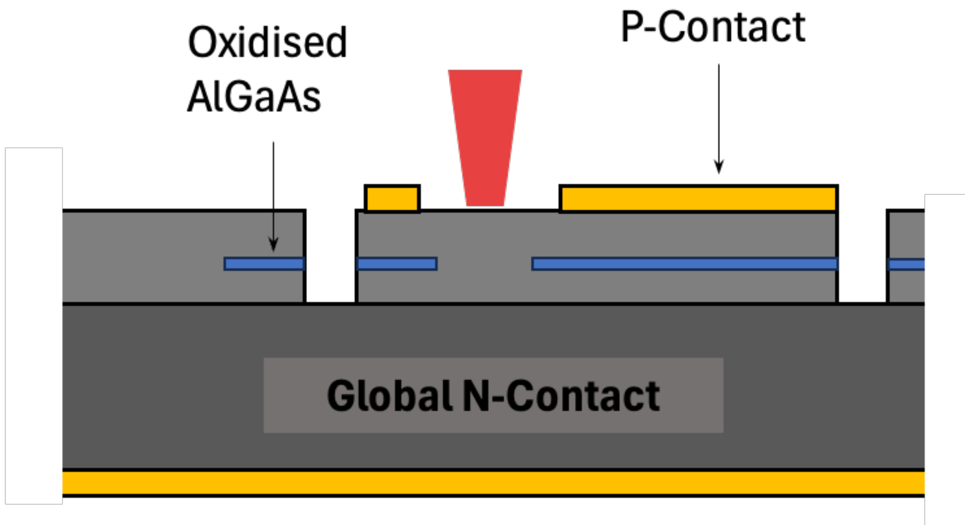
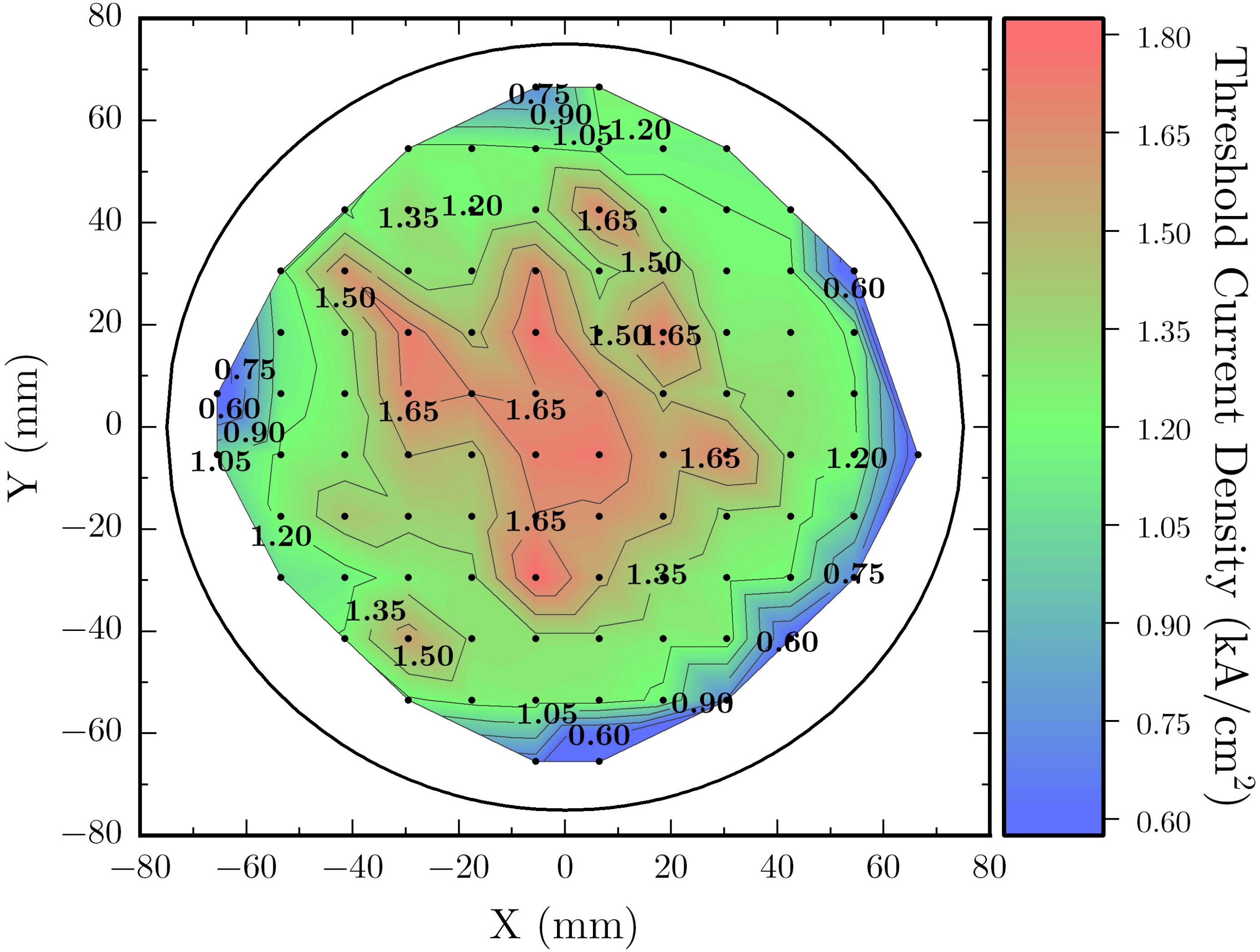
Wafer-Scale Analysis – J_{th}





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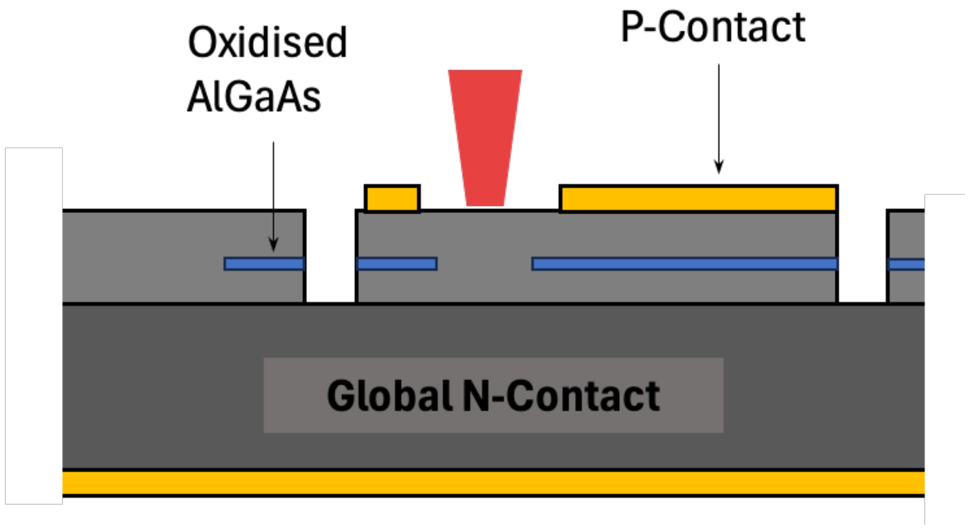

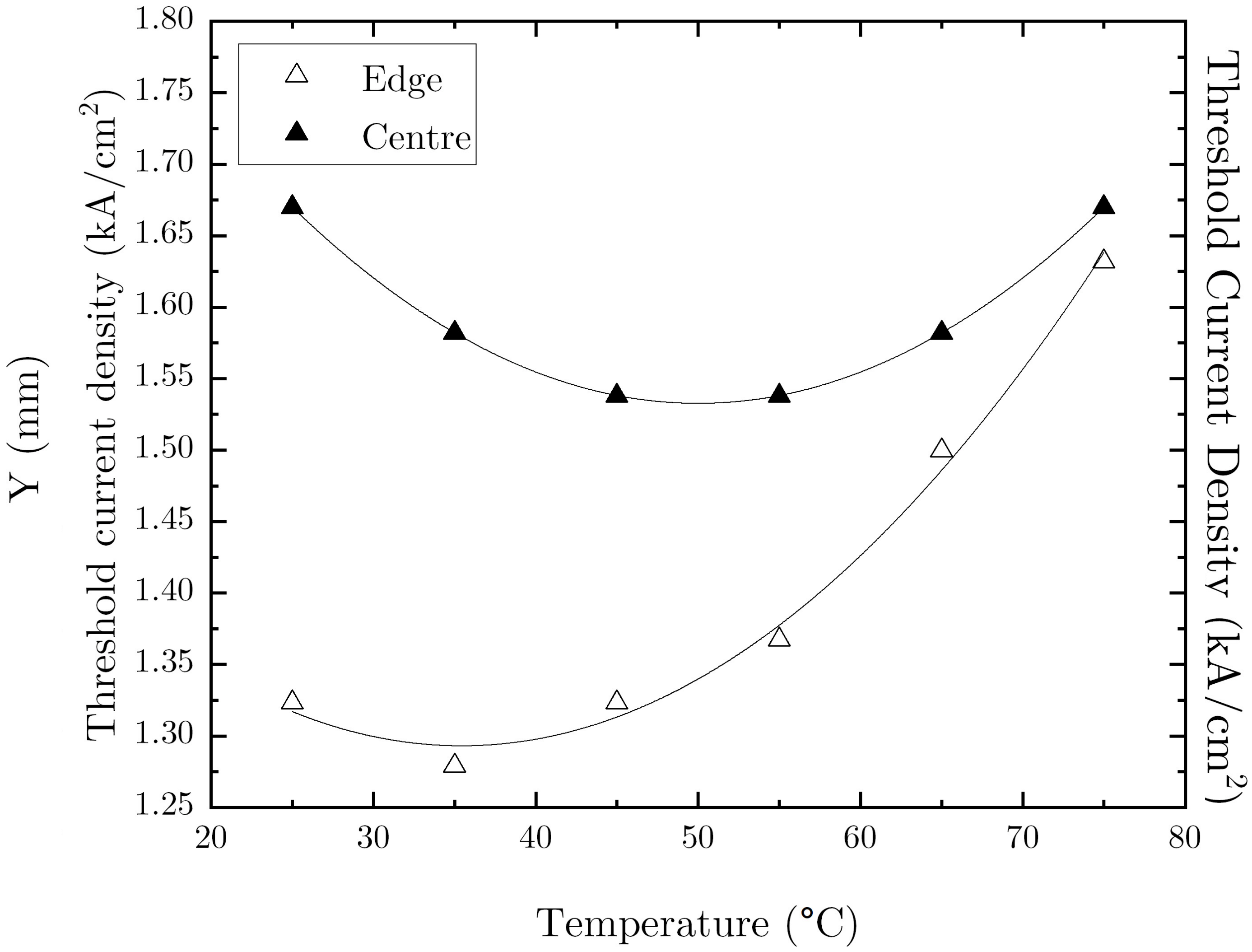

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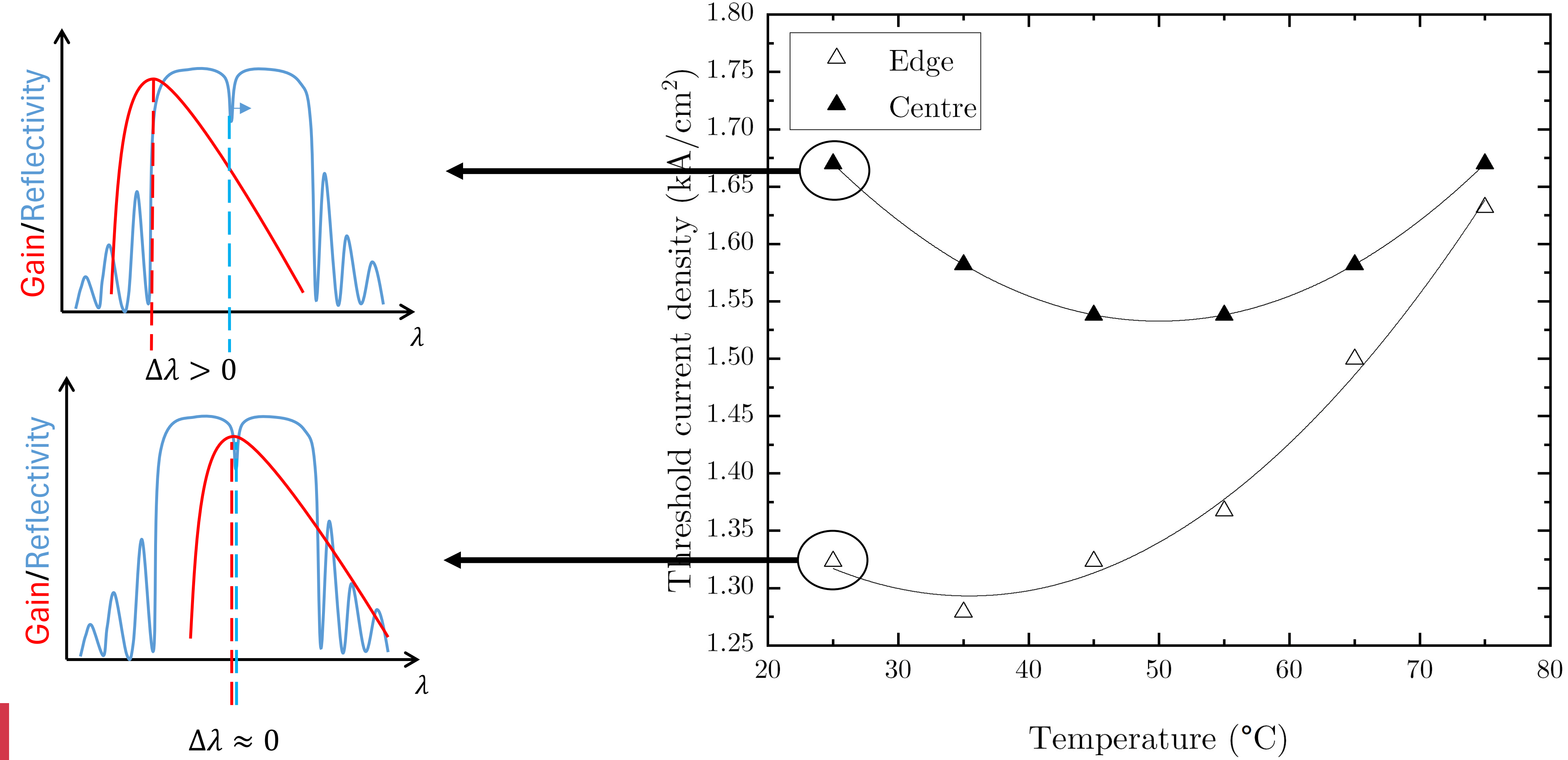
Wafer-Scale Analysis – Gain Peak Detuning



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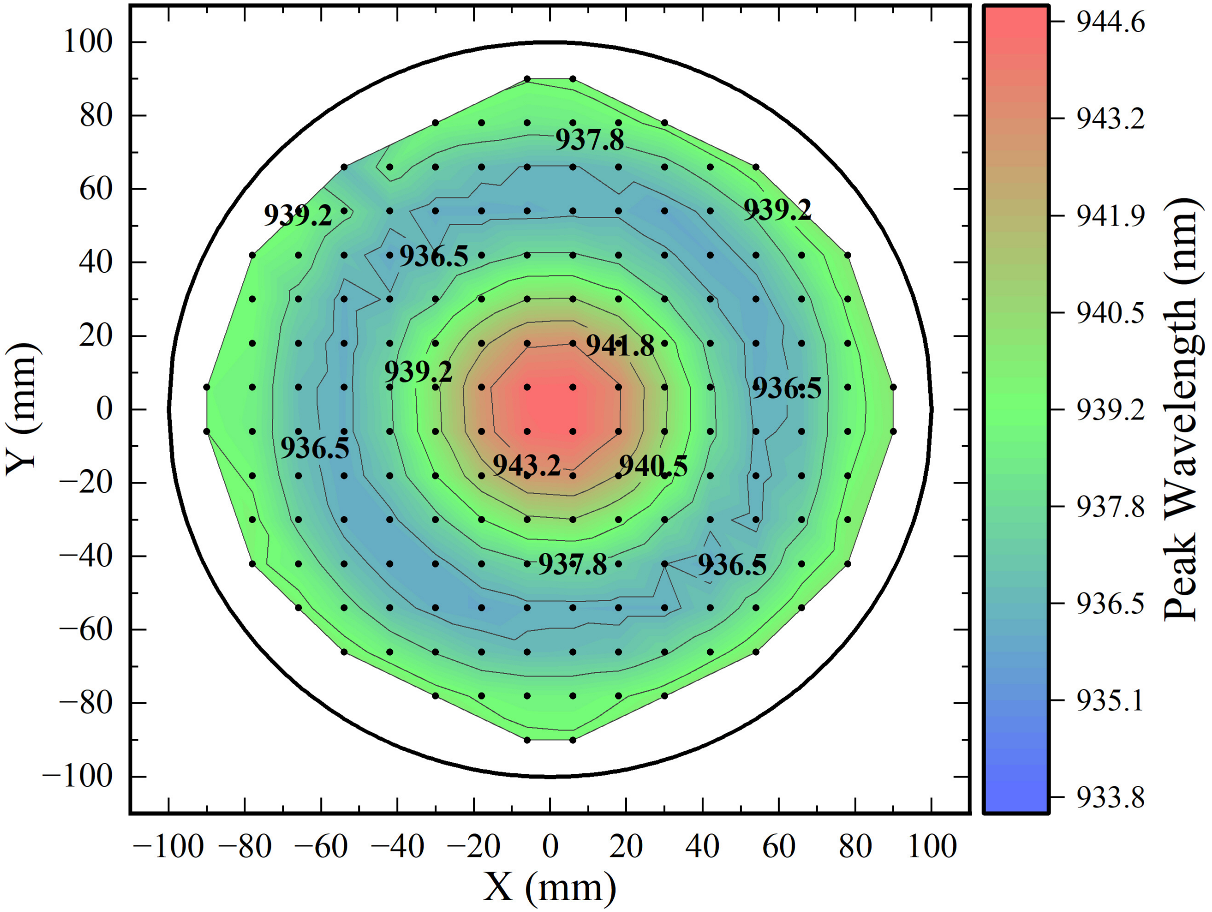
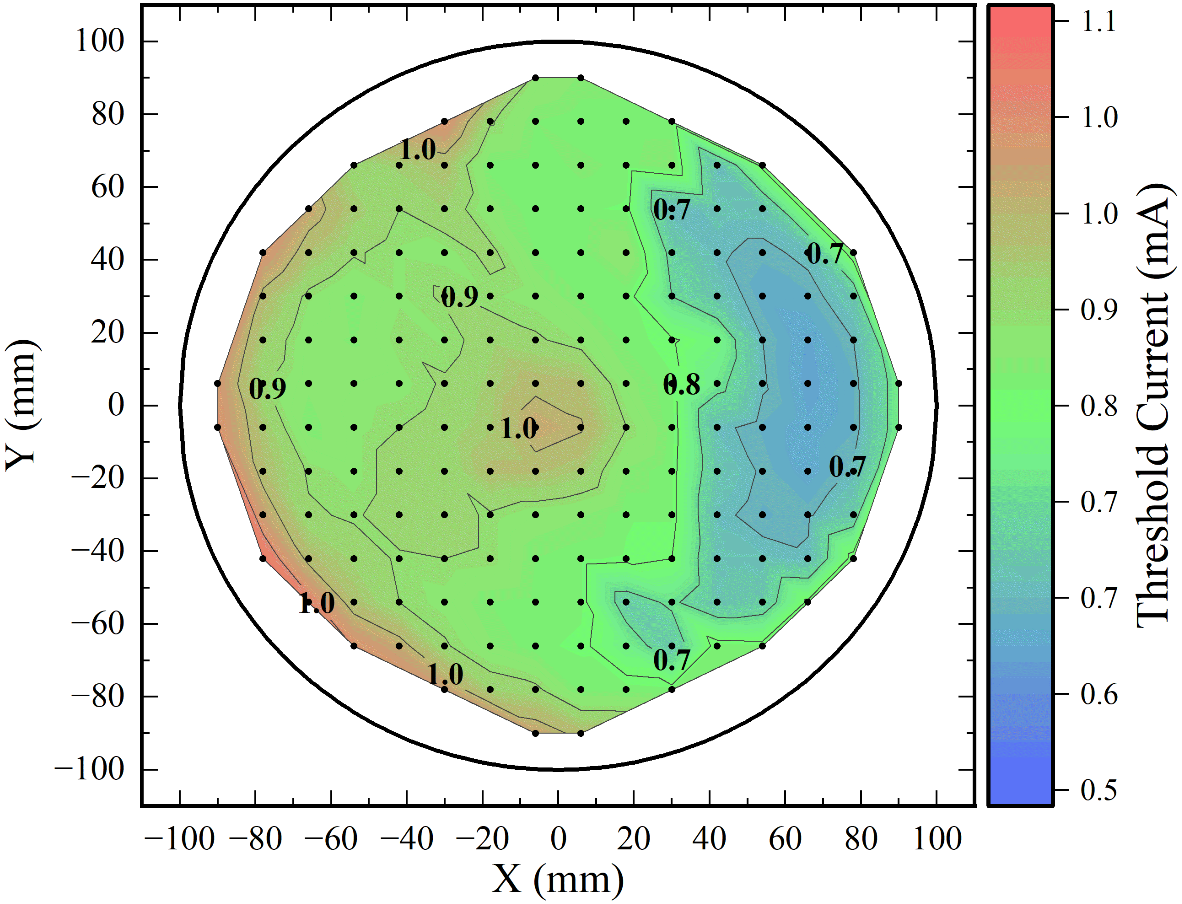
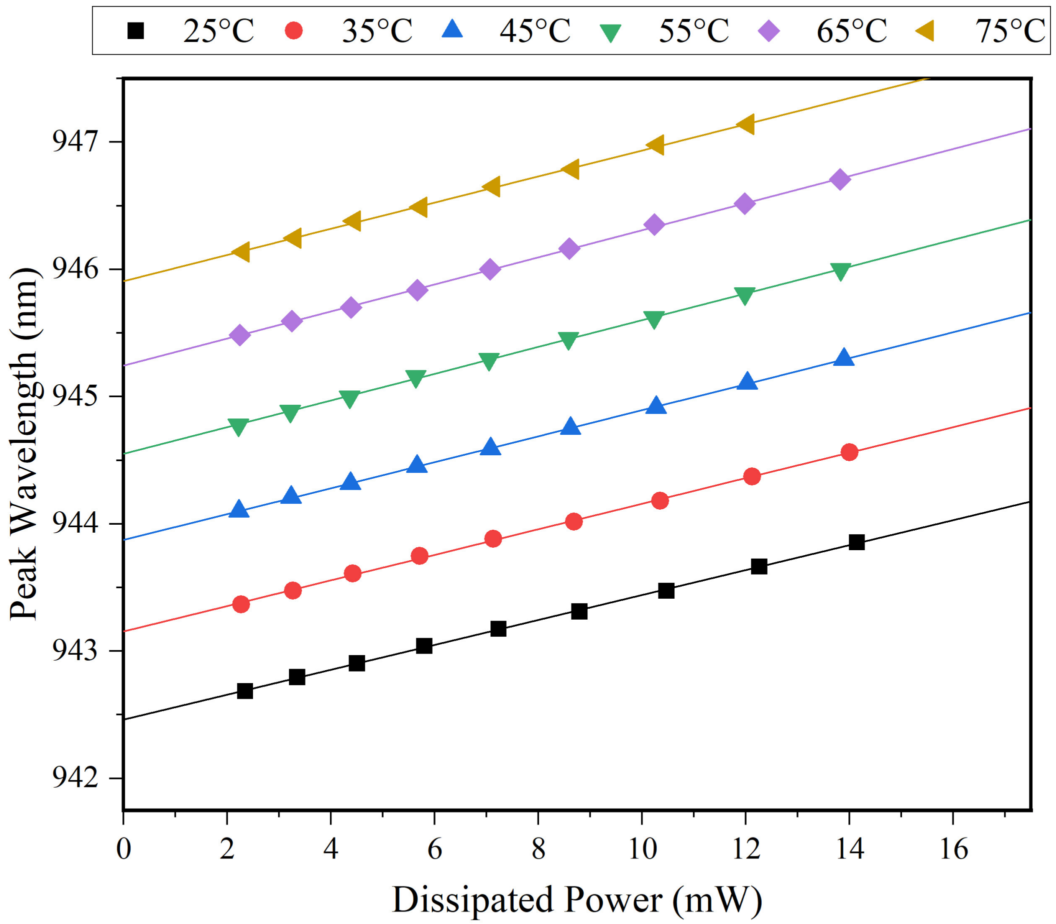
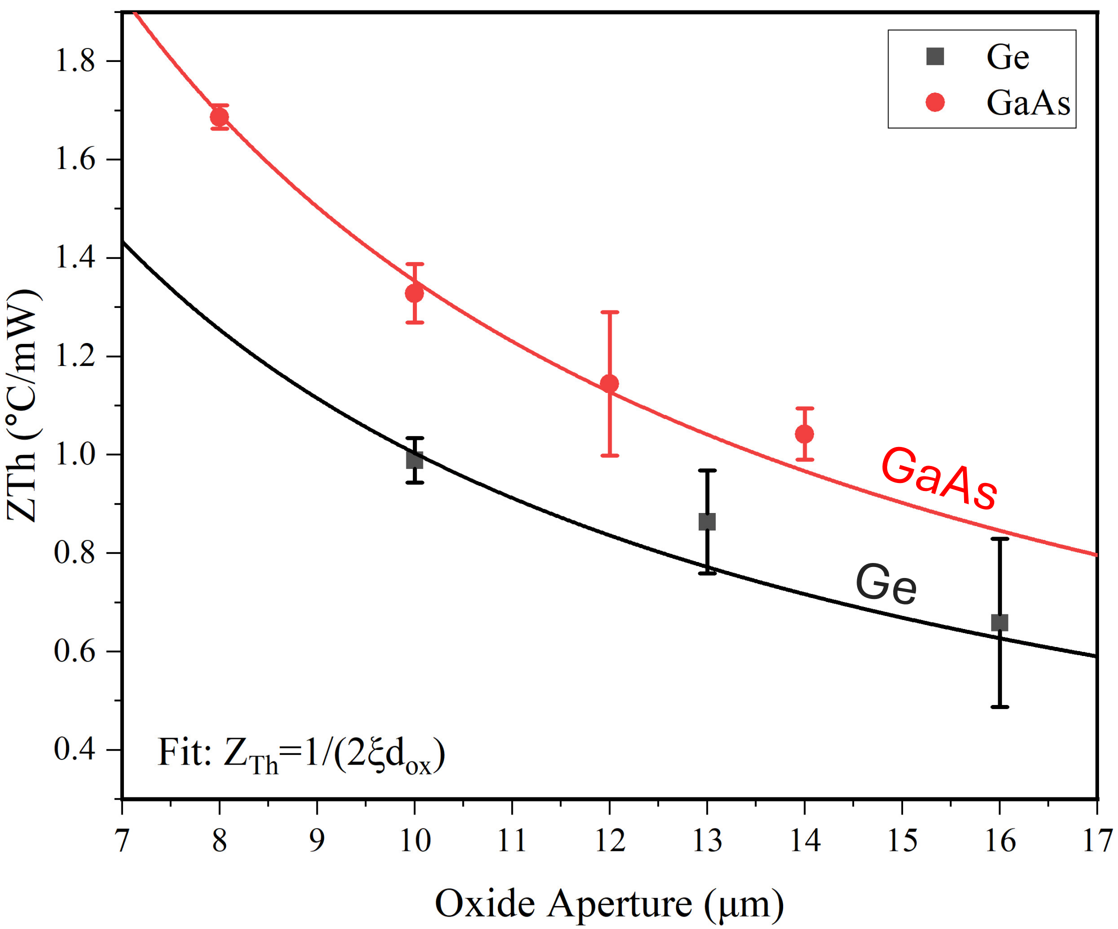
200 mm Wafer Development





VCSELs on Germanium (thermal performance vs GaAs)





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Cycle of 2-3 months

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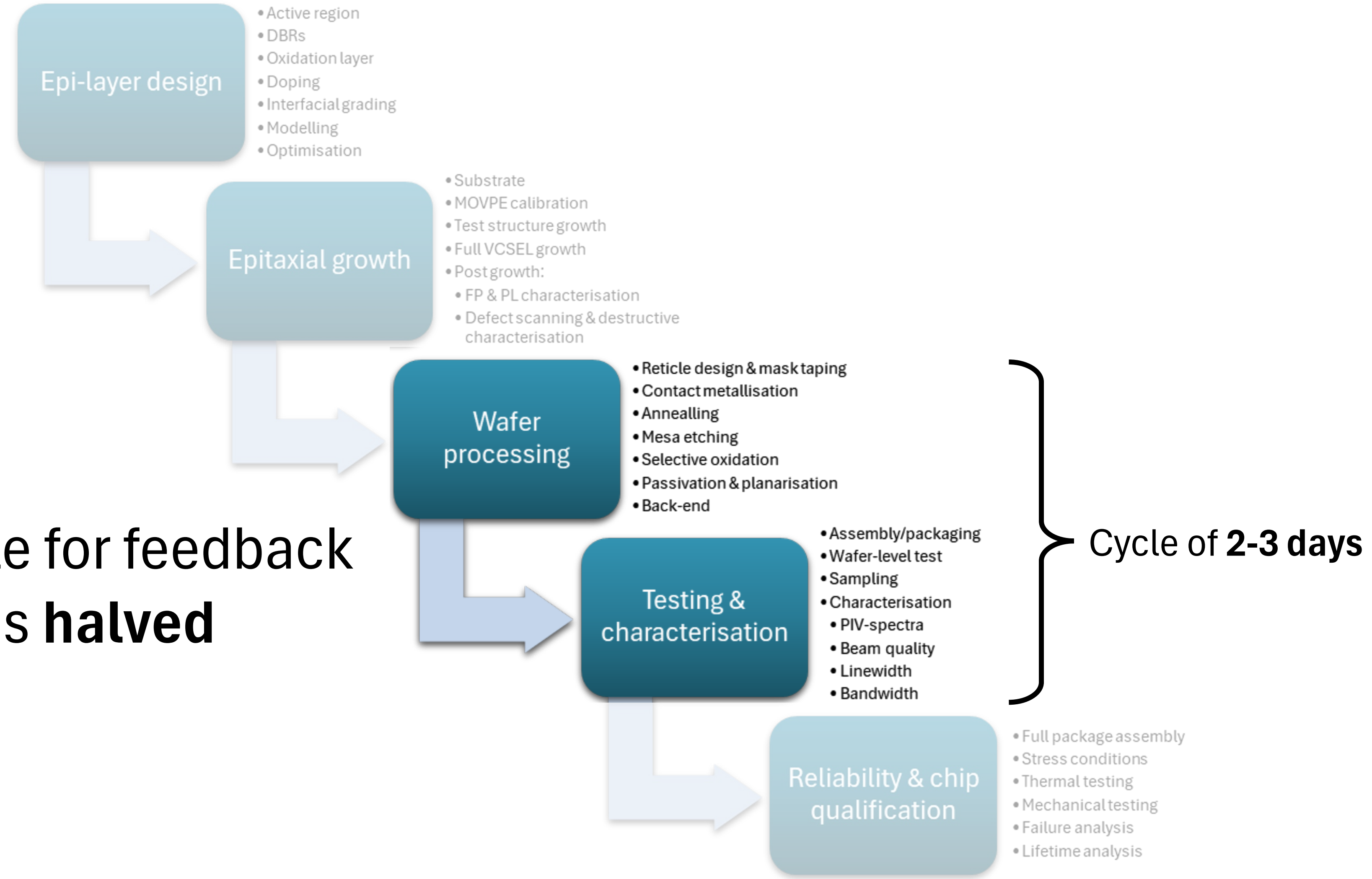

2 – 3 month cycle for feedback to epitaxy is **halved**

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Conclusion

Quick VCSELs (QuickSELs) which work for sensing/LiDAR, atomic clocks & magnetometers, and datacom applications

Total device processing time varies between 24 – 30 hours (versus 24 hours per mask layer)

Significantly reduces time required for feedback of VCSEL performance to epitaxy

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Acknowledgements

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- European Regional Development Fund through SMART Expertise Project ATLAS, under Grant 82371.
- UKRI Strength in Places Fund, under Project 107134.
- Innovate UK QFoundry project.

Supplementary Info

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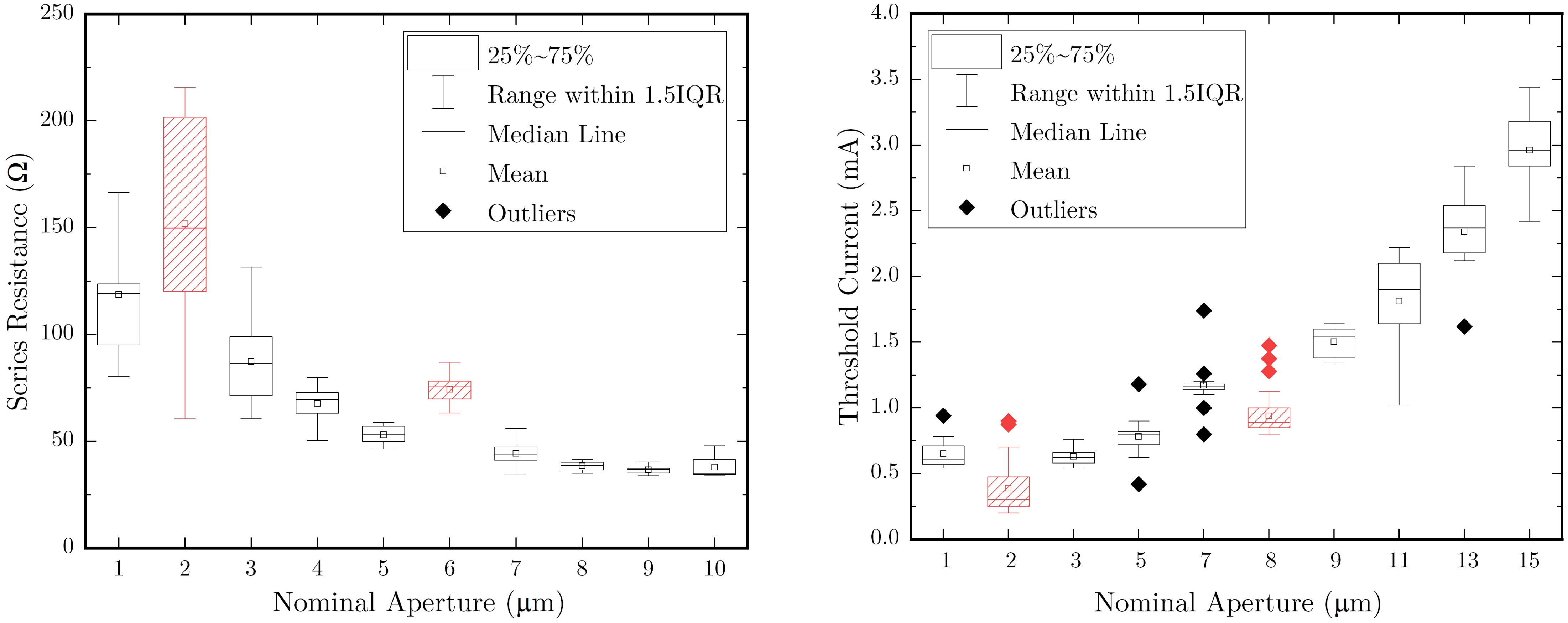
QuickSEL – Initial Qualification



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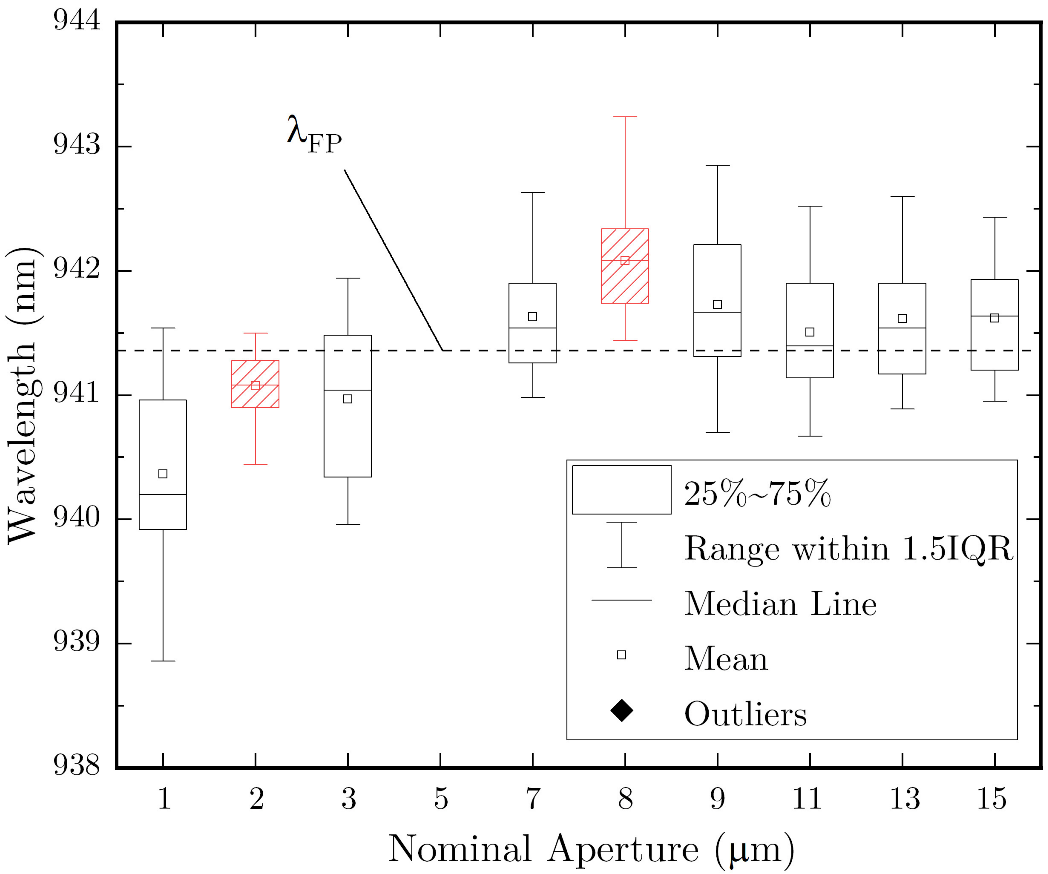

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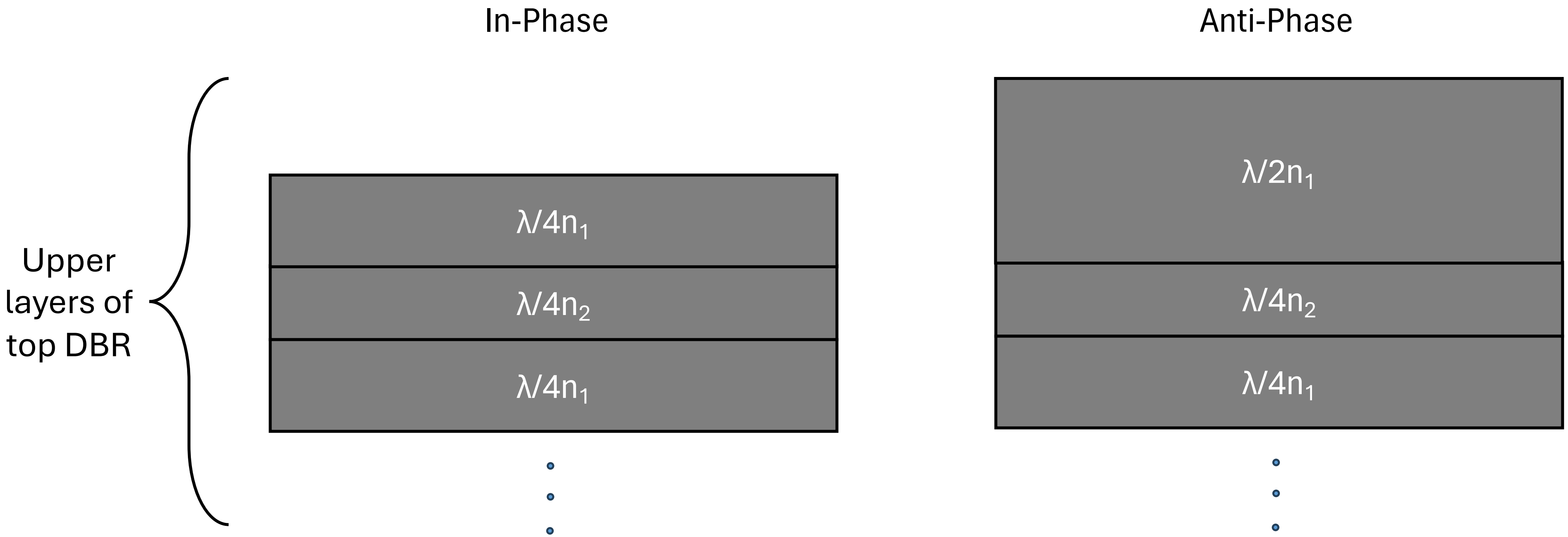
In-Phase vs Anti-Phase



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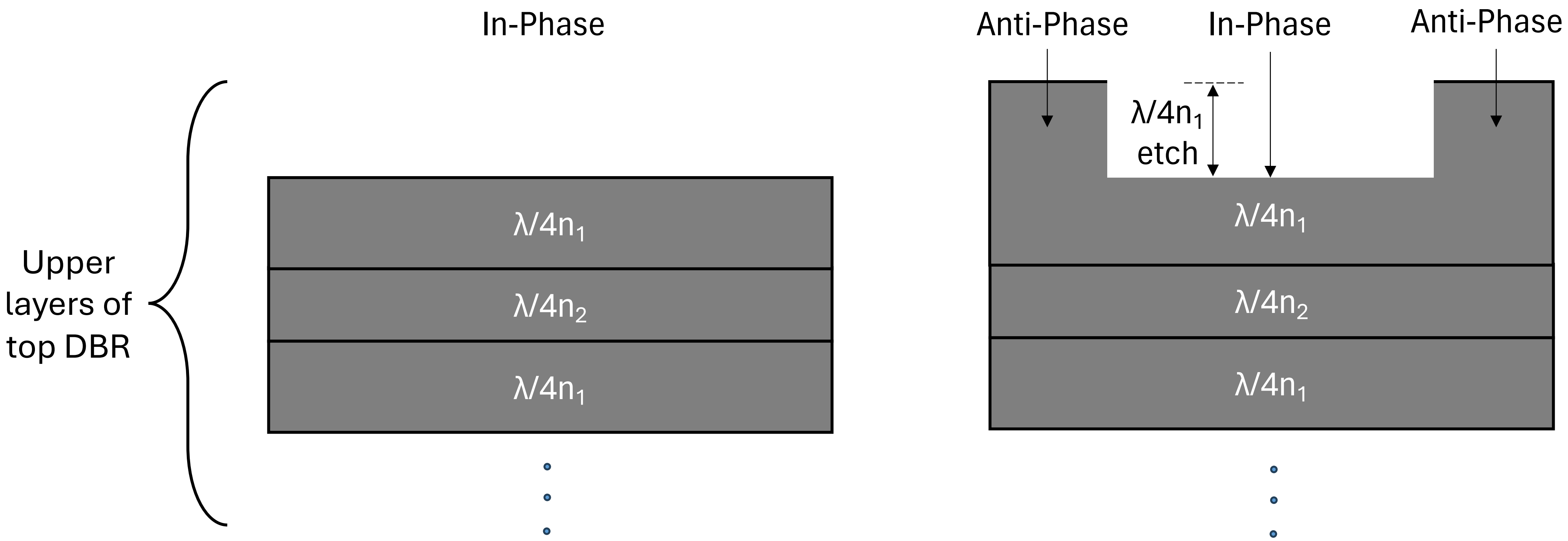

Advantageous for mode control

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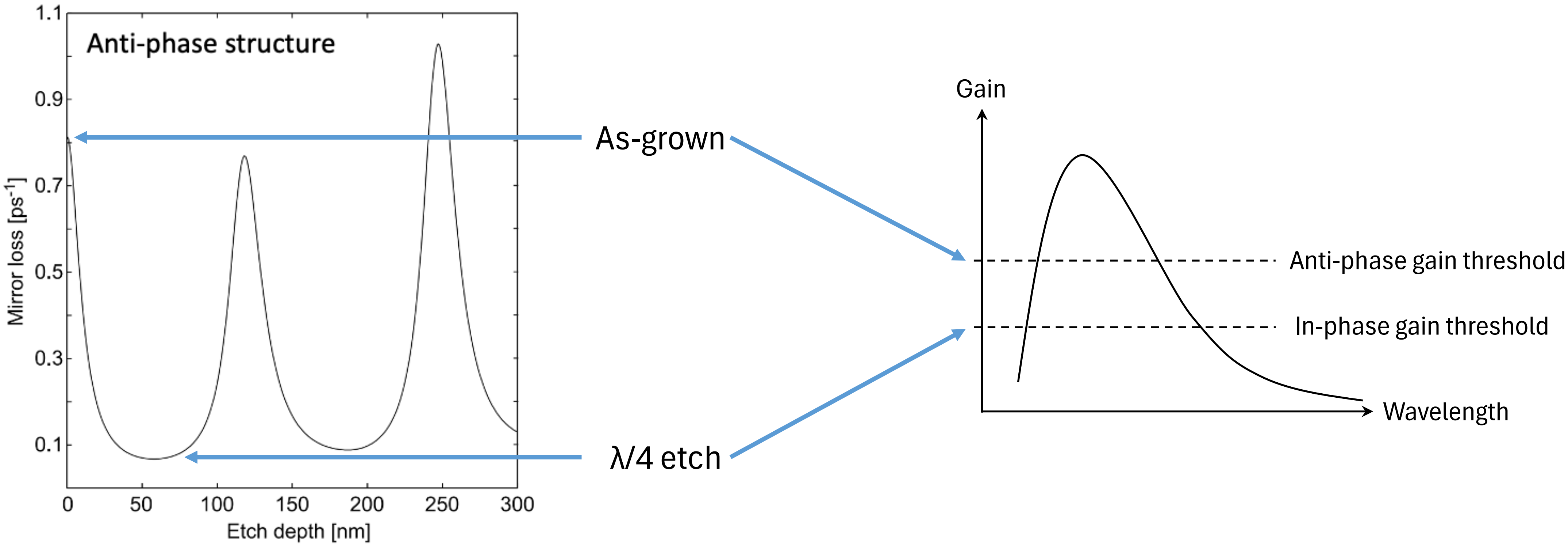
Phase Cap-Etch



From Haglund et al, IEEE PHOT. TECH. LET., 16, 2 (2004)