New workflows for resolving compound semiconductor defectivity issues using destructive and non-destructive electron microscopy techniques

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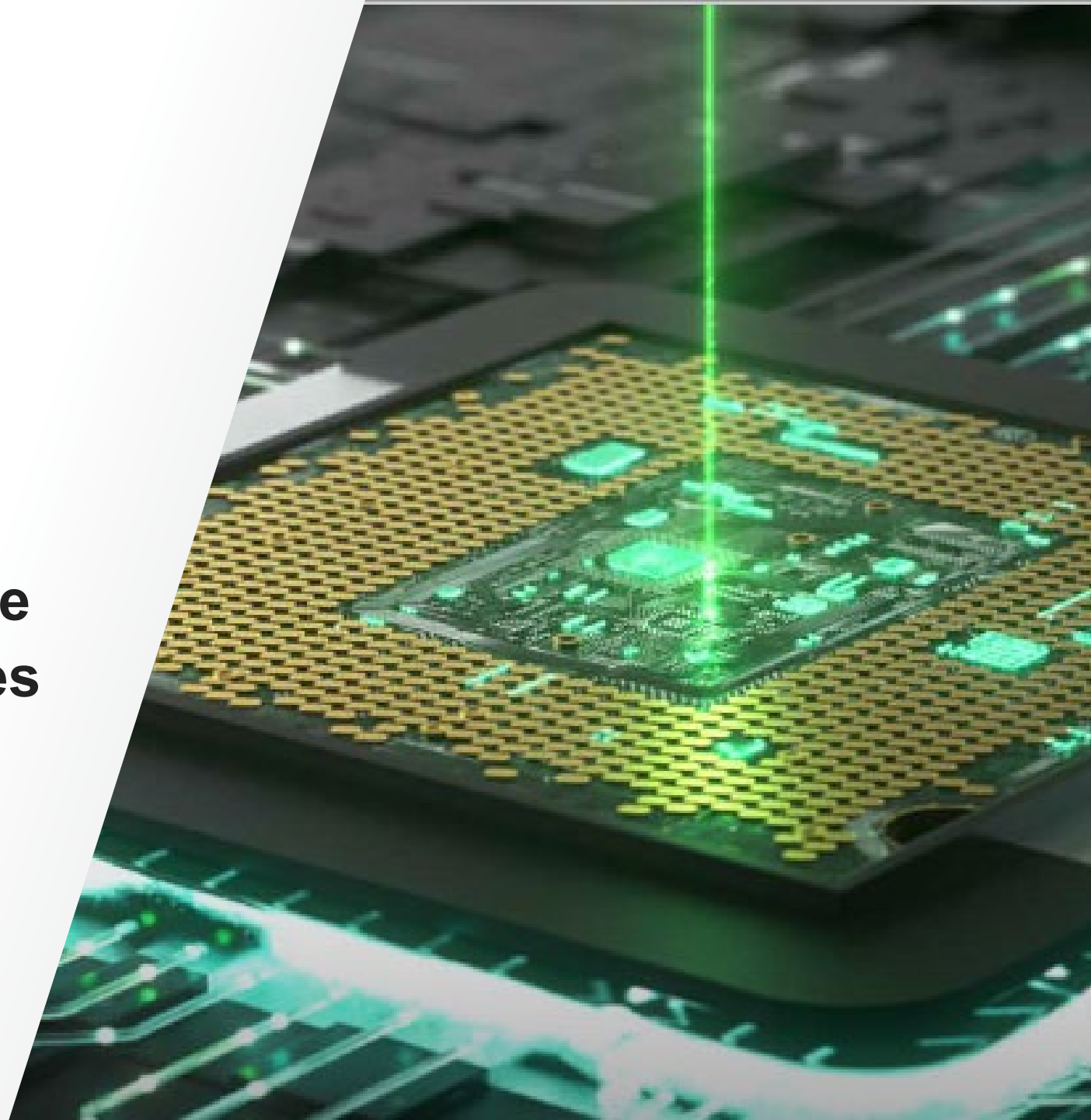
Regional Marketing Manager
April, 2023



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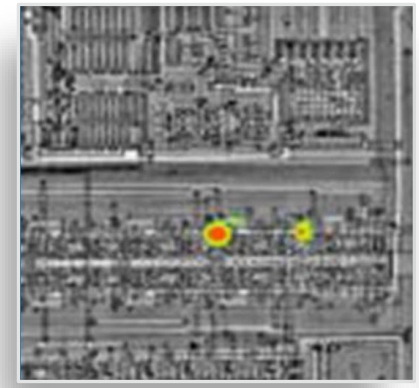
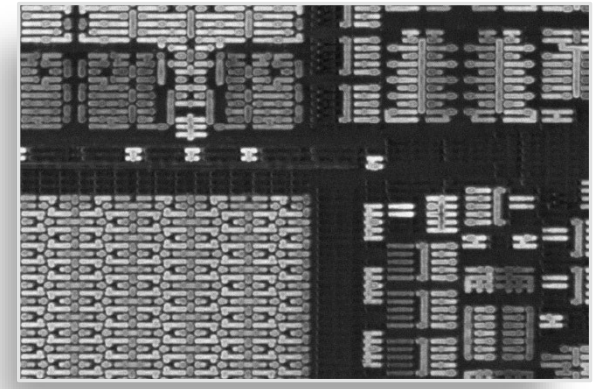
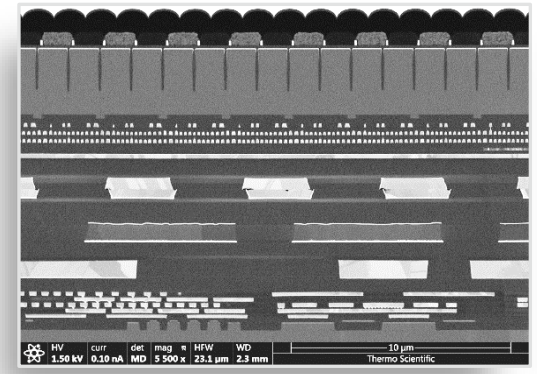
Existing failure analysis solutions

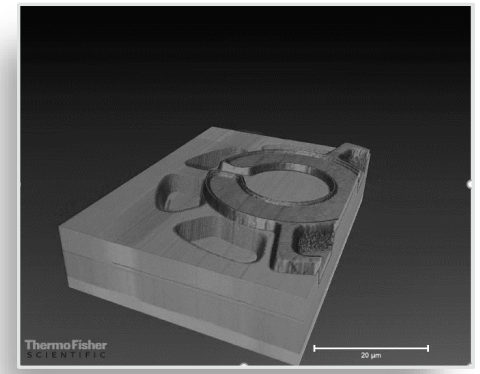
Logic & Memory



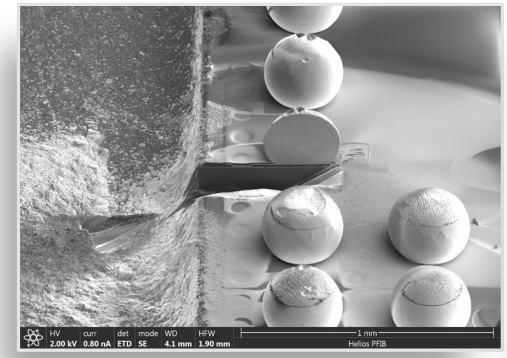


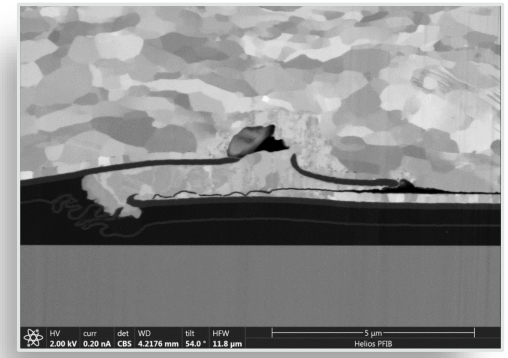
Optoelectronics & Display Devices



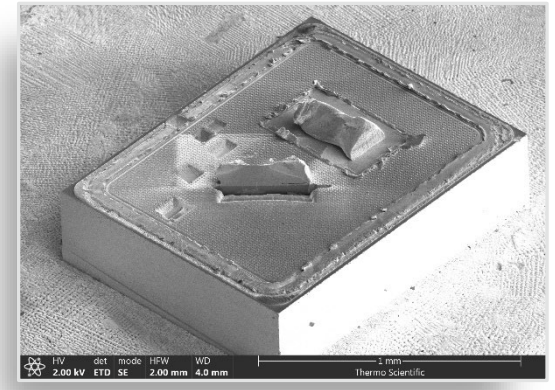


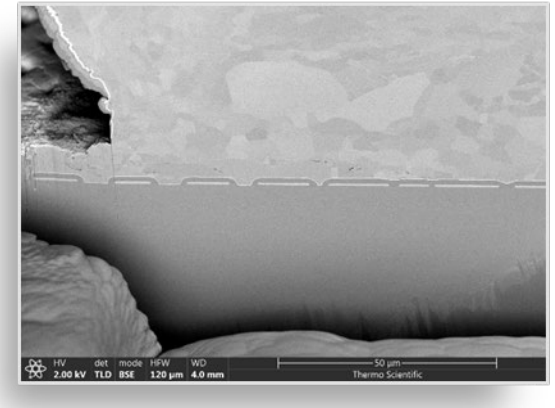
Device Packaging



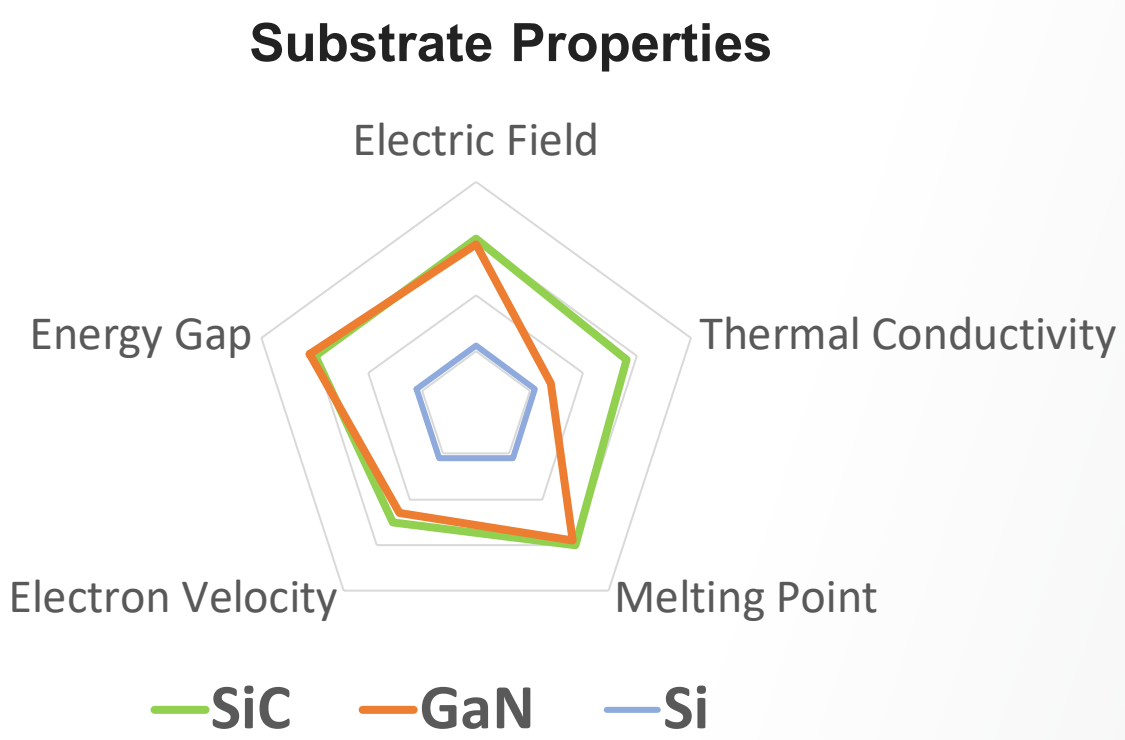


Power Devices & Compound Semiconductors





SiC/GaN - the perfect Power Device substrate choice?

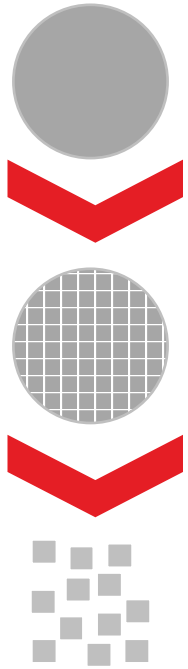


SiC advantages

- Higher voltage operation
- Higher temperature operation & endurance
- Higher frequency operation

… But SiC and GaN substrates have more defects and lower yields

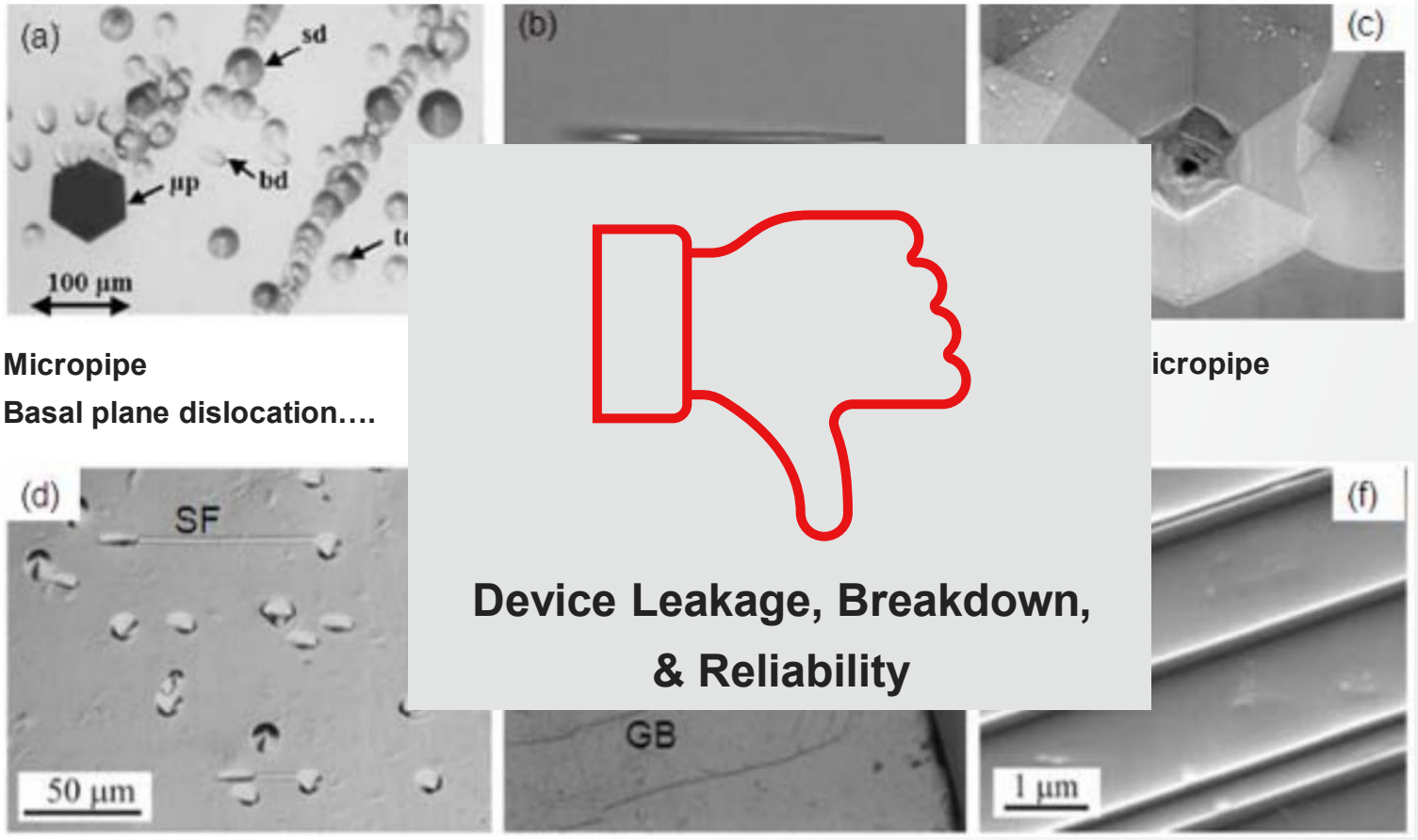
SiC & GaN substrates = high defectivity = more analysis demands



Sample Type	ROI	Solution Requirements
	Crystalline Defect	Process control & monitor
	Crystalline Defect + others	Crystalline Defect characterization
	Large Physical Defects	Fast turnaround FA localization + analysis

Wafer Level Inspection

Epitaxial growth causes large number of wafer crystalline defects



Micropipe

Basal plane dislocation….

icropipe

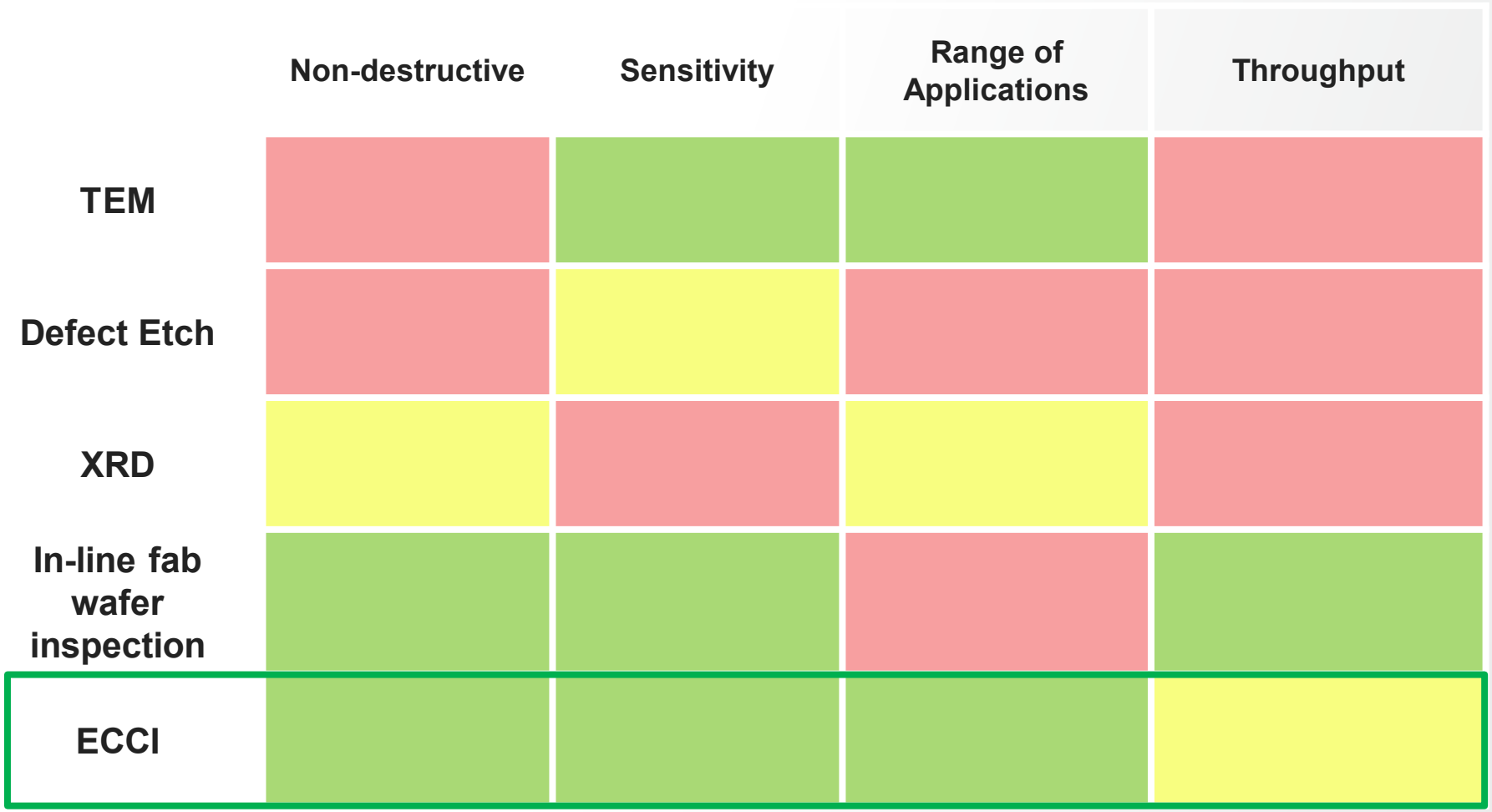
Device Leakage, Breakdown, & Reliability

Stacking fault

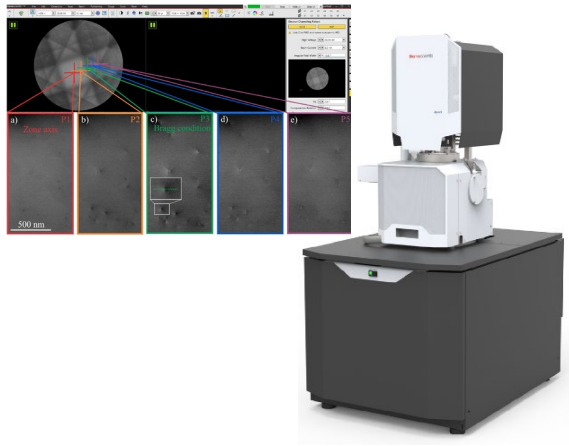
Grain boundary

Stacking fault

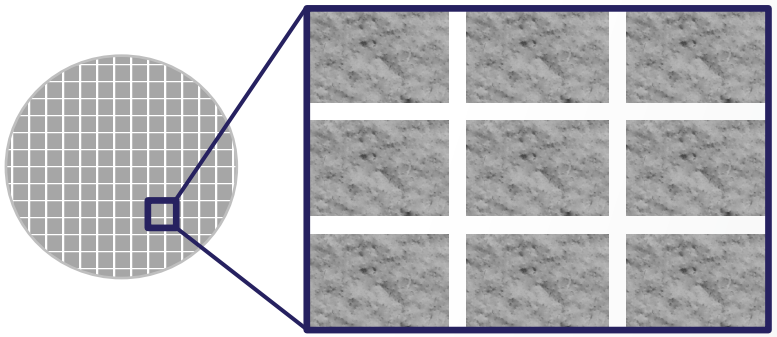
Wafer Defect Analysis - Available Solutions



Wafer Defect Analysis - ECCI



Apreo SEM
Wafer Navigation
Set ECCI Imaging conditions



Automated large area sample Imaging using MAPS

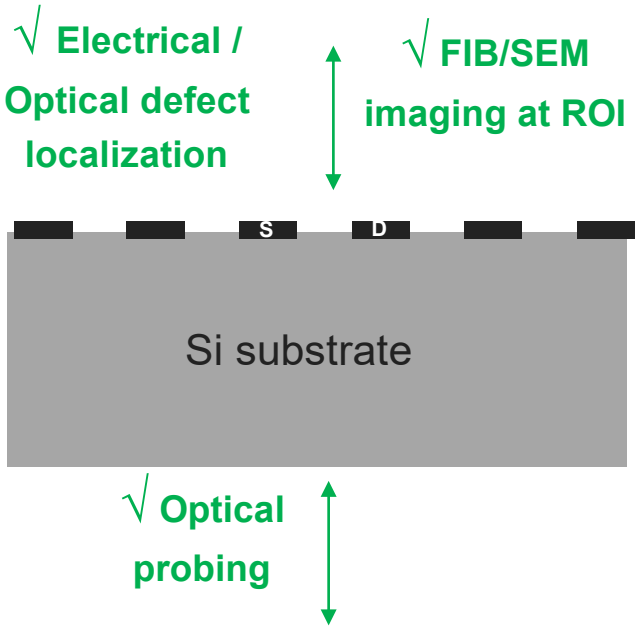
Final Output:
Operator Identifies crystalline defect density and classification

Apreo ECCI fully characterizes high defect density wafers

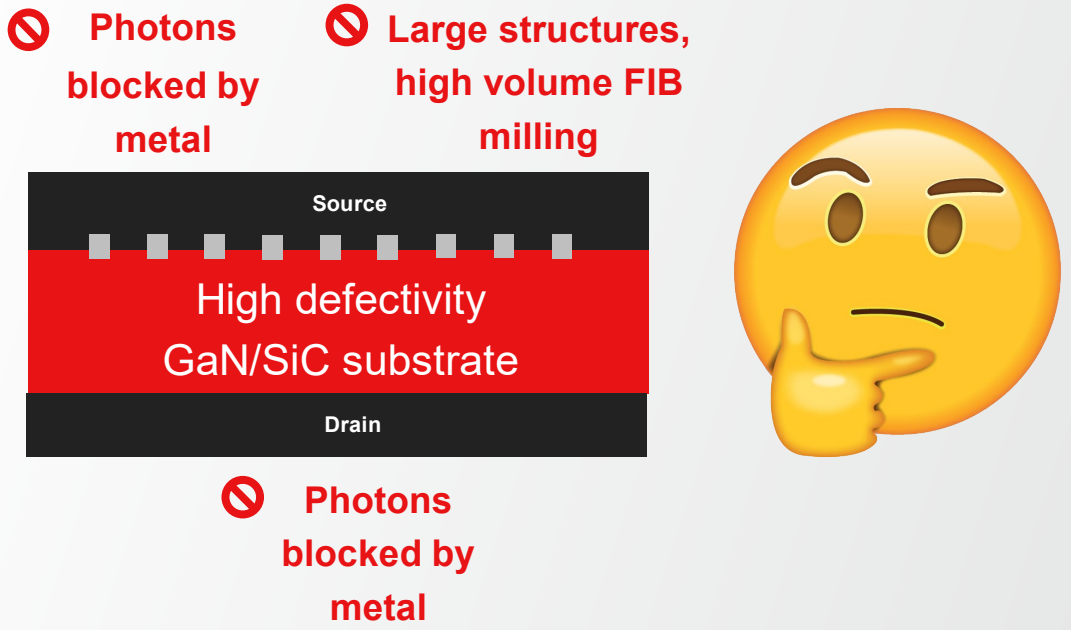
Failure Analysis
EFA to PFA

Power Devices present unique FA challenges

Logic & Memory FA

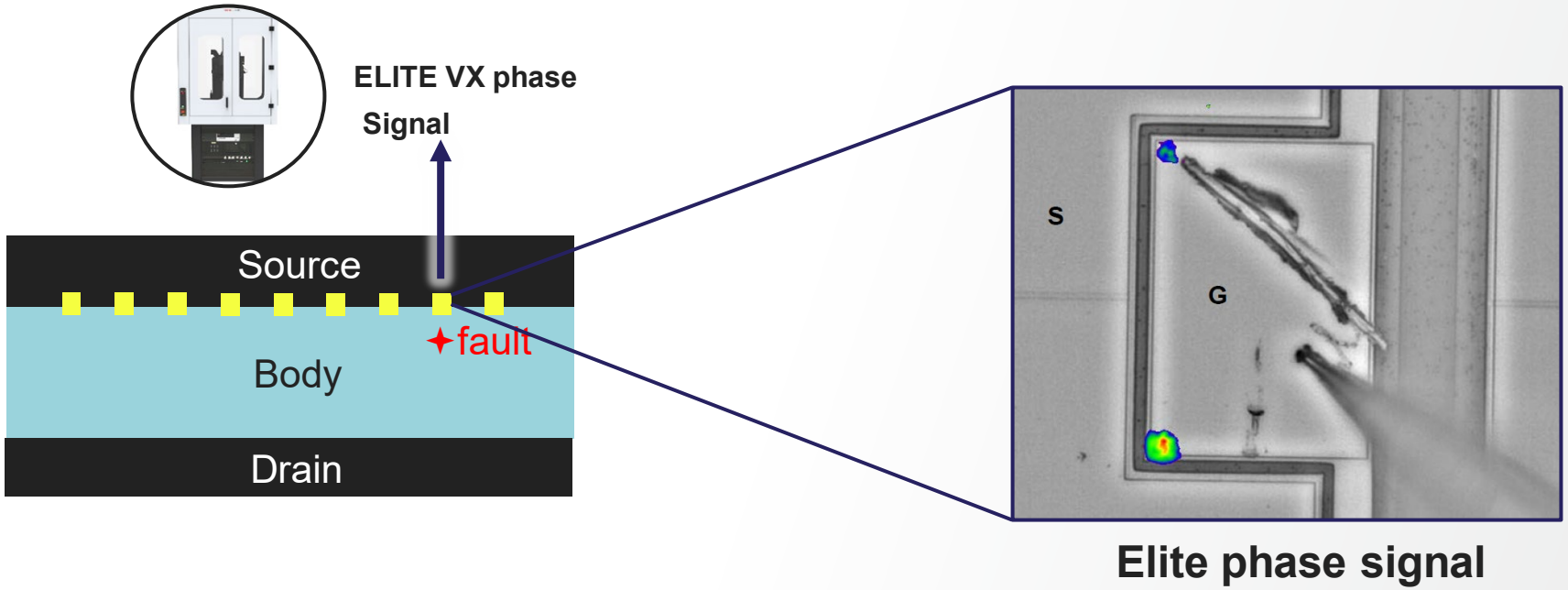


Power Device FA



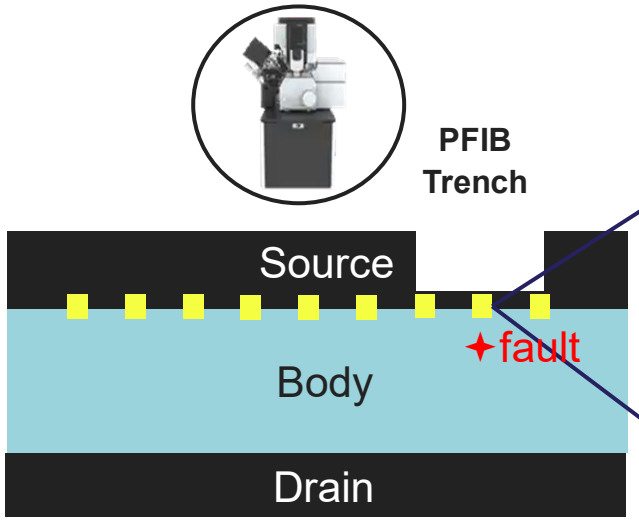
EFA to PFA Workflow for Power Devices

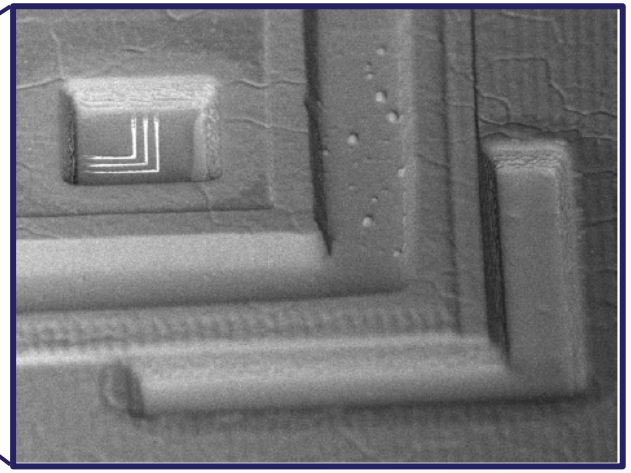
Coarse Fault Localization



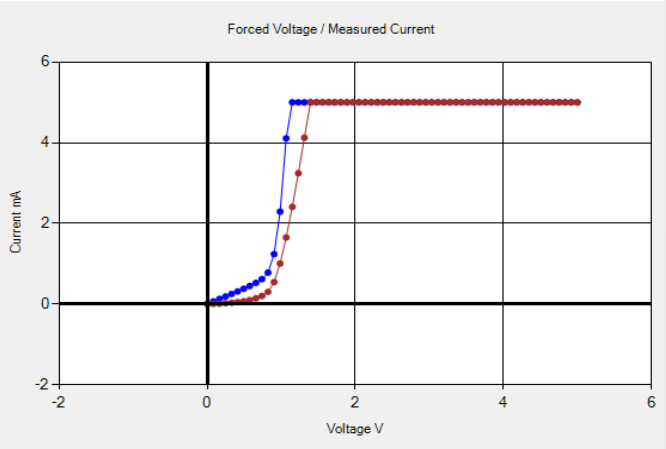
Coarse Fault Localization → Sample Preparation → Fine Fault Localization → Characterization and Analysis

Sample Preparation (for fine localization)





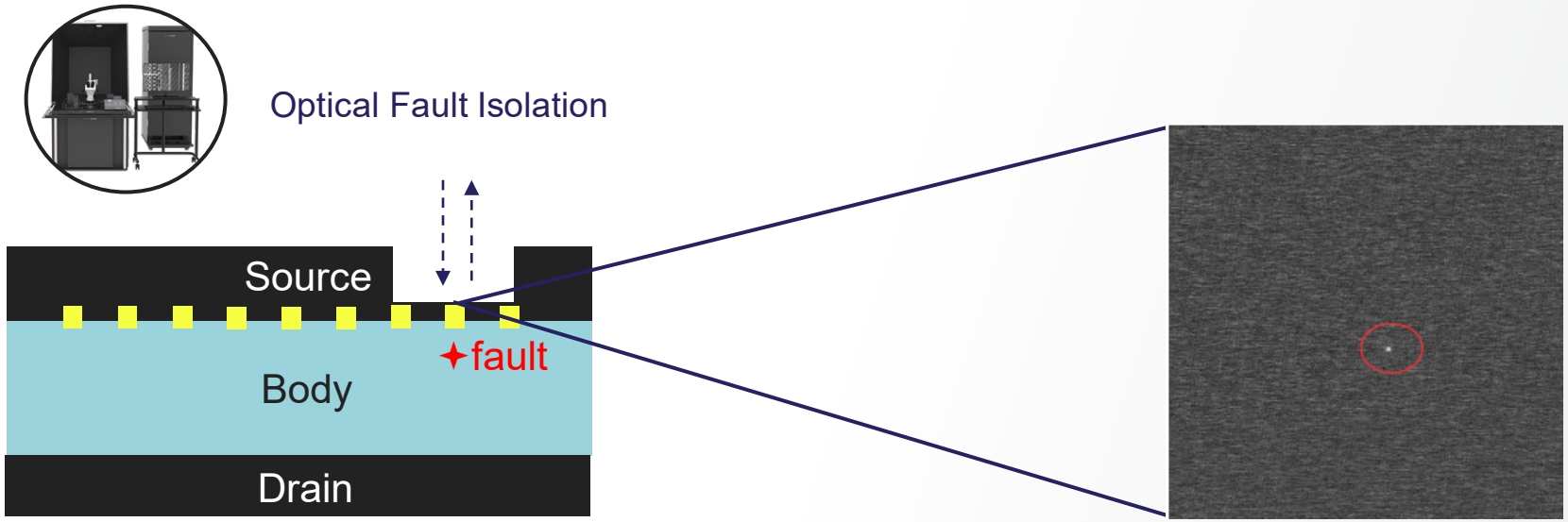
Site-Specific Delayering



Device still functions after PFIB delayering

Coarse Fault Localization → Sample Preparation → Fine Fault Localization → Characterization and Analysis

Fine Fault Localization



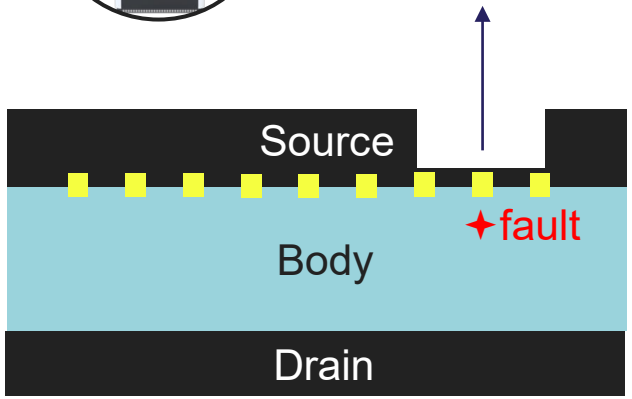
HV OBIRCH "re-localization"

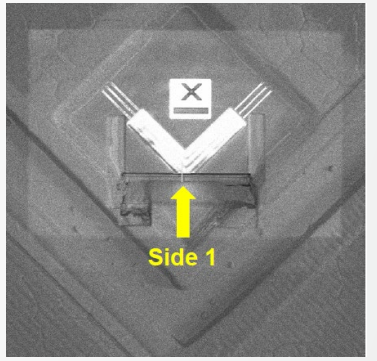
Defect is localized to the nm scale– can now go to PFA

Coarse Fault Localization → **Sample Preparation** → **Fine Fault Localization** → **Characterization and Analysis**

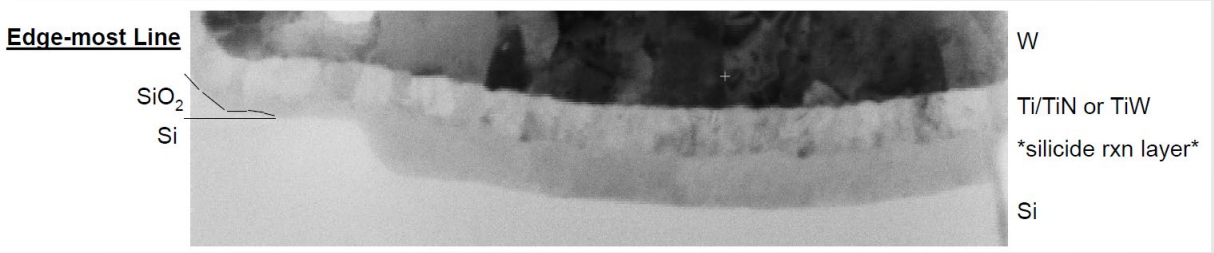
FA/Characterization & Analysis

Cross Sectioning or
TEM prep + STEM





Cross Sectioning



TEM prep + STEM

Coarse Fault Localization → **Sample Preparation** → **Fine Fault Localization** → **Characterization and Analysis**

Compound semiconductor FA workflows continue to evolve

Thermal Fault Isolation

Delayering

HV OBIRCH

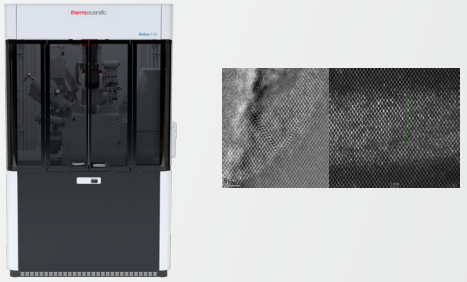
Cross Sectioning / (S)TEM Analysis

Coarse Fault Localization → Sample Preparation → Fine Fault Localization → Characterization and Analysis

ELITE VX

Helios 5 PFIB

Meridian S



Helios 5 CX & Talos F200E

References

Application Notes:

- Crystalline Defect Characterization in Compound Semiconductors

- Wide Bandgap Power Devices Failure Analysis

Blog:

- Power Semiconductor Devices - Electrical Failure Analysis - Blog

Webinar:

- Understanding crystalline defects in compound semiconductors using electron channeling contrast imaging

Thank You