



# Characterization of thin films and critical dimensions in SiC and GaN process flows

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# Presentation Outline

- Introduction to Onto Innovation
- Markets and Technologies Served
- Power Market Landscape
- SiC and GaN Device Fabrication Challenges
  - Epi Layer Control and Characterization
  - OCD and Thin Film Metrology
  - Metallization Metrology
- Onto Innovation Product Portfolio
- Discussion

Experience the  
Power of  
**Connected  
Thinking.**

## **Connected Solutions**

Building a smarter fab

## **Connected Analytics**

Yield management software that spans the  
fab ecosystem

## **Connected Outcomes**

The path to zero defects

# Onto Innovation Snapshot

High tech capital equipment company specializing in optical process solutions for semiconductor and related markets



**1,580** EMPLOYEES



**9,000** ACTIVE METROLOGY & INSPECTION TOOLS INSTALLED



**75 Fabs** FAB-WIDE YIELD/DEFECT SOFTWARE INSTALLED



**>400** PATENTS ISSUED FOR METROLOGY, INSPECTION, LITHOGRAPHY & SOFTWARE



**> \$1Bn** REVENUE FY 2022



# Portfolio of Synergistic Technologies Across Multiple Markets

Foundation for new products and solutions to customers future challenges

## SILICON WAFER MANUFACTURING

Raw material for chips

## DEVICE FABRICATION

Advanced Nodes

## DEVICE FABRICATION

Specialty Segments

## ADVANCED PACKAGING

Separating wafers to individual chips, connecting multiple chips into a single package



### Physical Defect Control

Cracks | Pits | Foreign material

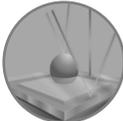


### 3D Metrology

Nanometer measurements | Feature shape/slope/angles | Film thickness



### Macro Defect Inspection



### 3D Metrology

Bump connections | Thru-silicon via's



### Material Analysis

Silicon purity | Unwanted elements

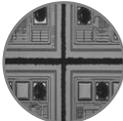


### Macro Defect Inspection

Foreign material | Scratches | Residue

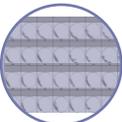


### CD Overlay

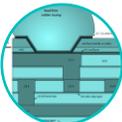


### Macro Defect Inspection

Placement locations



### Yield Analysis Software



### Metal Film Metrology



### Lithography

Printing connecting circuits



### Yield Analysis Software



### Yield Analysis Software

Experience the Power of

Connected Thinking

# Power Device Market Landscape



**Data Center P/S**  
(Si / SiC)



**Fast Charge**  
(GaN)



**Electric Vehicle**  
(Si / SiC / GaN)



**Portable Technologies**  
(GaN / Si BCD)



**Industrial Robotics**  
(Si / Si BCD)



**Distributed Power &  
Power Management**  
(Si BCD)



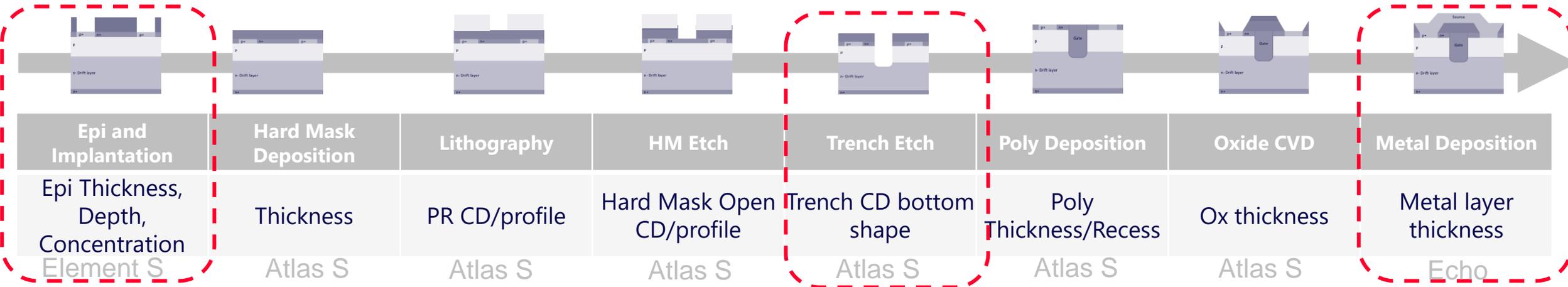
**Solar Inverter**  
(Si / SiC / GaN)

## Power Device Market Enabled by New Device Technology Trends

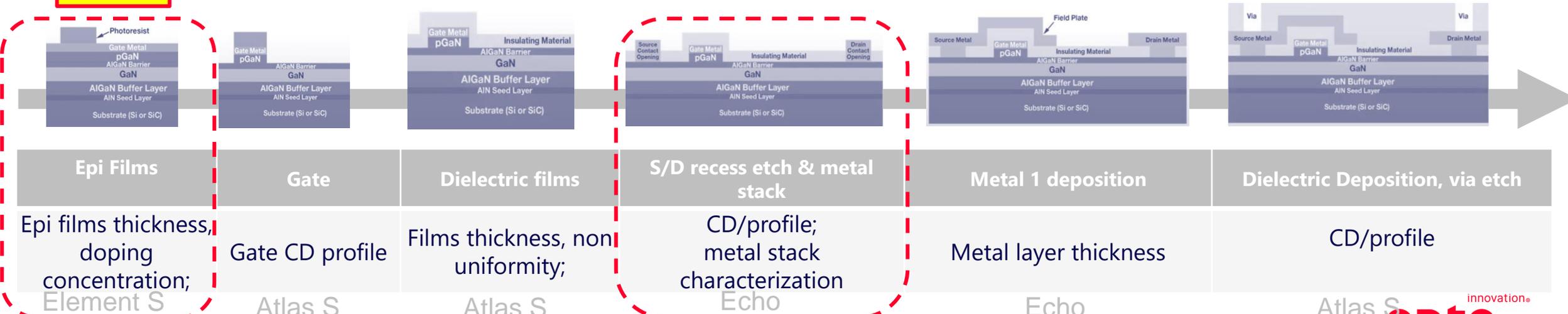
- **Wafer Size Migration** (Si, SiC, GaN)
- **Compound Semi (SiC, GaN)** enabling new power application technologies
- **Epi Layer Composition & Quality**
- **Dopant Profile Control**
- **High Aspect Ratio Trenches**  
(Si/SiC SJM, BCD Isolation)
- **Front/Back Metallization Schemes**
- ....and much more...

# SiC Mosfet and GaN HEMT Process Control Requirements

## SiC

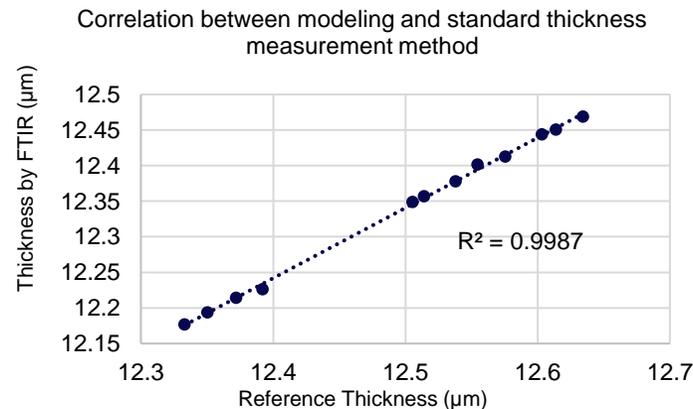
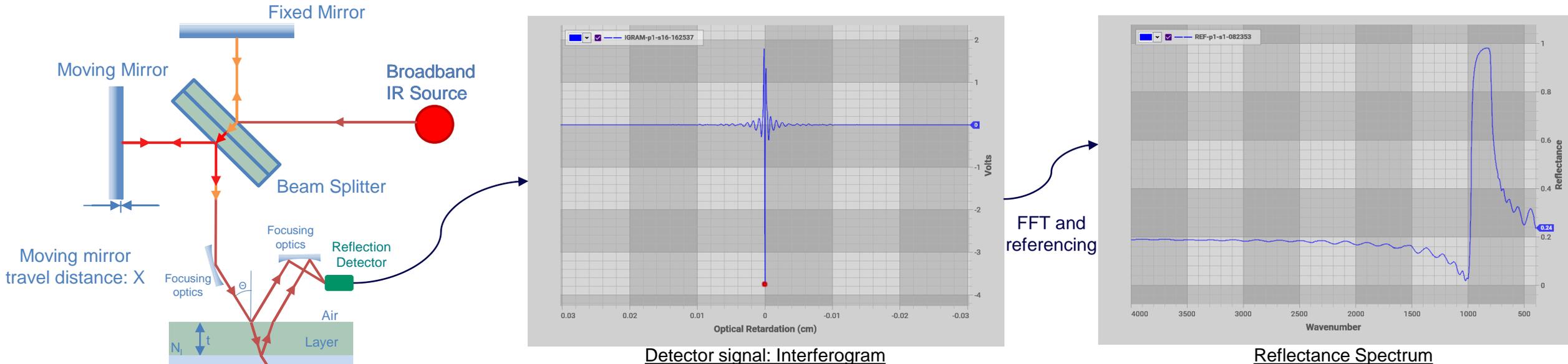


## GaN



# SiC and GaN Epitaxial Layer Characterization using FTIR

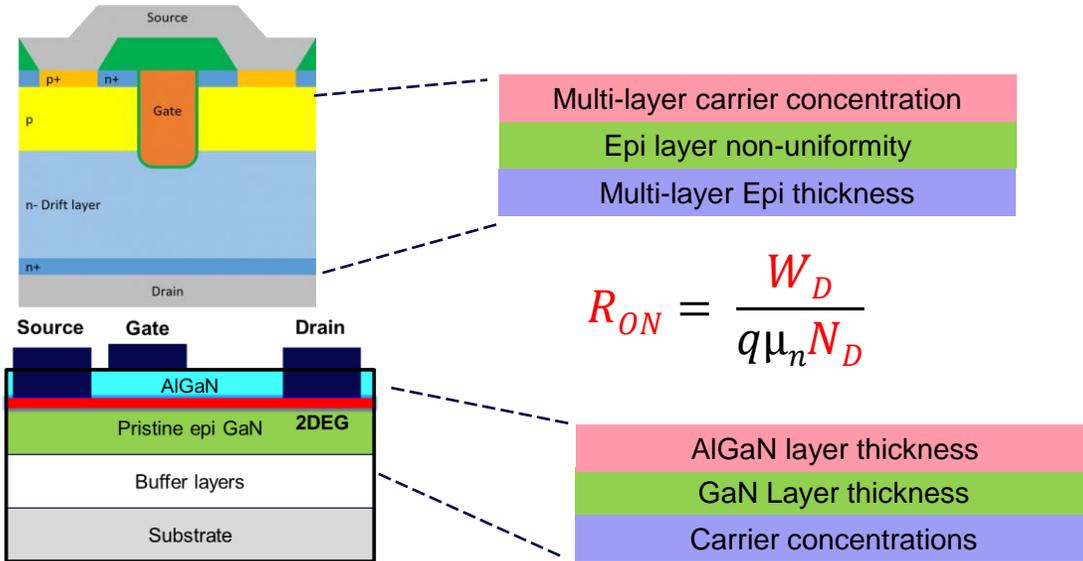
Wide Adoption in Specialty Markets (SiC, GaN, GaAs, etc.)



- Fast, non-contact, non-destructive and accurate measurements of epi layer film thickness, non-uniformity and carrier concentration
- Collect the interferogram using a Michelson interferometer, then FFT to get reflectance spectrum  $R = I_R/I_0$
- Match theoretical and measured reflectance spectra
- Excellent correlation to reference thickness measurements

# Epitaxial Layer Metrology

## SiC and GaN Power Device Epi Process Challenges



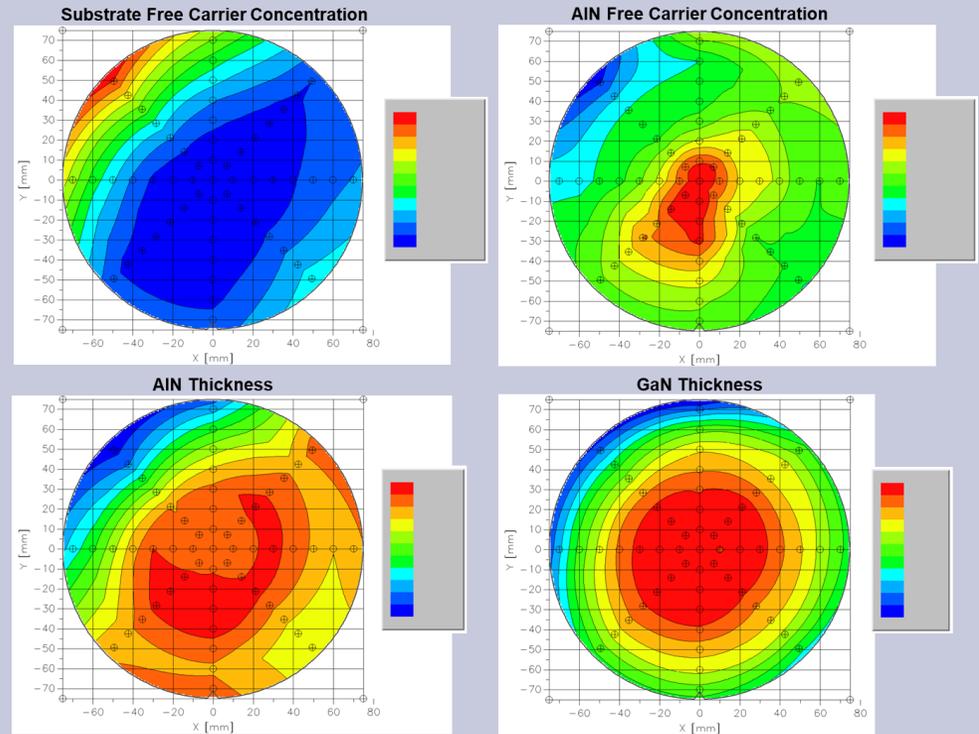
$$R_{ON} = \frac{W_D}{q\mu_n N_D}$$

### Epitaxial Layer Metrology Requirements

- Epi layer thickness needs to increase for higher  $V_{bd}$
- $R_{on}$  depends on drift layer thickness as well as dopant concentration
- Multi-layer thickness control for epi layers
- Carrier concentration in epi layers for GaN

FTIR technology provides unique solution to multi-layer epitaxial layer metrology

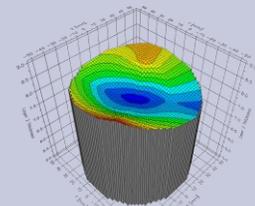
## GaN: Epi Layer Thickness; Dopant Concentration



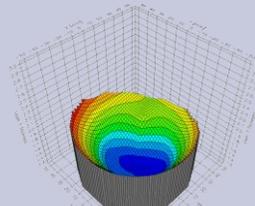
GaN:  
Epi layer thickness and AlN/SiC carrier concentration

# Epitaxial Layer Metrology

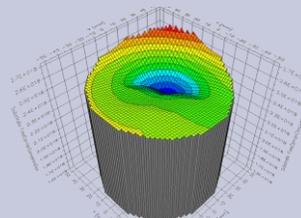
SiC: Epi Layer Thickness; Dopant Concentration



Layer 2 Thickness

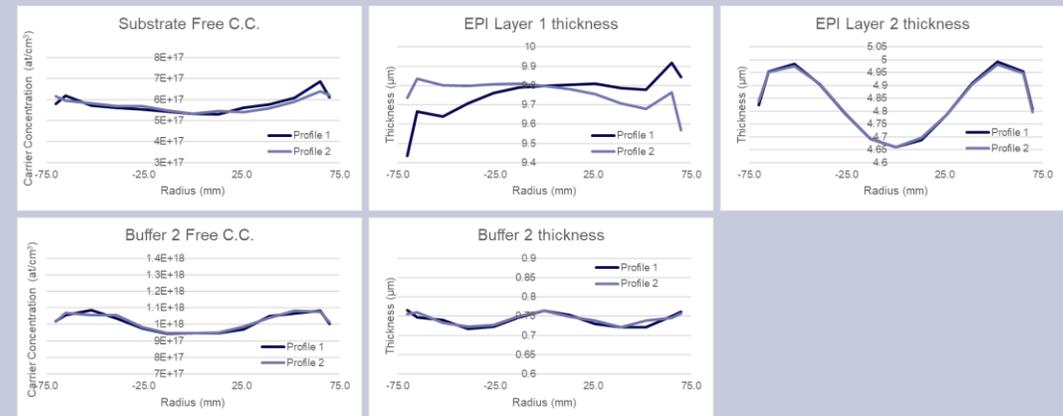
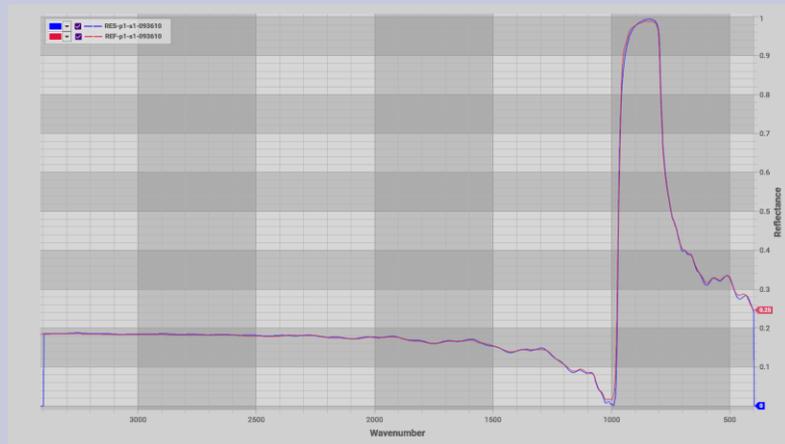


Layer 1 Thickness



Substrate Carrier Conc.

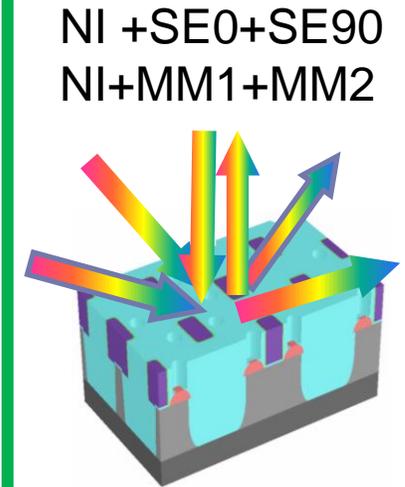
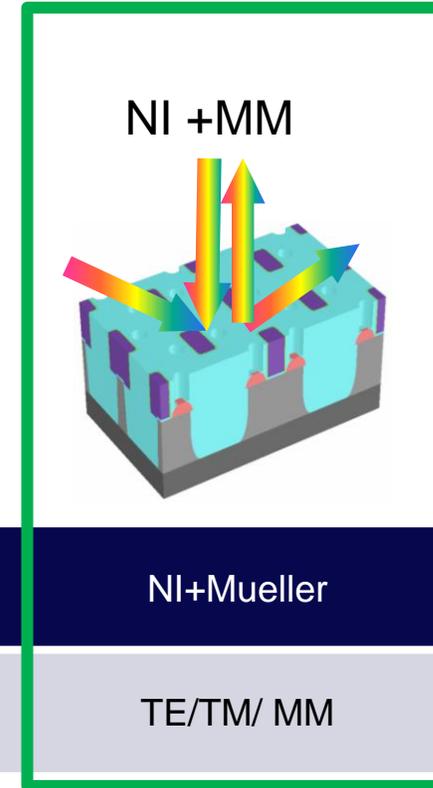
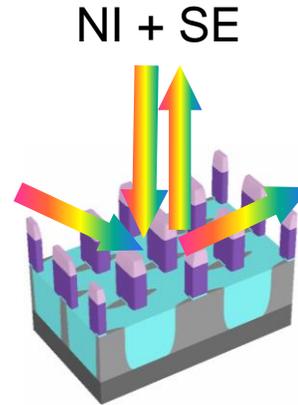
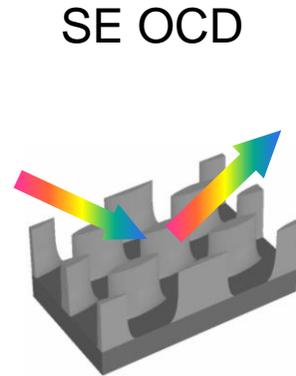
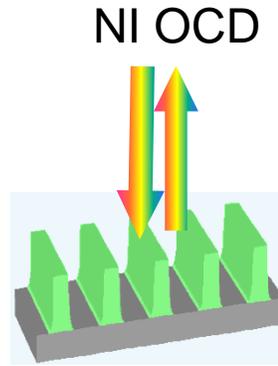
Parameter		Wafer Average	Wafer Stdev
Substrate	Free C.C. (at.cm <sup>-3</sup> )	5.8e17	3.75e16
EPI layer 1	Thickness (μm)	9.751	0.098
Buffer 2	Thickness (μm)	0.741	0.015
	Free C.C. (at.cm <sup>-3</sup> )	1.02e18	4.96e16
EPI layer 2	Thickness (μm)	4.849	0.108



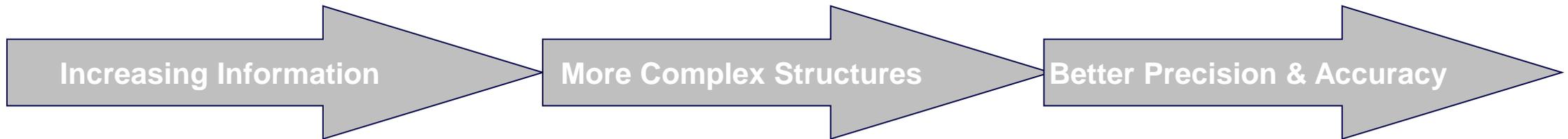
FTIR modeling can perform accurate measurements on complex SiC structure with repetitions of buffer & drift layers

# Thin Films and OCD on the Same Platform

Advance Node Metrology now being used for Specialty Market

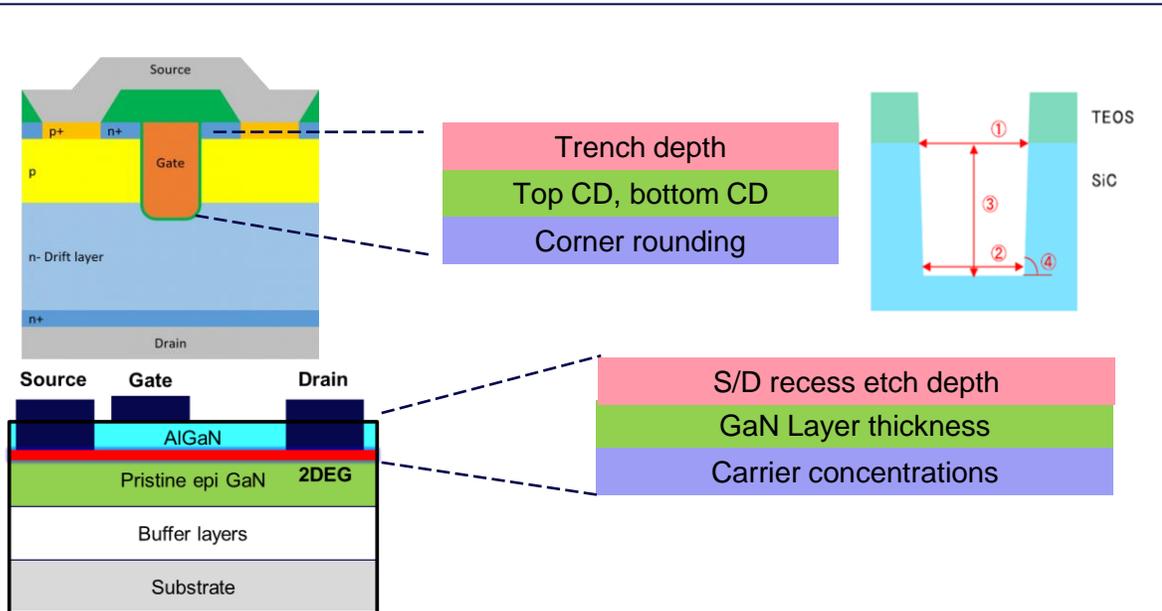


	NI OCD	SE (RCE)	NI+SE	NI+Mueller	NI+SE0+SE90 NI+MM1+MM2
Data	TE/TM	N, S, C	TE/TM/N, S, C	TE/TM/ MM	TE/TM, SE or MM for multi-azimuths



# Optical Critical Dimensions, and Thin Films Metrology

## SiC and GaN Power Device Critical Dimensions

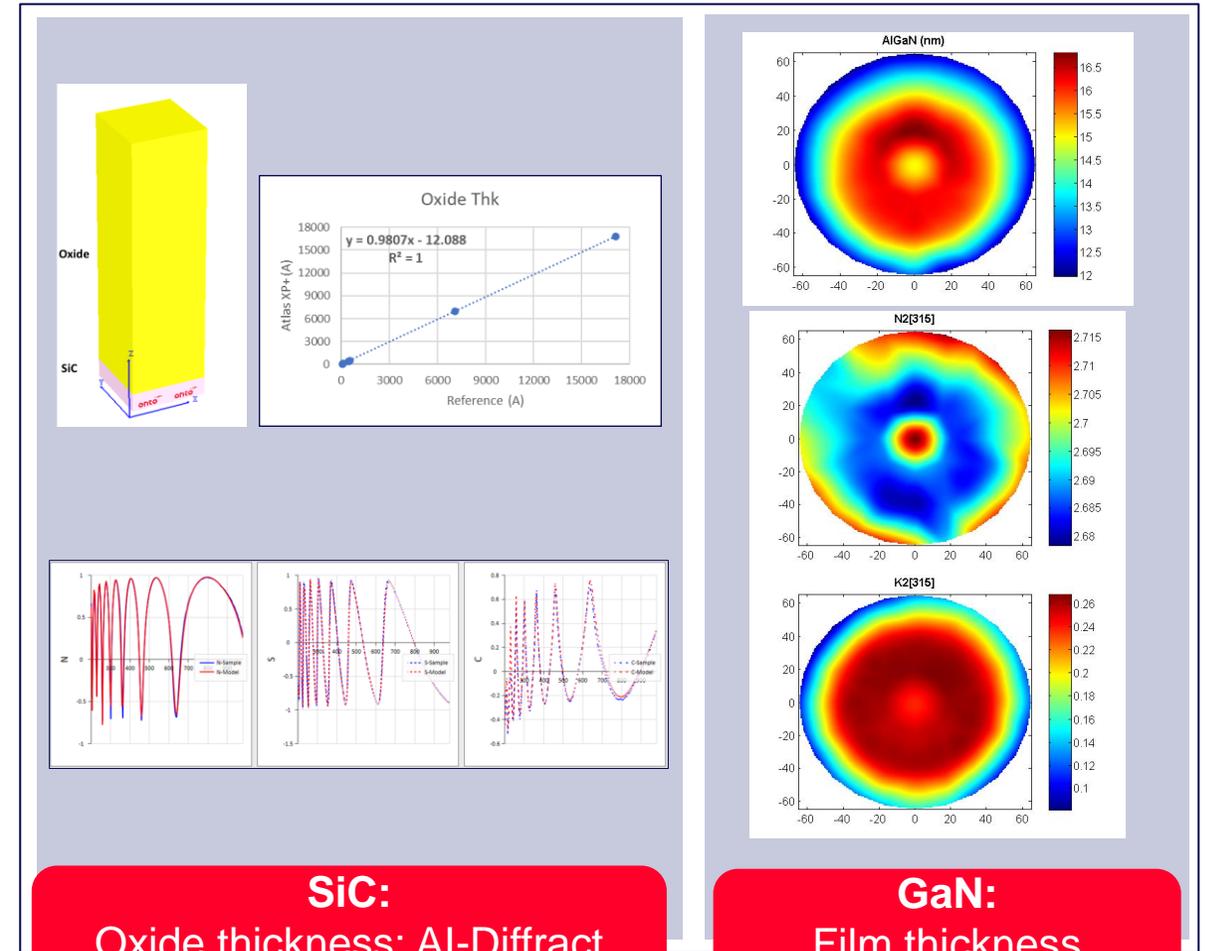


### OCD Requirements

- **Must control depth, top CD and bottom CD** to accurately extend inversion layer for free carrier flow for all devices across the wafer
- **Corner rounding** is needed to hold off high electric field density
- **S/D contact recess etch depth** critical to stop at the 2DEG
- **Film thickness** and uniformity controls breakdown voltage

Optical CD measurements enable uniform trench profiles and etch CDs across the wafer

## Thin film characterization

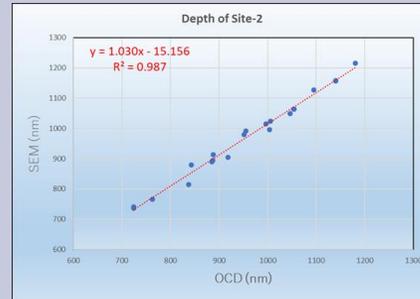
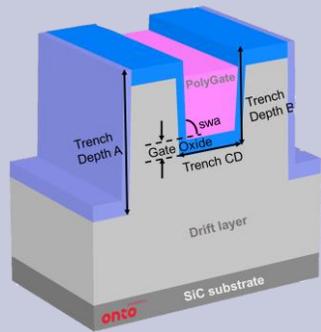


**SiC:**  
Oxide thickness; Al-Diffract Model Fit; Correlation to SEM

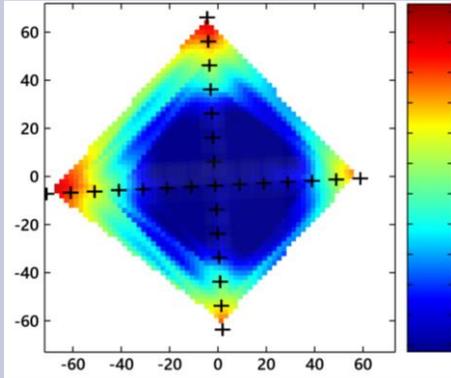
**GaN:**  
Film thickness n/k measurements

# Optical Critical Dimensions, and Thin Films Metrology

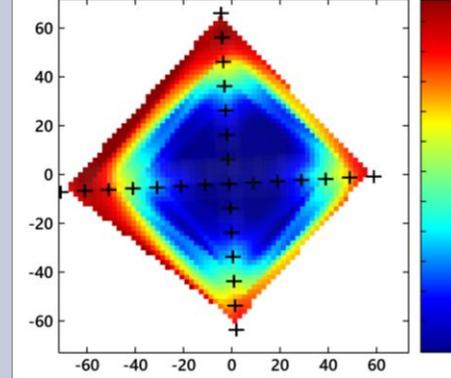
## Dual-trench depth profiles



Trench A Depth

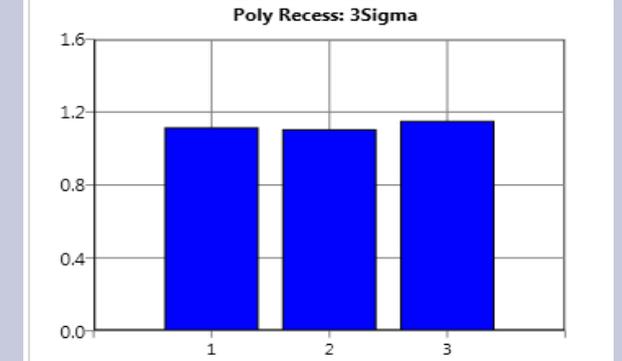
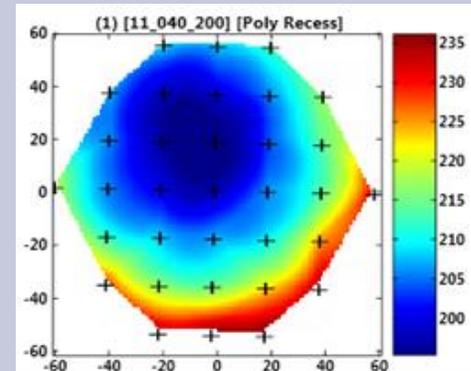
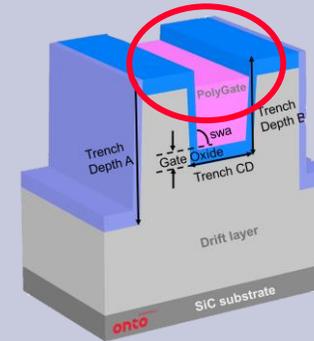


Trench B Depth



Double trench depths mapped  
Correlated to SEM data

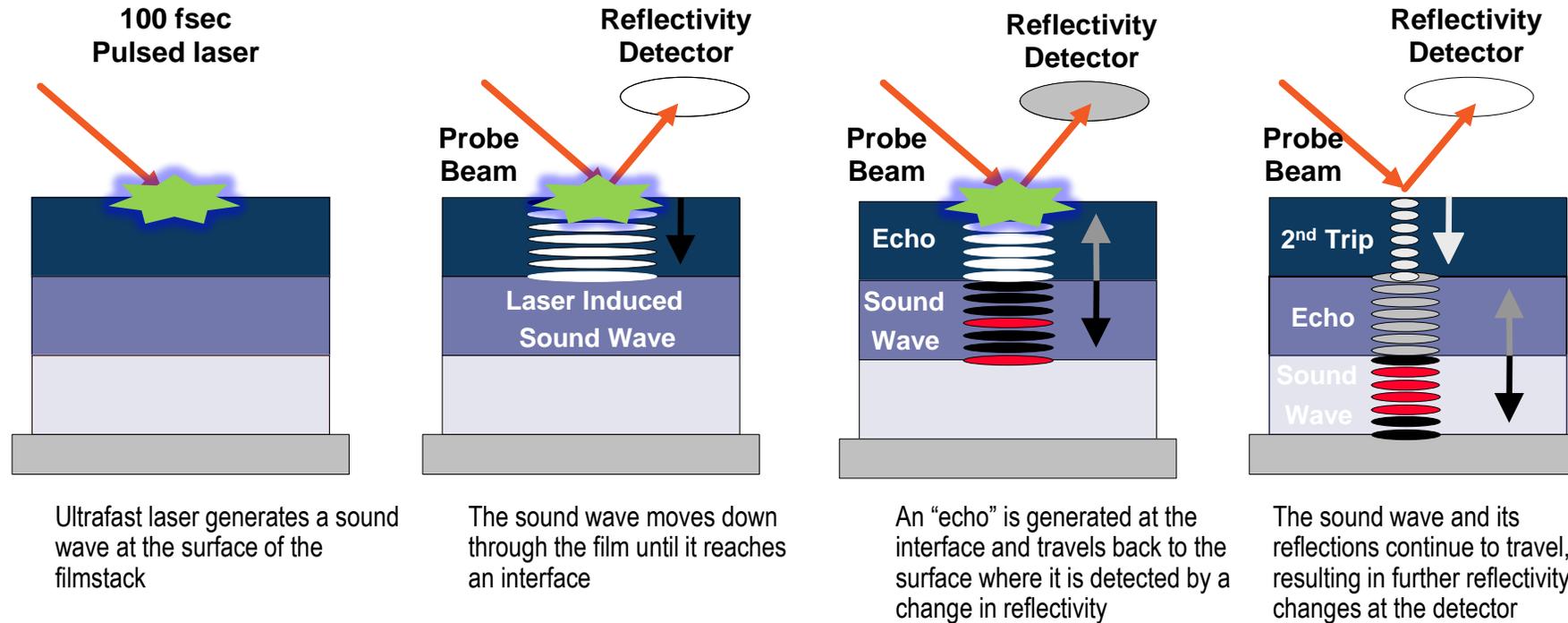
## SiC: Poly recess etch and trench depth mapping



Poly recess etch mapped – accurate recess important  
for next step (dielectric dep), which controls  $V_{SG}$

# PULSE Technology for Metallization Metrology

## Unique Picosecond Laser Ultrasonics



Ultrafast laser generates a sound wave at the surface of the filmstack

The sound wave moves down through the film until it reaches an interface

An "echo" is generated at the interface and travels back to the surface where it is detected by a change in reflectivity

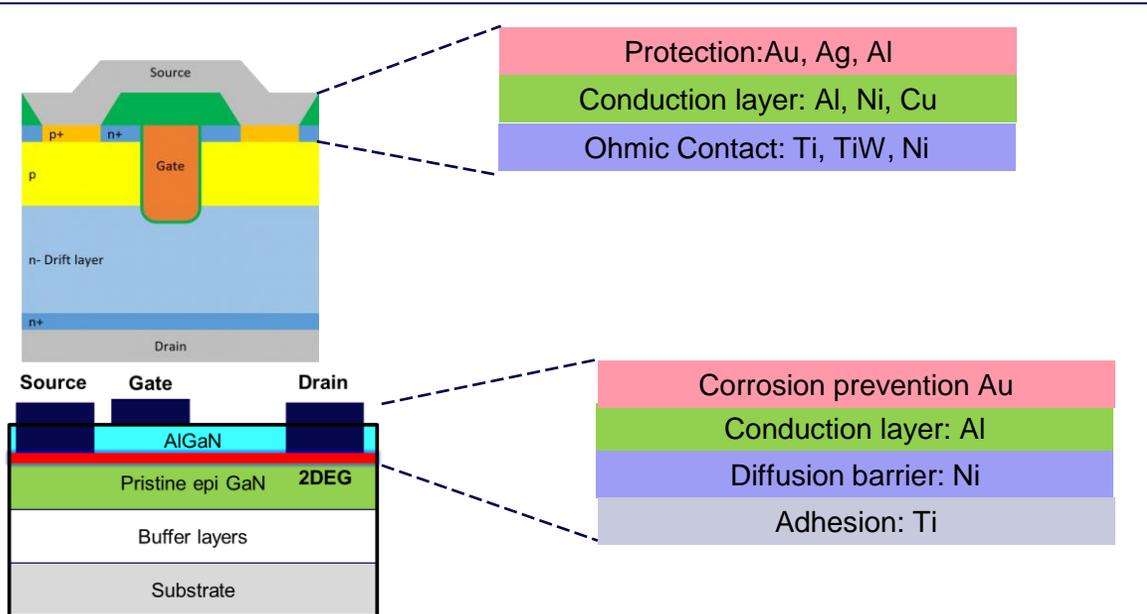
The sound wave and its reflections continue to travel, resulting in further reflectivity changes at the detector

Time to the Echo = Thickness

Size/shape/decay of echo = Material Properties (roughness, adhesion, density)

# Opaque Films Challenges, and HVM Solution

## SiC and GaN Power Device Metal Process Challenges

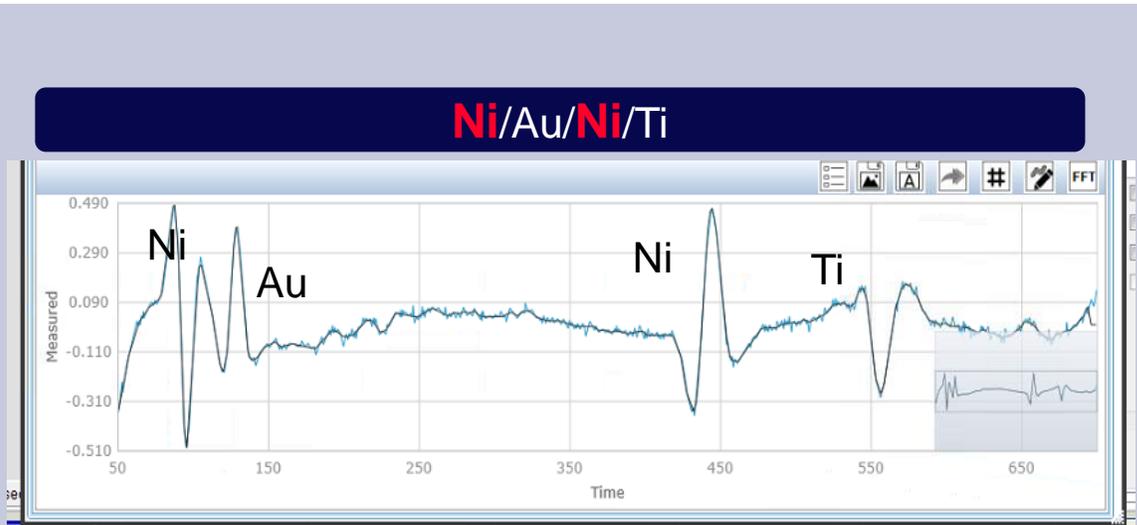
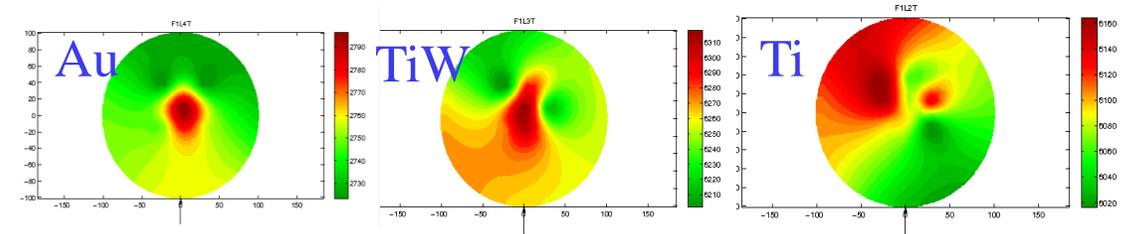


### Metallization Challenges & Requirements

- **Contact resistance** control between metal and SiC
- **Multi-layer thickness** control for each layer
- **Uniformity control** for 10-20nm thin films like diffusion barriers
- **Uniformity control** for > 150mm wafers

Need HVM-ready non-destructive high throughput method to monitor multi-layer metal films

## Multi-layer measurements

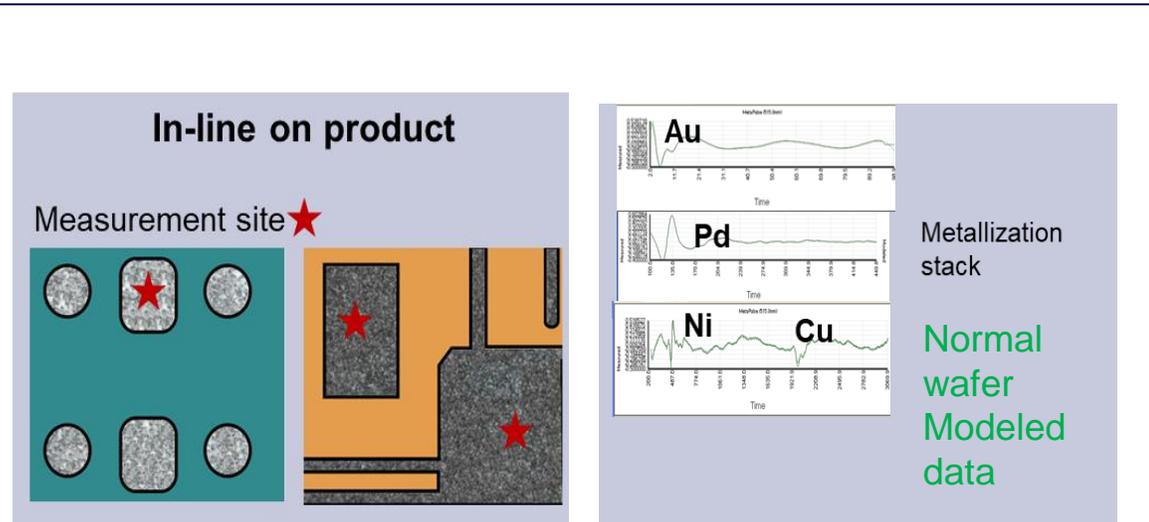


Within-wafer uniformity mapping

Measurement of repeating layers of same metal

# Opaque Films Challenges, and HVM Solution

## Multilayer metallization stack; in-line HVM solution

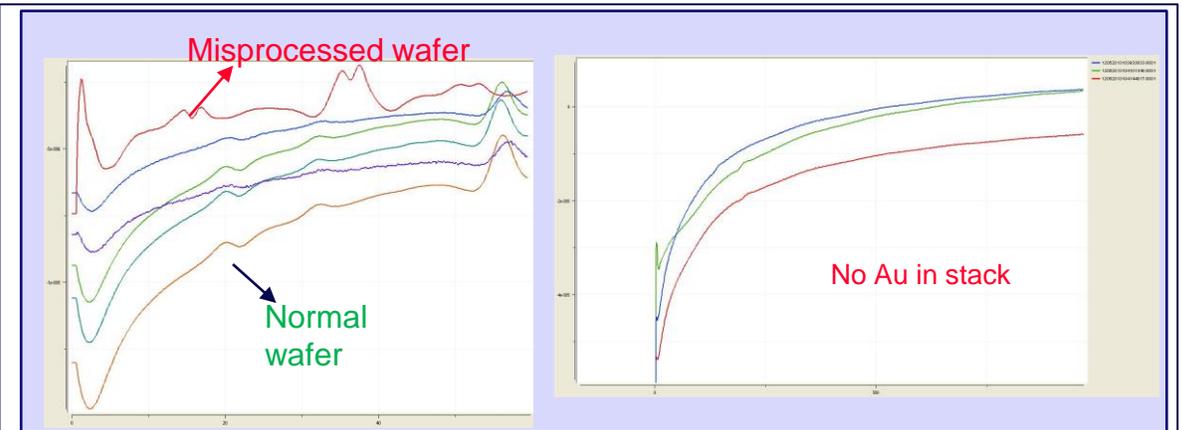


### ❑ Metallization Challenges & Requirements

- Simultaneous measurement
- Gage-capable **repeatability** on on wafer; pattern loading effects
- Detection of **missing layers** or misprocess

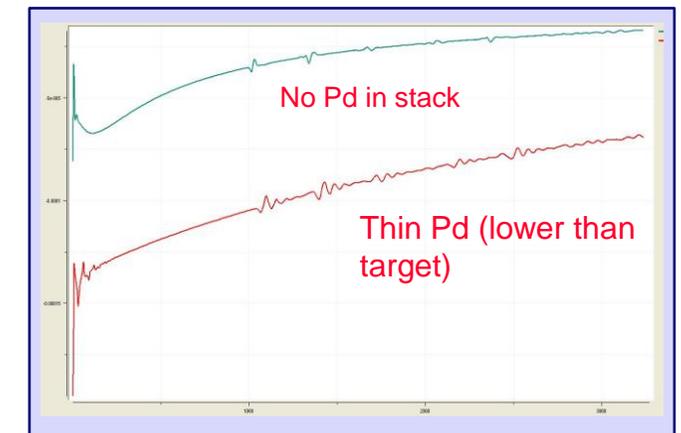
Metalization: Simultaneous measurement of multi layers

## Misprocess Detection Au/Pd/Ni/Cu



### ❑ Echo signatures

- Missing layers or misprocessed layers in 4-layer stack flagged automatically using GOF criteria
- Data validated w/X-SEM

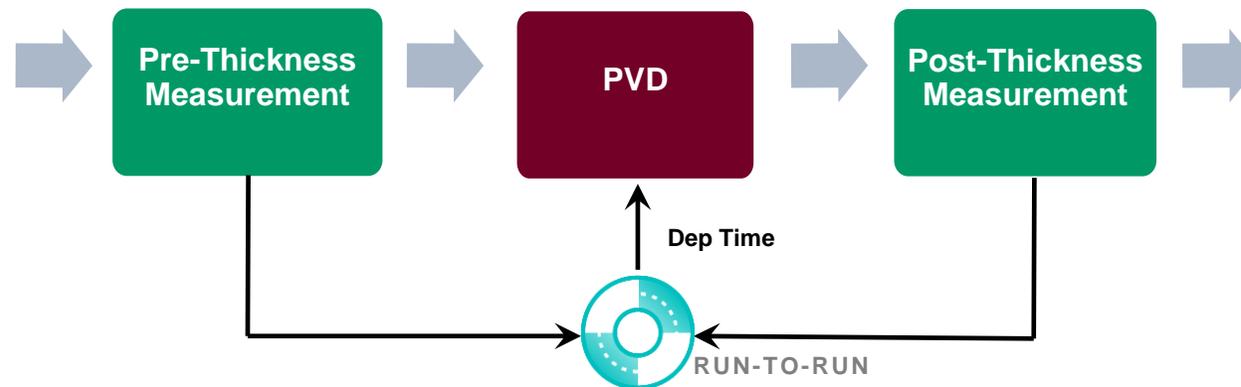
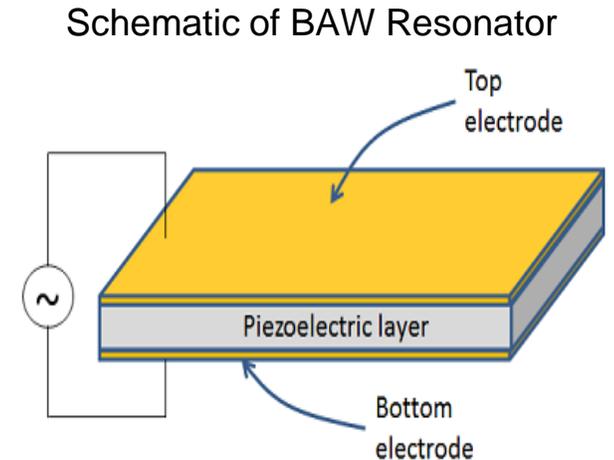


HVM solution for detecting misprocessing

# Example of Total Solutions: W-i-W Frequency Mismatch

**Unique HW + Enterprise SW + Customer HVP = Solution**

- **Issue:**
  - High WiW non-uniformity of film deposition across the wafer can lead to different frequencies in MEMS devices center-to-edge of the wafer
- **Onto Solution:**
  - **ECHO™** can measure metal films in-line
  - **Discovery R2R** monitors the film, data are fed forward/backward into the PVD chamber for precise WiW and WtW thickness control of PVD piezoelectric films
- **Result:**
  - 50% - 100% improvement in Cpk is seen in film thickness uniformity and stress



Experience the Power of

**Connected Thinking**

# Conclusions

## M&I Technology Adopted for Advance Nodes now used in Specialty Markets

Technology	Solutions for SiC/GaN
<b>FTIR:</b> <ul style="list-style-type: none"><li>Fast, non-contact, non-destructive and accurate measurements of films thickness and carrier concentration</li></ul>	<ul style="list-style-type: none"><li>Accurately monitor epi layer thickness and dopant concentration, thereby reduce variability of <math>V_{bd}</math> and <math>R_{on}</math> in devices W-i-W and W-t-W</li></ul>
<b>OCD/Thin-Film Metrology:</b> <ul style="list-style-type: none"><li>Optical characterization for trench and recess etch critical dimensions</li><li>Spectroscopic ellipsometry for thin film thickness mapping</li></ul>	<ul style="list-style-type: none"><li>Control of trench top/bottom CD accurately extends inversion layer in drift region</li><li>Measurement/control of corner rounding reduces localized hot-spots resulting from high electric field density</li><li>OCD metrology enables excellent control of S/D recess etch in GaN – critical for making ohmic contact</li></ul>
<b>Opaque Films Metrology</b> <ul style="list-style-type: none"><li>Unique acoustic technology to monitor metal films</li><li>Multiple layers can be monitored simultaneously, and missing layers can be flagged</li></ul>	<ul style="list-style-type: none"><li>Accurate control of thin films will ensure good adhesion and diffusion-barriers in metal stack</li><li>Thin film control will become much more critical as SiC wafers transition from 150mm to 200mm</li></ul>

# Onto Innovation's Major Products



**Atlas® V, Atlas® S**  
Standalone thin film and  
OCD metrology



**Element™ S**  
FTIR metrology



**JetStep®**  
Litho for Advanced Packaging and FPD



**Aspect®**  
OCD metrology for 3D NAND and  
high aspect ratio structures



**AWX™ FSI**  
Unpatterned frontside inspection



**Analysis Software**  
Inline yield and defect management



**IMPULSE® V**  
Integrated thin film and OCD metrology



**EB40® / NovusEdge®**  
Automated all-surface defect inspection  
for patterned and unpatterned wafers



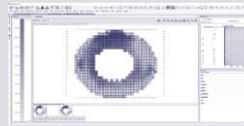
**Control Software**  
Fabwide R2R and FDC



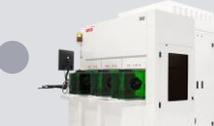
**Echo™**  
Acoustic film metrology



**Dragonfly® G3**  
2D/3D inspection and metrology



**Classification Software**  
ADC, SPR, and review solutions



**Iris™**  
Thin film and common  
OCD metrology



**Firefly®**  
Sub-micron panel inspection



**Ai Diffract™ Software**  
AI-guided OCD modeling  
and analysis software



**IVS™**  
Overlay and CD metrology



**NSX® and F30®**  
2D inspection, CD, RDL/TSV, 2D bump,  
2D/3D metrology, all-surface ready

- ≤ 200mm
- 300mm

# Thank You

谢谢 | 謝謝

Danke

ありがとう

감사합니다

Obrigado

Merci

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[www.ontoinnovation.com](http://www.ontoinnovation.com)