

CS International 2024

# Heterogenous Integration of Compound Semiconductors by W2W and D2W Bonding

Dr. Bernd Dielacher  
Business Development Manager

Leading supplier of wafer processing equipment for the MEMS, nanotechnology and semiconductor markets

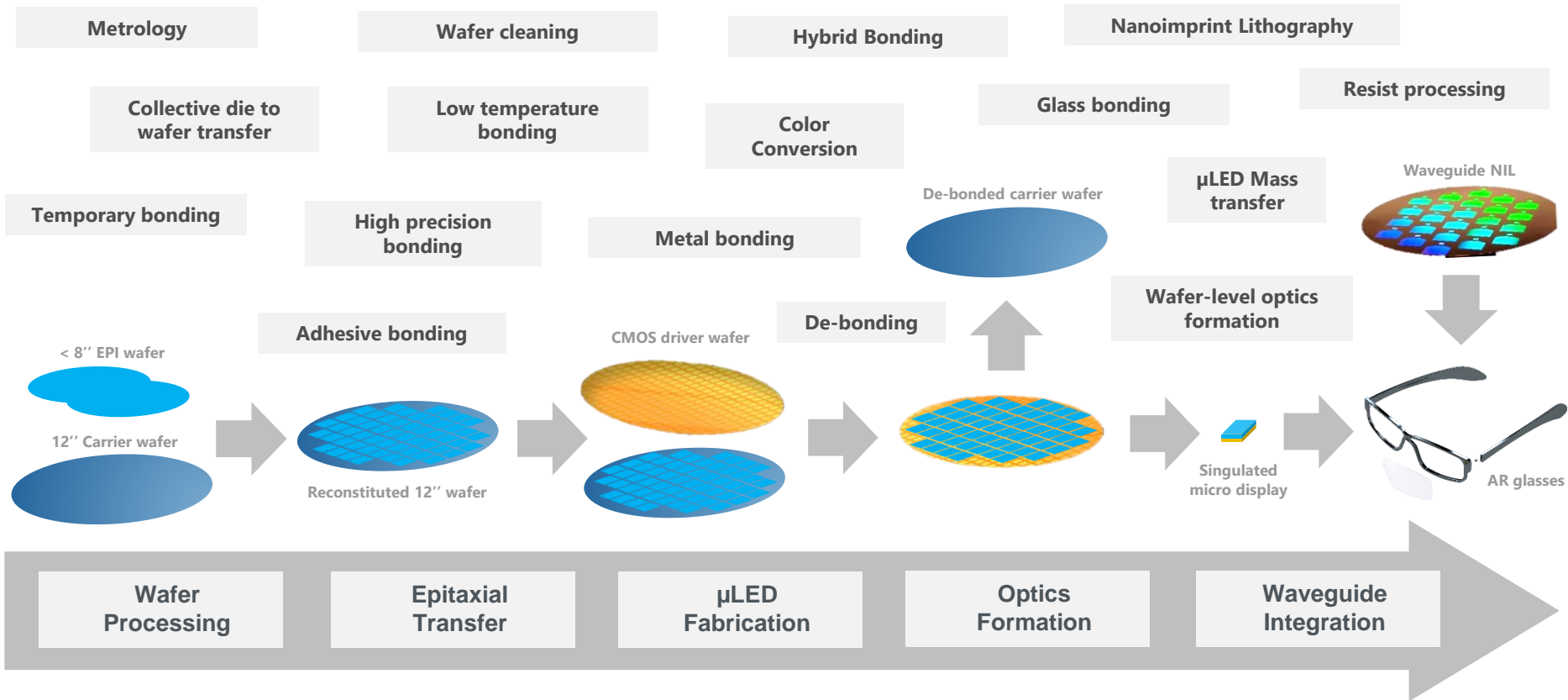
Founded in 1980 by DI Erich and Aya Maria Thalner. More than 1300 employees worldwide

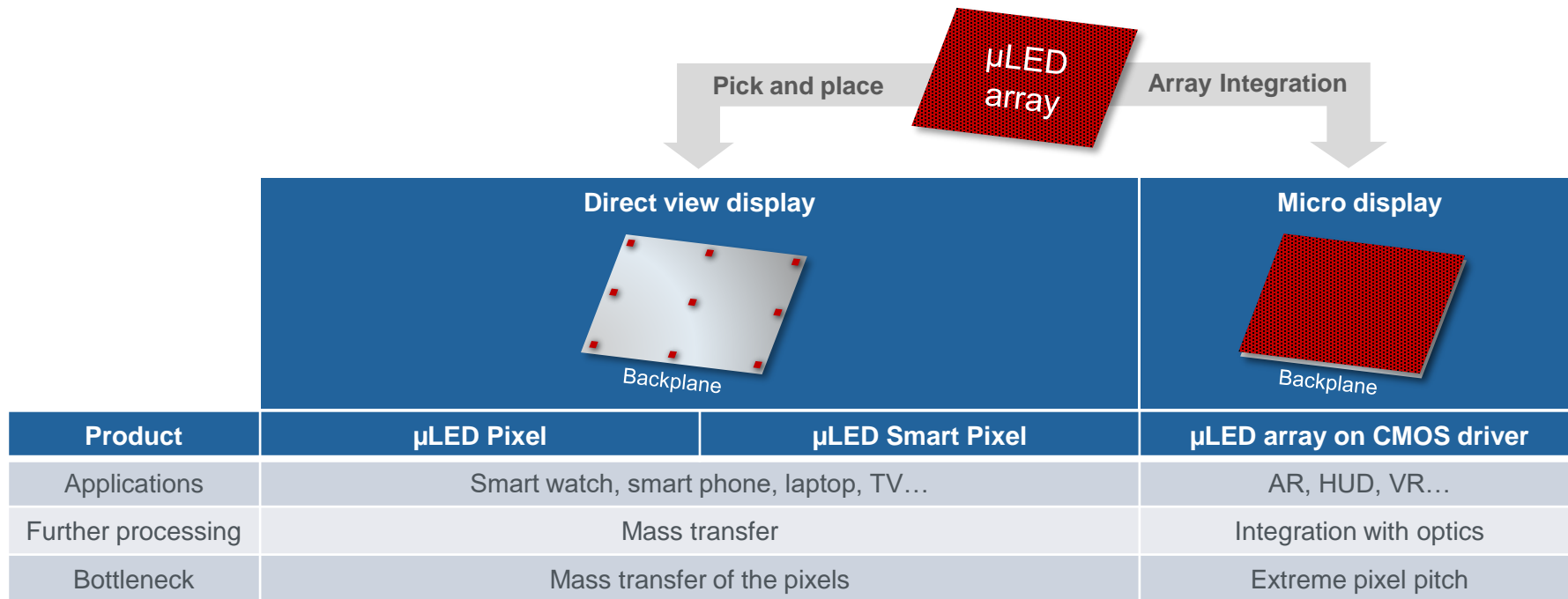
Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China and Taiwan



EV Group Headquarters  
St. Florian am Inn, Austria

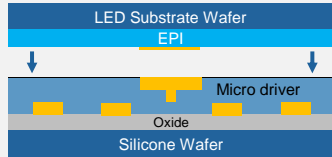
# EVG Enables Full Process of $\mu$ LED Displays Fabrication



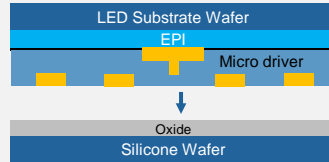


The following slides show a representative but not full list of EVG technologies for μLED displays manufacturing.  
The process flows vary significantly from company to company.

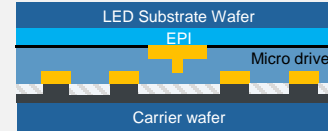
## 1. Adhesive bond, Metal aligned bond



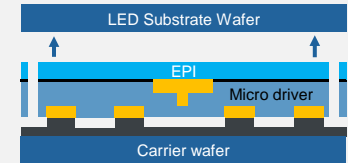
## 2. Carrier removal



## 3. Adhesive bonding



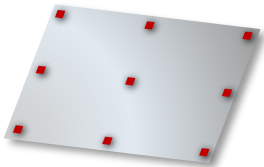
## 4. Substrate LLO, Patterning + Etching



Next step: mass transfer



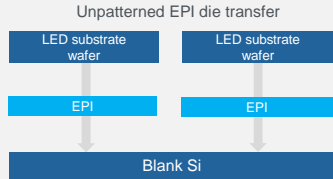
Smart pixel process requires a wide range of bonding technologies, including adhesive and metal bonding



Direct View Display

EVG Technology	Application	Equipment
Ultra Thin Layer Transfer	CMOS driver substrate (SOI)	EVG850LT
IR-Laser Release	Alternative to thinning and wet oxide etching	EVG850DB
Adhesive bonding	EPI transfer + LED transfer	EVG5XX, EVG850, Gemini
Laser Lift Off	EPI substrate removal	EVG850DB
Metal Bonding	Integration	EVG5XX, Gemini

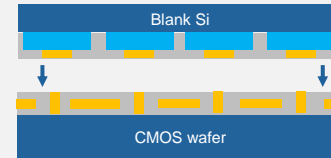
## 1. LED wafer reconstitution



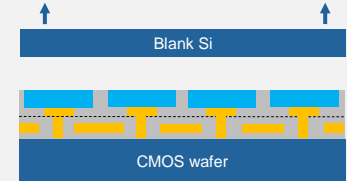
## 2. Reconstituted wafer planarization and patterning.



## 3. Hybrid bond



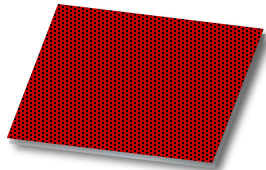
## 4. Carrier removal,



Next steps:  
Optics, color conversion integration



μDisplay manufacturing requires high precision aligned bonding to fulfill the fine pixel Pitch requirements



Micro Display

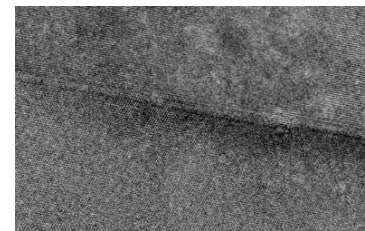
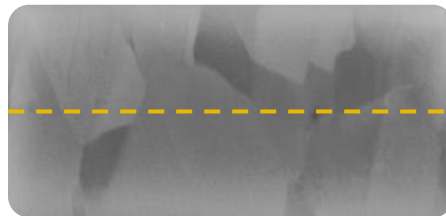
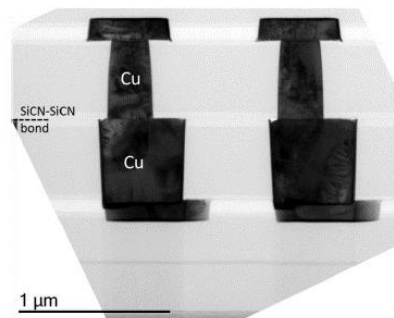
EVG Technology	Application	Equipment
Laser Lift Off	EPI substrate removal	EVG850DB
Wafer Reconstitution	Utilization of 300mm frontend semiconductor processing	EVG320
Hybrid bonding	Fine pitch bond of the μLED EPI wafer to the CMOS driver wafer	GEMINI FB
NIL	Optics formation	EVG7XXX
Spin & Spray coating	Color conversion layer deposition	EVG1XX





Wafer bonding is a key technology in heterogenous integration of compound semiconductor materials

No Interlayer	Anodic	Pitch
	Fusion	2 $\mu$ m
	Hybrid	2 $\mu$ m
Metal Interlayer	Thermo-Compression	5 $\mu$ m
	Solder-based Eutectic/TLP	30 $\mu$ m
Insulating Interlayer	Adhesive	30 $\mu$ m
	Glass Frit	



# Wafer Bonding | Transient Liquid Phase Bonding

→ Reducing residual stress by lowering the bonding temperature



→ Bonding temperature needs to be minimized

→ **Solution: Transient Liquid Phase (TLP) Bonding**

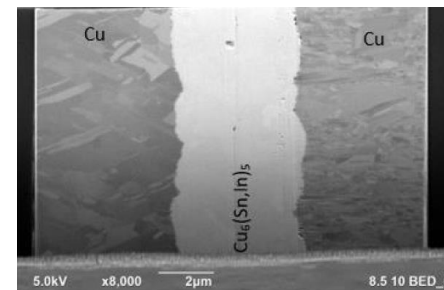
- Bonding at lower temperature
- Re-melting temperatures much higher than bonding temperature

Transient Liquid Phase Bonding	
Au-In	180 °C
Cu-Sn	250-280 °C
Ni-Sn	280-300 °C
Ag-Sn	250-280 °C
Ag-In	180 °C
Cu-In	170-180 °C
Cu-In-Sn	150 °C

Bonding temperatures of available TLP material systems are clearly below commonly utilized eutectic, anodic or glass frit bonding

→ Latest Developments:

Successful bonding of Cu-In-Sn @ 150 °C





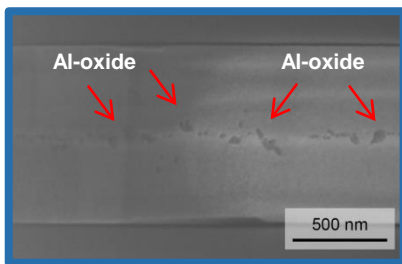
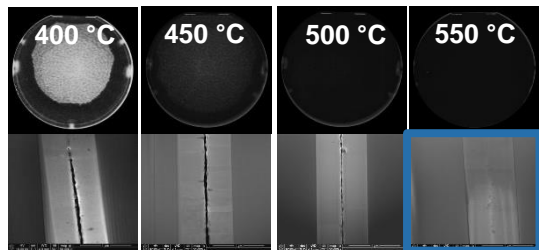


ComBond® technology allows for low-temperature oxide-free metal bonding (e.g. Al-Al)

## Conventional Bonding



Increasing temperature leads to increasing bond interface quality

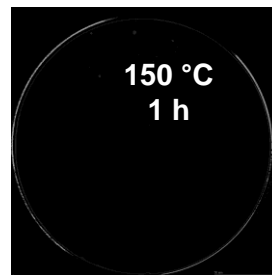


C-SAM  
measurements  
and SEM  
images

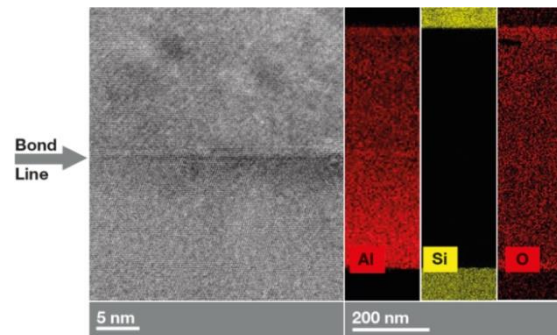
## EVG Combond®



High bond quality and strength at low temperature



No O<sub>2</sub> concentration difference between bulk and interface

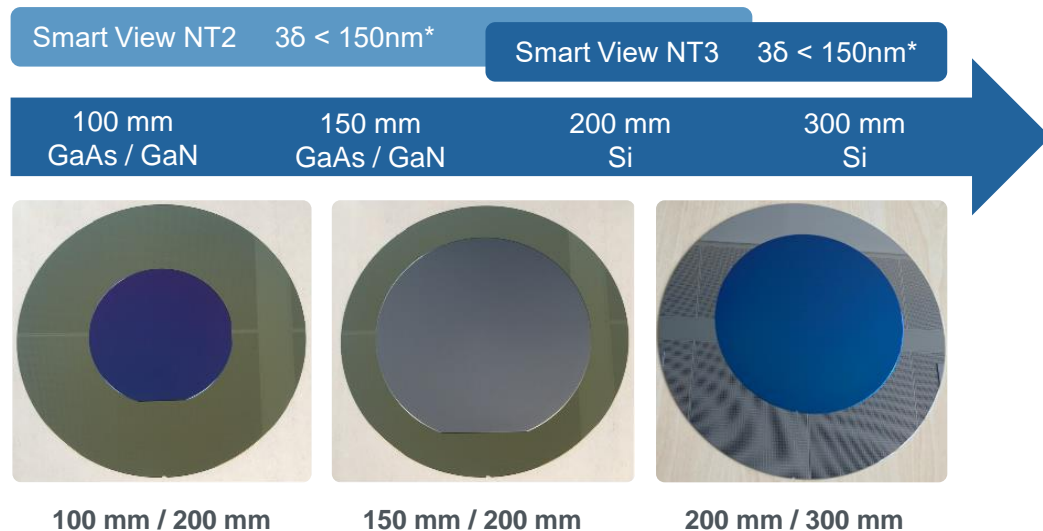


No aluminum oxide precipitates

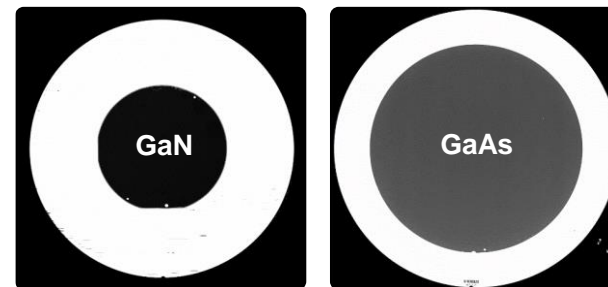
# Heterogenous Wafer Bonding | Different Substrate Dimension



Bonding of wafers of different size enables seamless integration of EPI and CMOS wafers



Bonding area > 99%



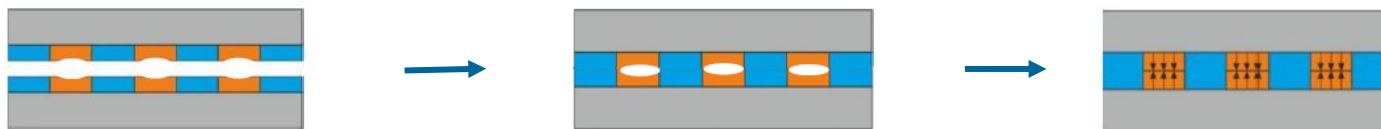
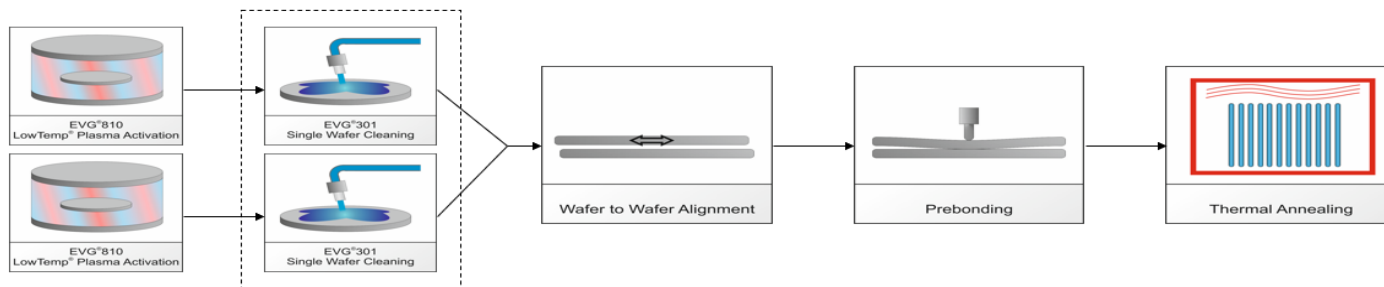
100 mm / 200 mm

150 mm / 200 mm

Scanning Acoustic Microscopy

\*LED applications

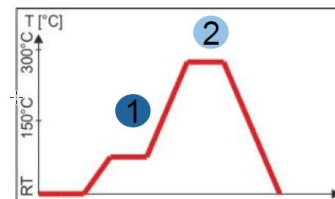
# Wafer Bonding | Fusion and Hybrid Bonding



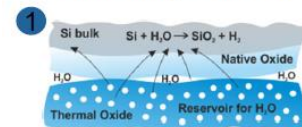
Wet cleaning and plasma activation are applicable for surface preparation.

Wet cleaning can include the use of chemicals for metal oxide removal

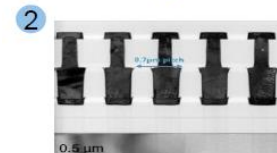
Wafers will be aligned using F2F optical alignment. Once aligned, wafers will be contacted at room temperature.



## Annealing Process

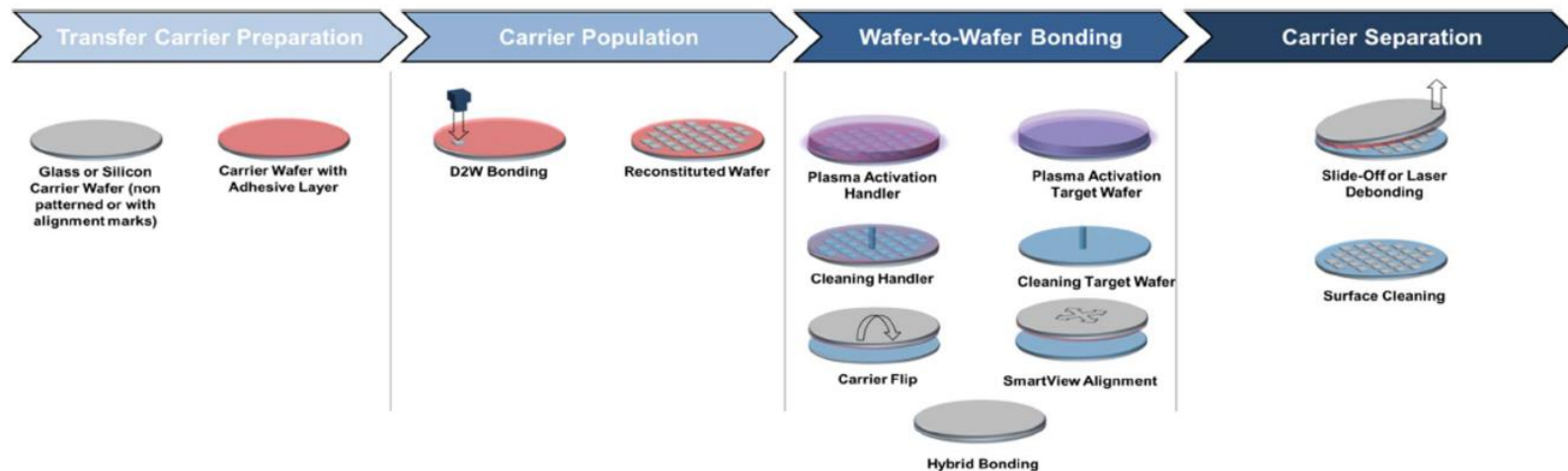


## Dielectric layer Annealing



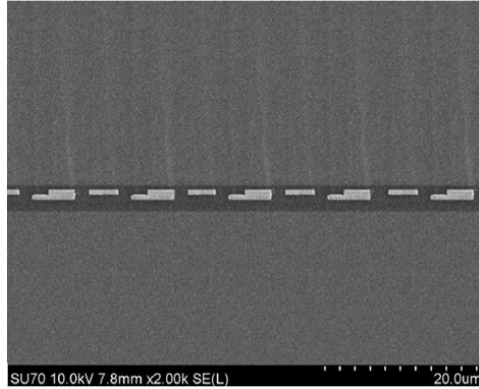
Interconnect gap closure due to different CTE of Dielectric bonding material and interconnect material

# D2W Bonding | Collective D2W Process Flow

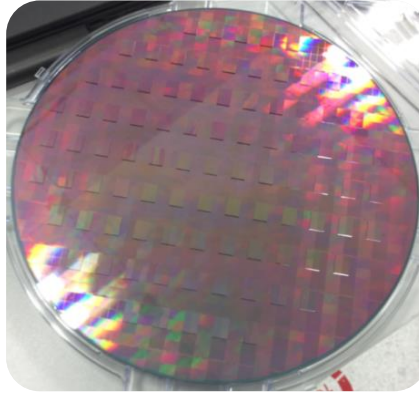


Transfer Method	Pro's	Con's	Maturity
Collective Die Transfer by Reconstituted Carrier	<ul style="list-style-type: none"> <li>Proven technology</li> <li>Die Activation and cleaning equivalent to W2W hybrid bonding</li> <li>Oxide management</li> <li>Rework on carrier feasible</li> </ul>	<ul style="list-style-type: none"> <li>Error propagation of D2W + W2W alignment</li> <li>Cost of carrier prep, utilization and clean</li> <li>Die thickness needs to be in narrow range</li> </ul>	Application specific volume production proven for several years

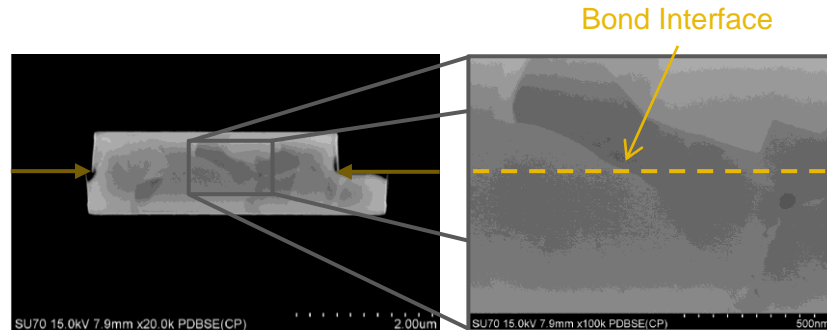
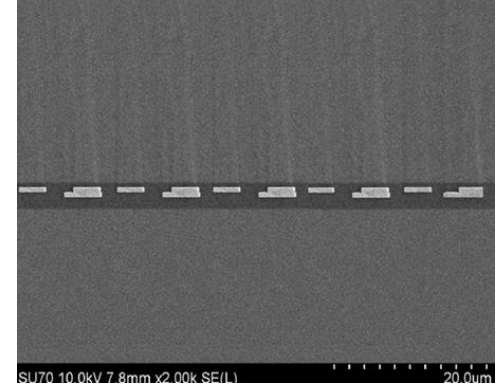
Edge Die



300mm 10x14 Dies



Center Die



High Die transfer rate and alignment accuracy < 2μm

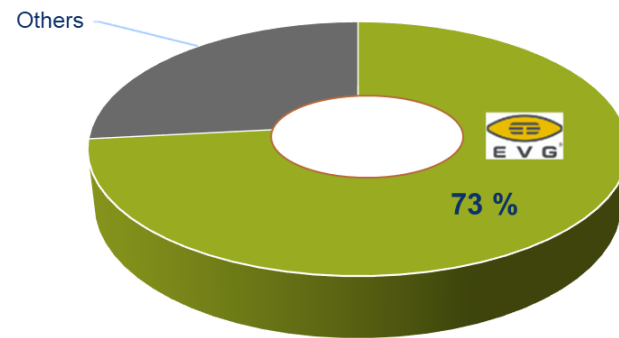


TEM evaluation of mechanical contact of the bonding pads and Cu grain growth across the bonding interface

→ **EVG** is market leader in **wafer bonding**, a **key technology** for μLED displays manufacturing. Our solutions go beyond bonding and enable many **AR** and **VR** applications for the industry leaders.

- **Other Key Technologies for μLED manufacturing**
- Waveguides nanoimprint
  - Wafer-level micro-optics
  - Mass transfer

2020 Permanent Bonding Market Share  
Breakdown by Player Revenue (\$M)



*Image adapted from "Bonding and Lithography Equipment Market for Moore than Moore Devices | Report | Yole Développement | 2021"*

Bonding  
Technologies





# Thank you!

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