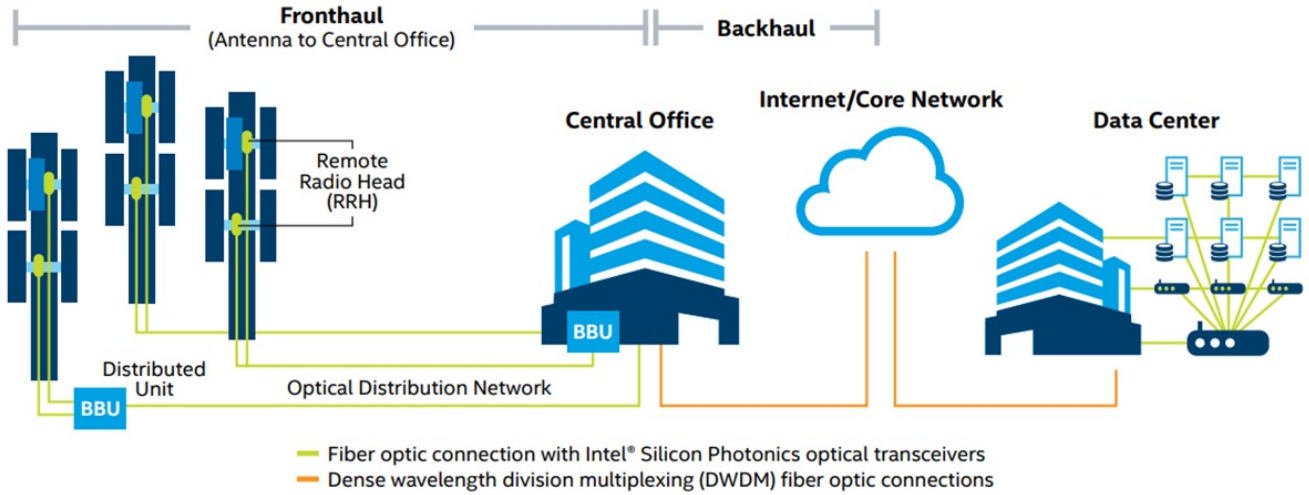
Towards a Comprehensive Multiphysics Design Solution for CPO

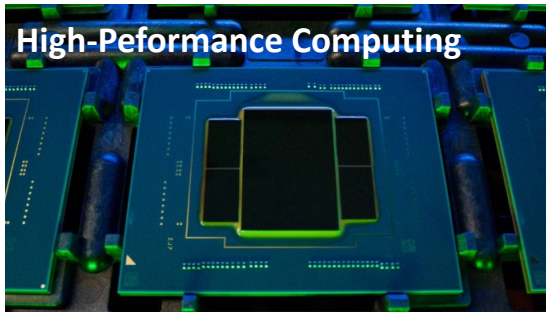
Ahsan Alam

Lead R&D Engineer

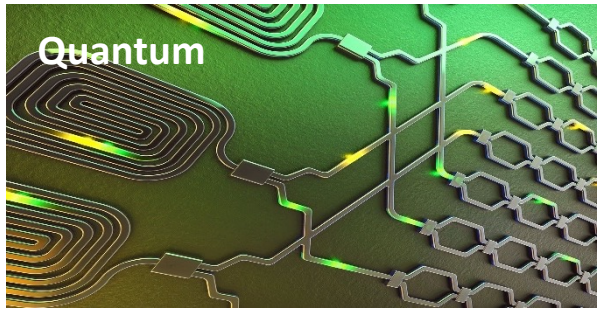
Photonics is a Key Enabler of 5G, Data Centers, AI and More



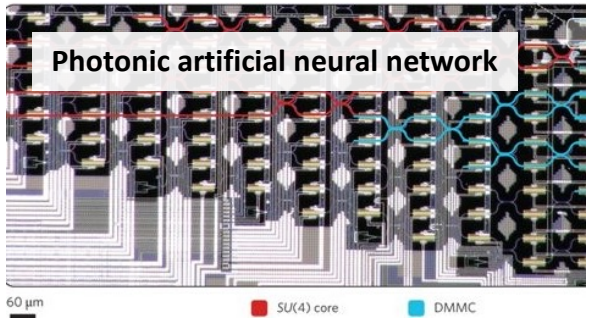
Source: "Exploring 5G Fronthaul Network Architecture Intelligence Splits & Connectivity" 5G Wireless Communications – Silicon Photonics, Intel



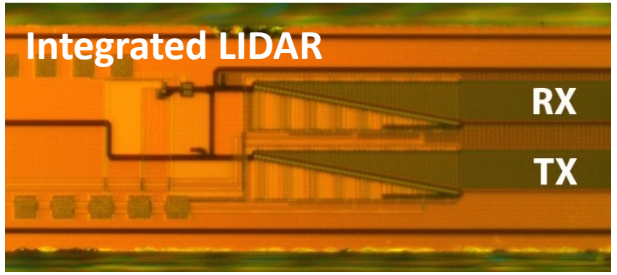
High Performance Computing | Ayar Labs In-Package Optical I/O
https://ayarlabs.com/high-performance-computing/



https://spectrum.ieee.org/tech-talk/computing/hardware/building-quantum-computers-with-photons
Image: Xiaogang Qiang/University of Bristol



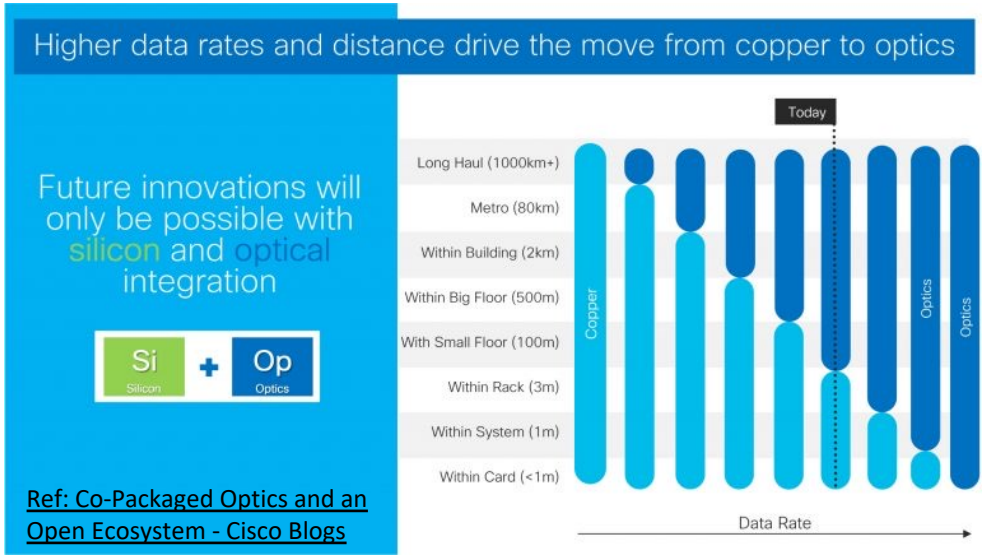
Y. Shen et al. Deep learning with coherent nanophotonic circuits,
Nature Photonics,
https://doi.org/10.1038/nphoton.2017.93



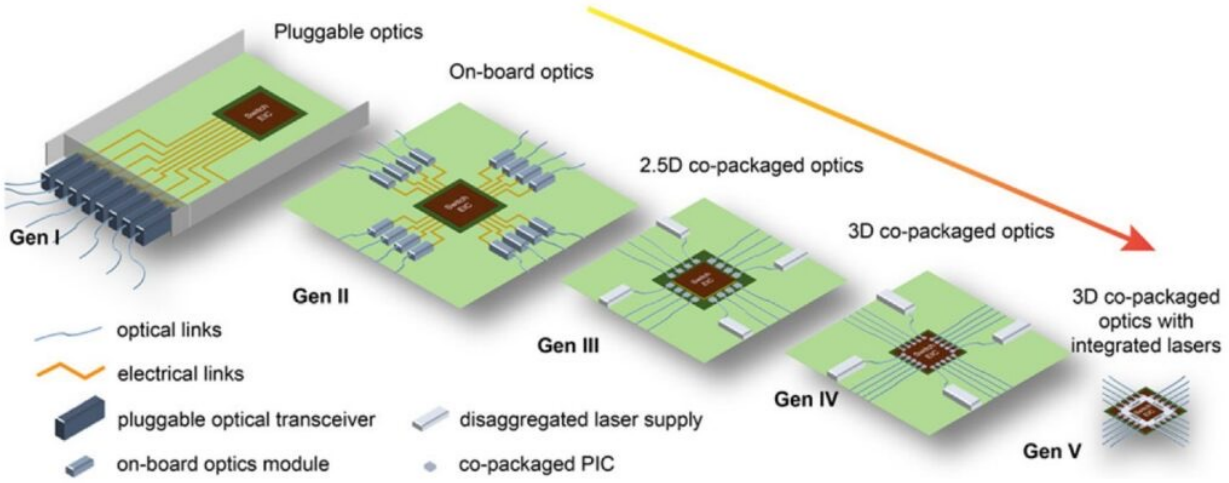
MIT and DARPA Pack Lidar Sensor Onto Single Chip
https://spectrum.ieee.org/tech-talk/semiconductors/optoelectronics/mit-lidar-on-a-chip
Image: Christopher V. Poulton

Why Co-Packaged Optics?

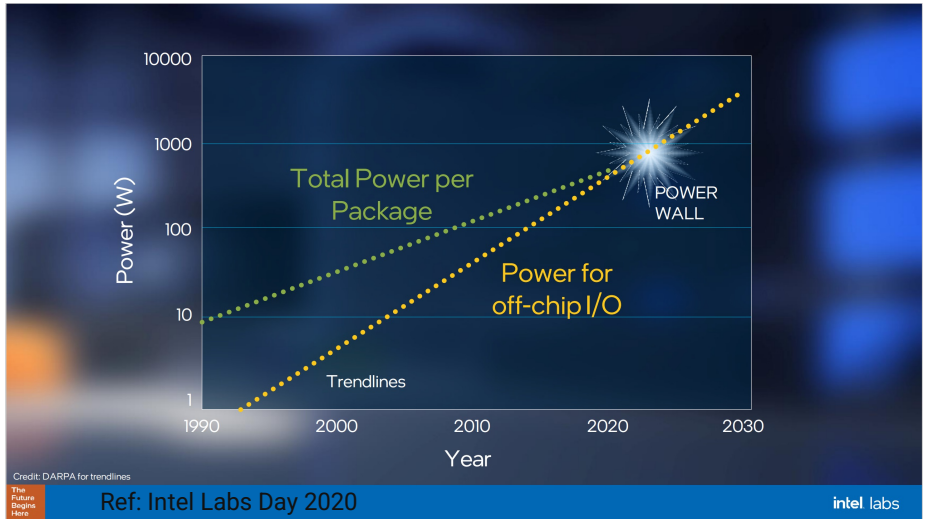
- Traditional Cu interconnects cannot scale to current requirements
- Optical interconnects will continue to replace copper
- Current optical interconnects provide increased scalability, but power/cost requirements become untenable
- Co-packaged optics brings power and cost down and allows for breaking through the “power wall”



Ref: Co-Packaged Optics and an Open Ecosystem - Cisco Blogs

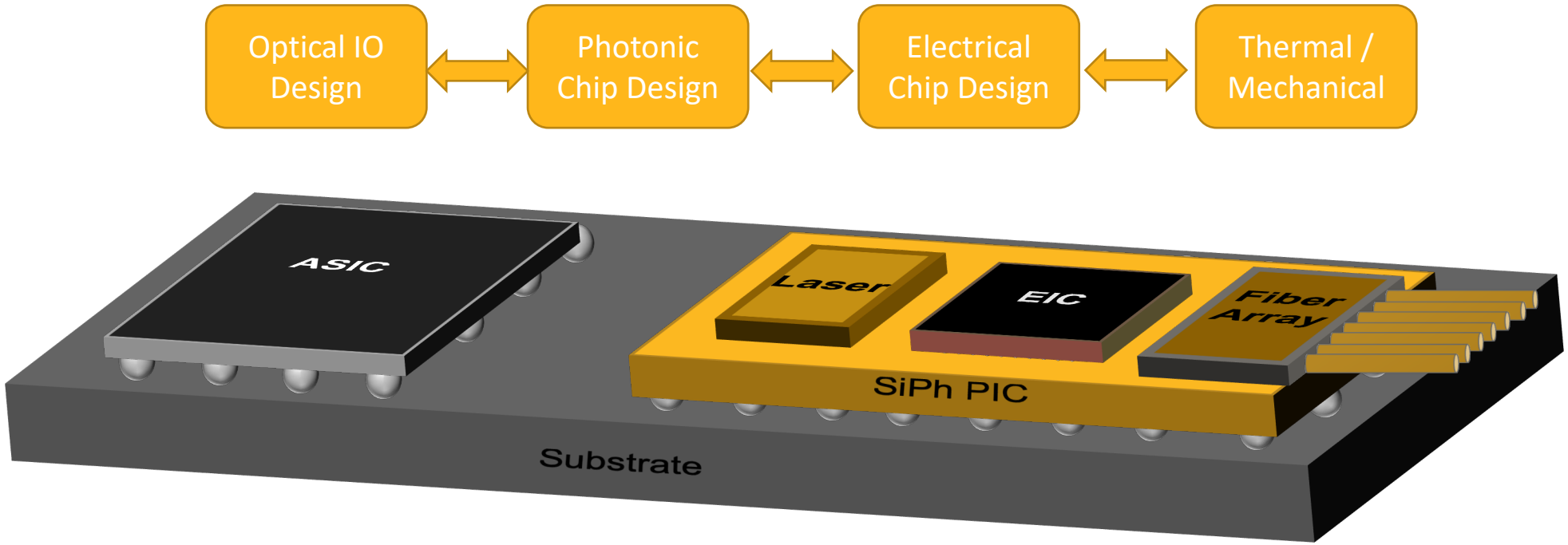


Ref: “Perspective on the future of silicon photonics and electronics” N. Margalit, et.al., Appl. Phys. Lett. 118, 220501 (2021)

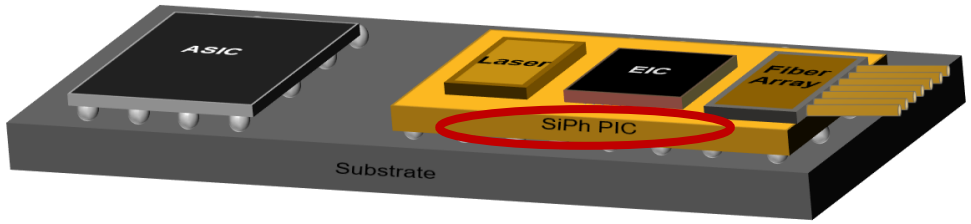


Co-Packaged Optics Challenges

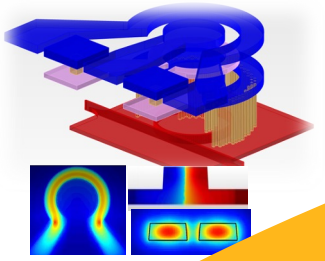
- New technologies such as co-packaged optics, introduce new design complexities for 3D-IC design.
- These challenges arise from the complex nature of full system design, involving multiple physics and scales, for example in optical I/O, thermal and RF modeling.



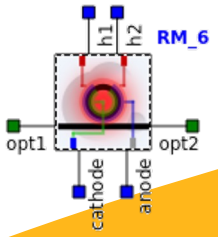
Multi-Platform PIC Design Ecosystem with Best-in-Class Tools



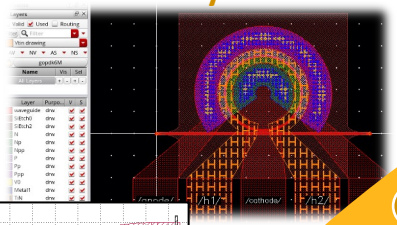
Ansys Lumerical
FDTD/MODE/CHARGE/
HEAT/FEEM/MQW

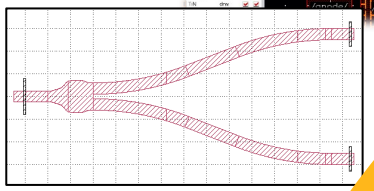


Ansys Lumerical
CML Compiler



Cadence
Virtuoso Layout Suite





KLayout

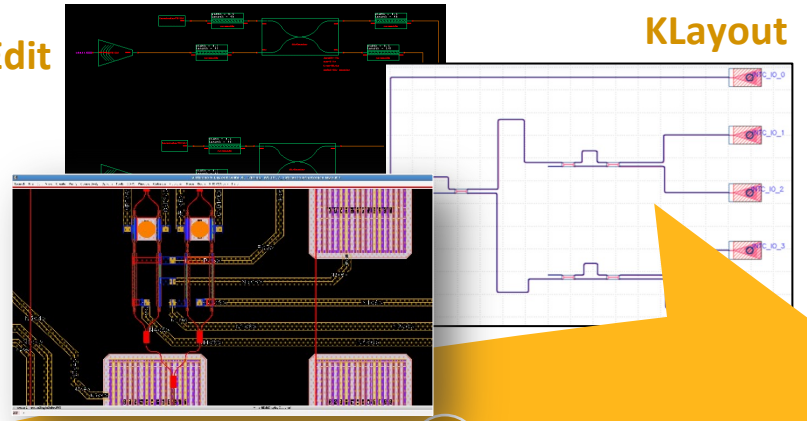
Photonic component layout

Photonic Multiphysics simulations

Photonic compact models

L-Edit

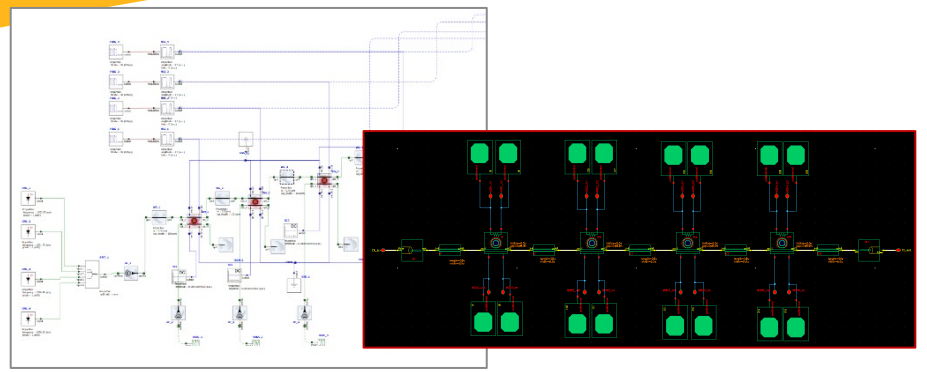
KLayout



Cadence
Virtuoso
Layout
Suite

SDL & LVS

Schematic-driven flows for circuit designs

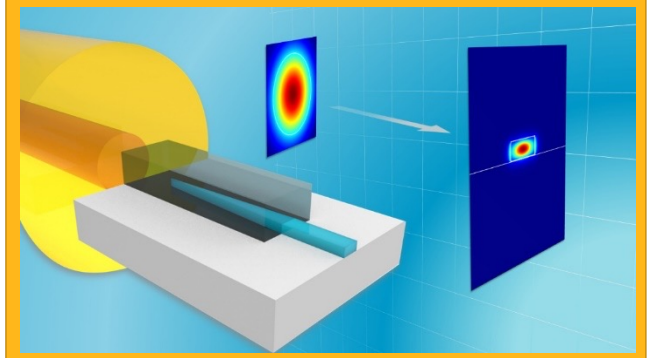


Lumerical
INTERCONNECT/Verilog-A & **Cadence**
Virtuoso ADE, Spectre/AMSD

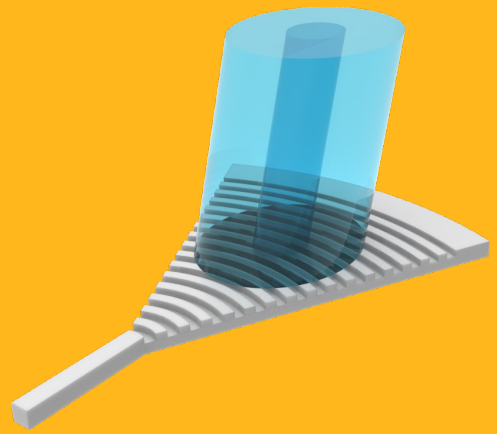
Optical Coupling to and from PIC

- Due to the large **mode size mismatch** between the optical fibers and waveguide, getting light in and out of PIC remains a challenge
- Common designs for getting light in and out of PIC:

Edge coupler

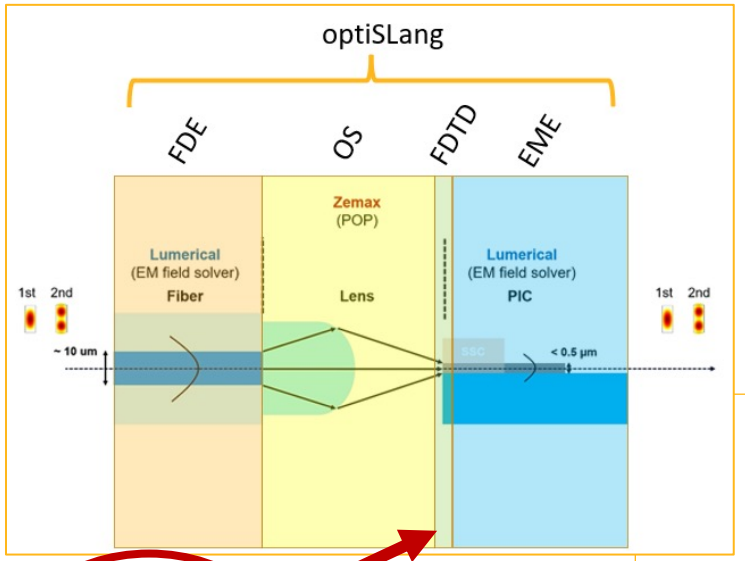


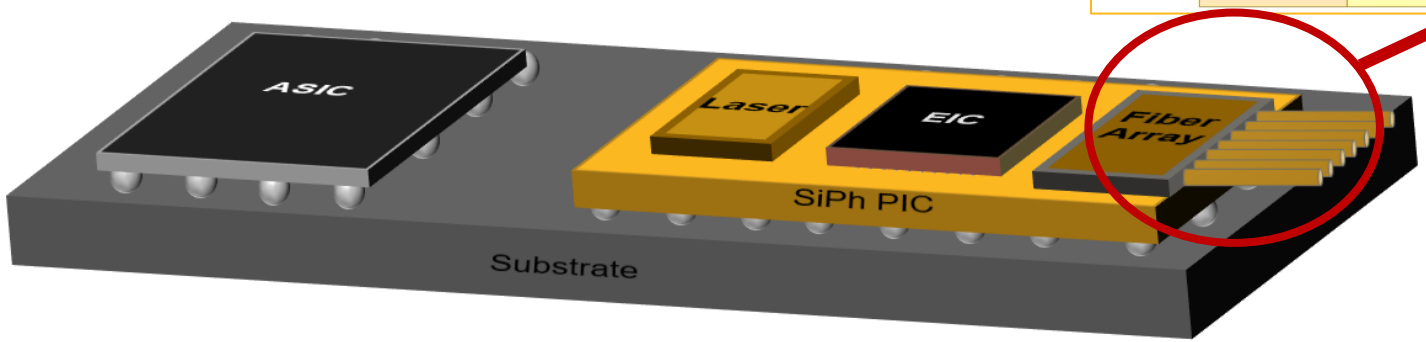
Grating coupler

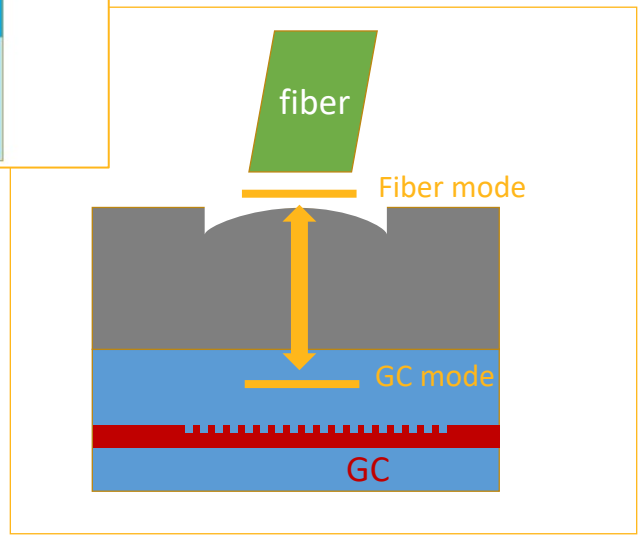


Optical IO Simulation

- Ansys **Zemax** and **Lumerical** offer interoperable tools that enable engineers to accurately account for both nano-scale and macro-scale optical effects in their devices, using ray tracing and Maxwell's equation-based simulation tools.
- Automated optimization workflows for both grating coupler and edge coupler to fiber coupling
- Robustness analysis and tolerancing against fiber misalignment and manufacturing variations

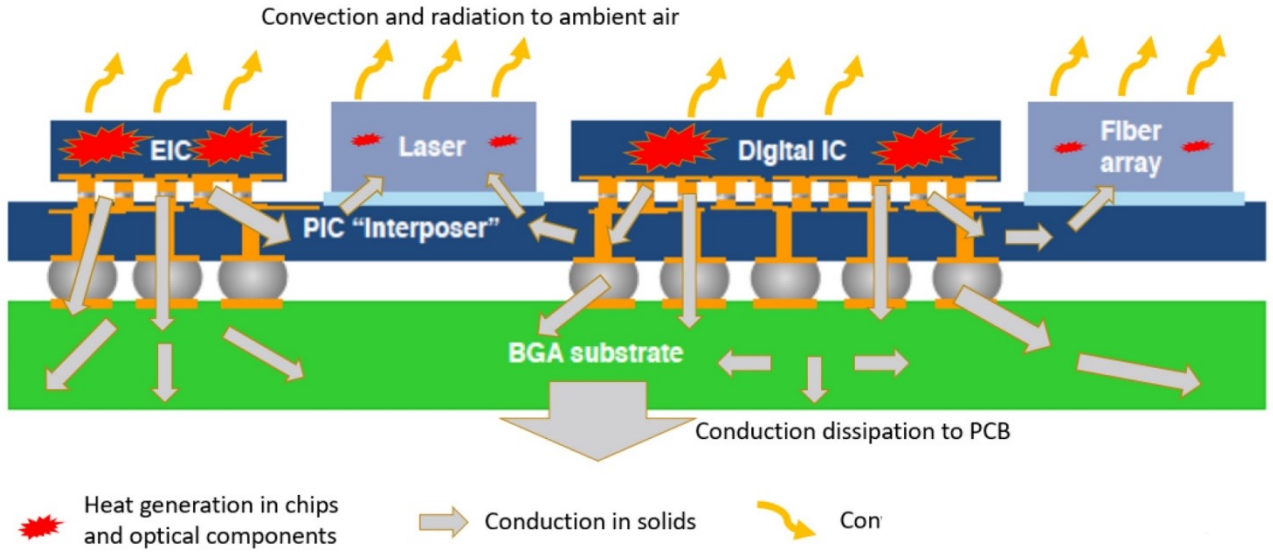






Thermal Effects

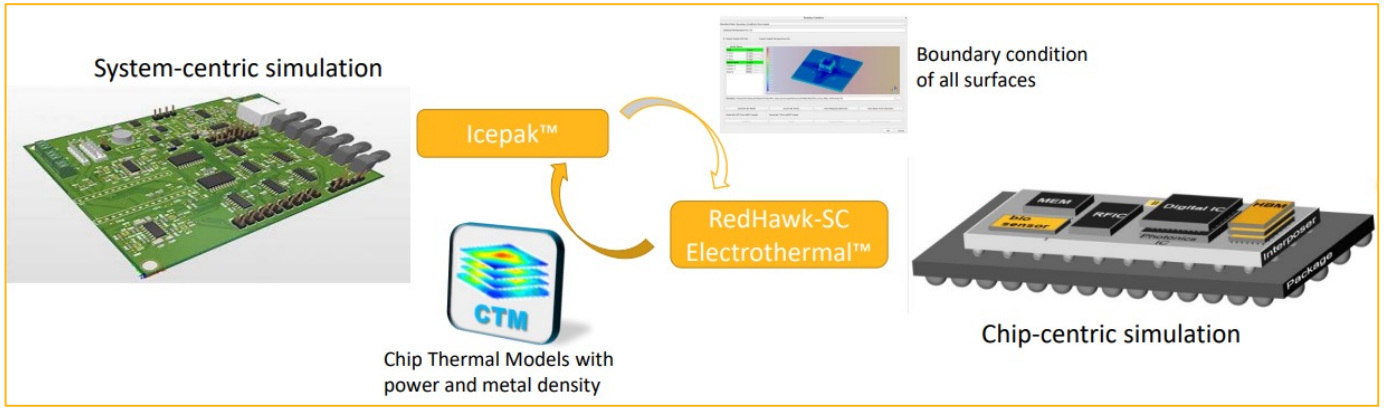
- Bringing electrical and photonic dies in proximity introduces thermal stability challenge
- Heat generated in ASIC, EIC, PCB, and PIC needs to be modeled and the possibility of thermal crosstalk need to be investigated
- Accurate estimation of thermal budget for photonic integrated circuit (PIC) is needed

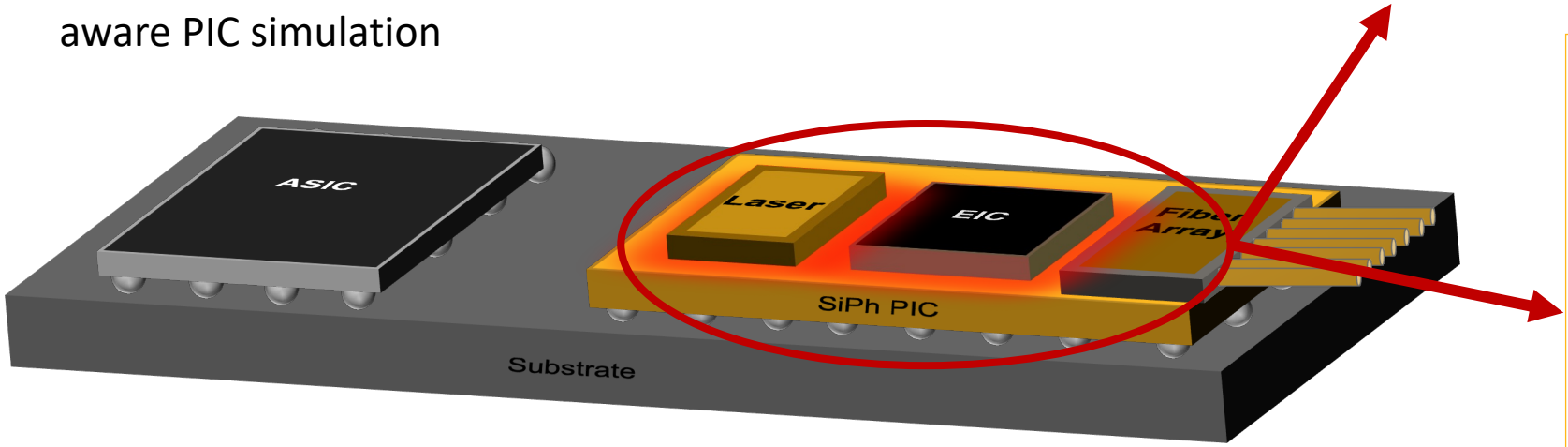


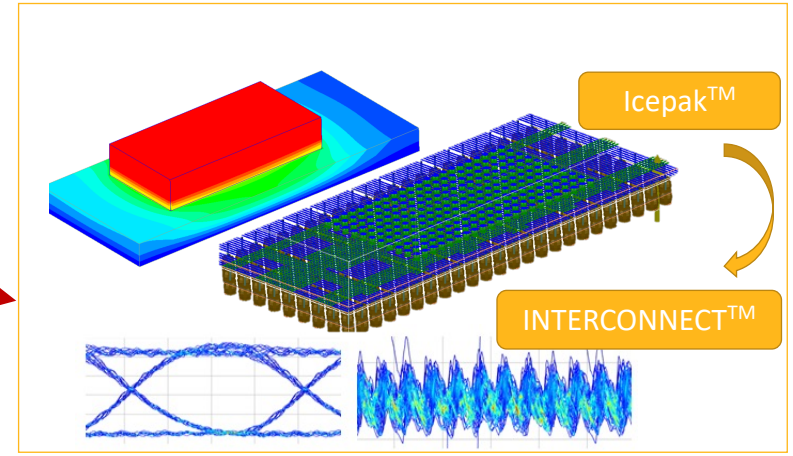
Thermal Analysis

- Ansys **Icepak** and **RedHawk-SC Electrothermal** in collaboration with **Lumerical** enable thermal analysis for 3D-IC designs including photonic integrated circuits.

- Run chip-level thermal simulation with RedHawk-SC Electrothermal and generate chip thermal model (CTM).
- Use CTMs for electrical and photonics dies in Icepak for full system level thermal simulation.
- Import temperature map from thermal simulation into INTERCONNECT for thermally-aware PIC simulation

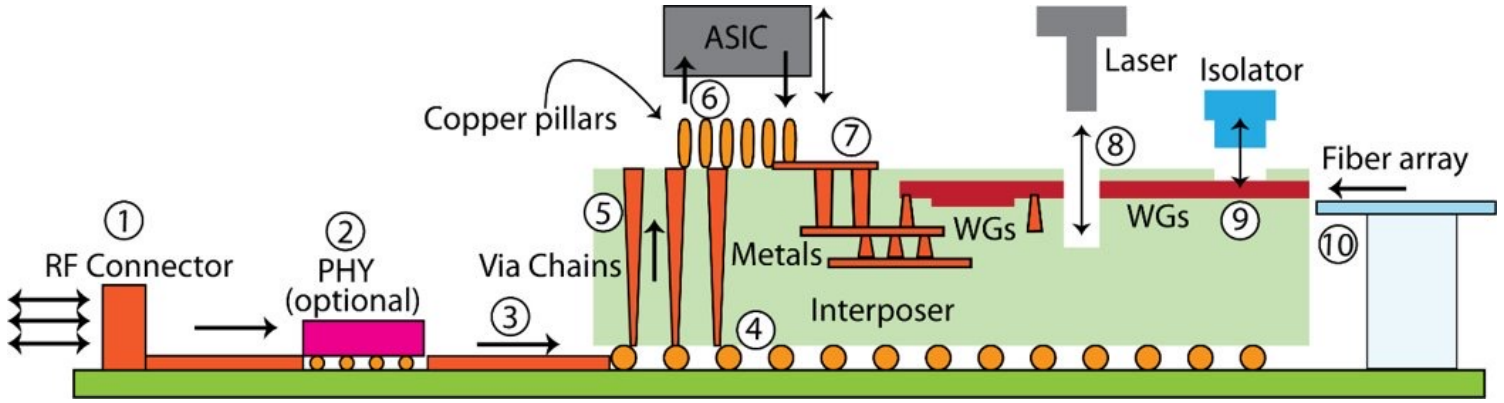






Packaging Interconnects Effects

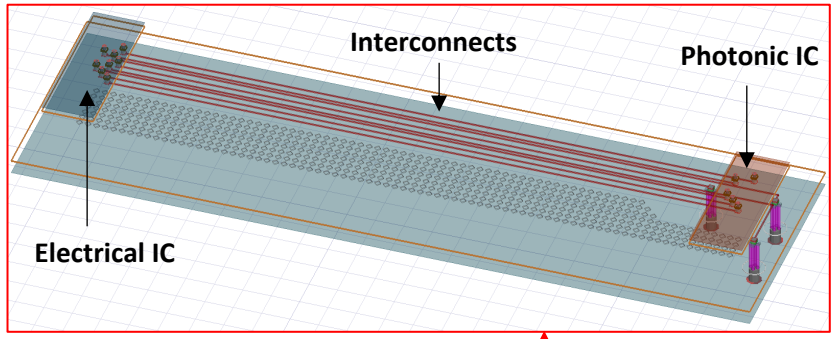
- Typical photonic circuit simulation/design does not include packaging interconnects, e.g., vias, BGAs, copper pillars, etc.
- Packaging interconnects can include additional loss and distortion to the RF signal and affect the overall signal integrity.
- Full electro-optical simulation with packaging interconnects is necessary.

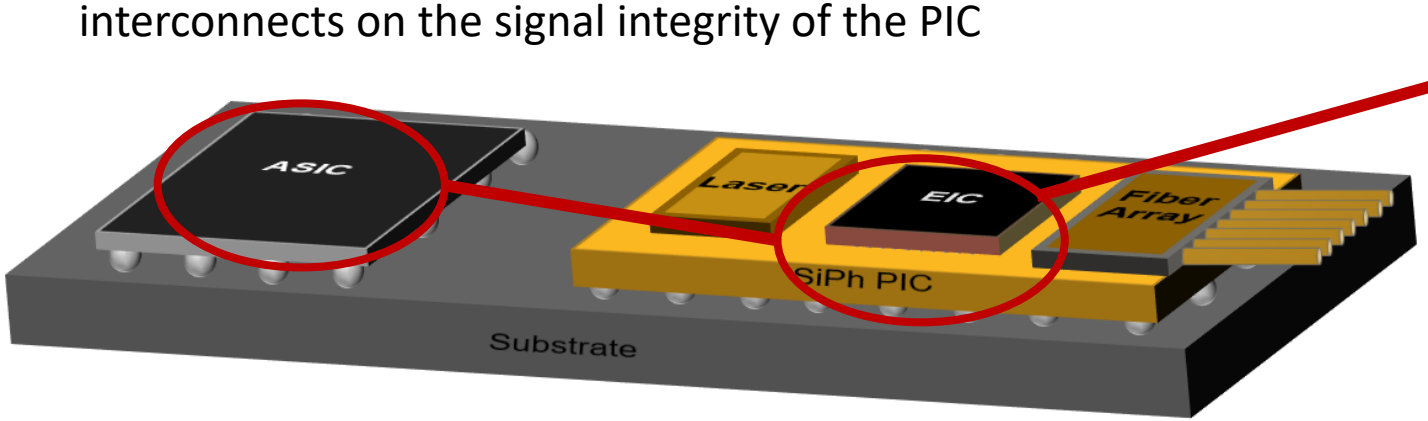


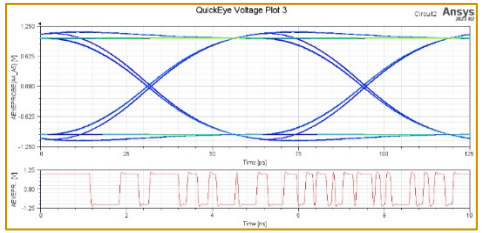
Signal Integrity Analysis

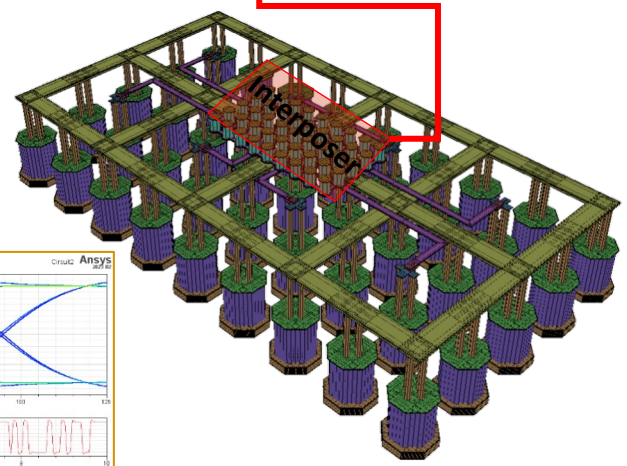
- Ansys **Lumerical** along with **HFSS, RaptorX** offer workflows for users to be able to do RF analysis for their 3D-IC designs to ensure the desired RF performance, minimize signal degradation, and optimize the overall functionality of the integrated circuit.

- Design RF connectors, e.g., ball-grid arrays (BGA) and transmission lines/traces in HFSS/RaptorX and extract S-parameters
- Import electrical S-parameters into INTERCONNECT and perform photonic integrated circuit simulation
- Account for the added noise and loss coming from the package interconnects on the signal integrity of the PIC





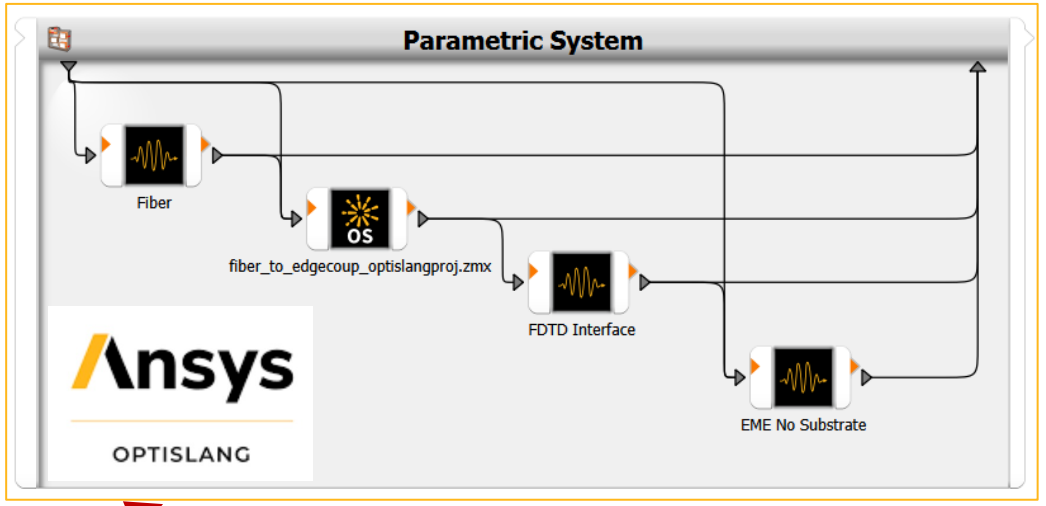


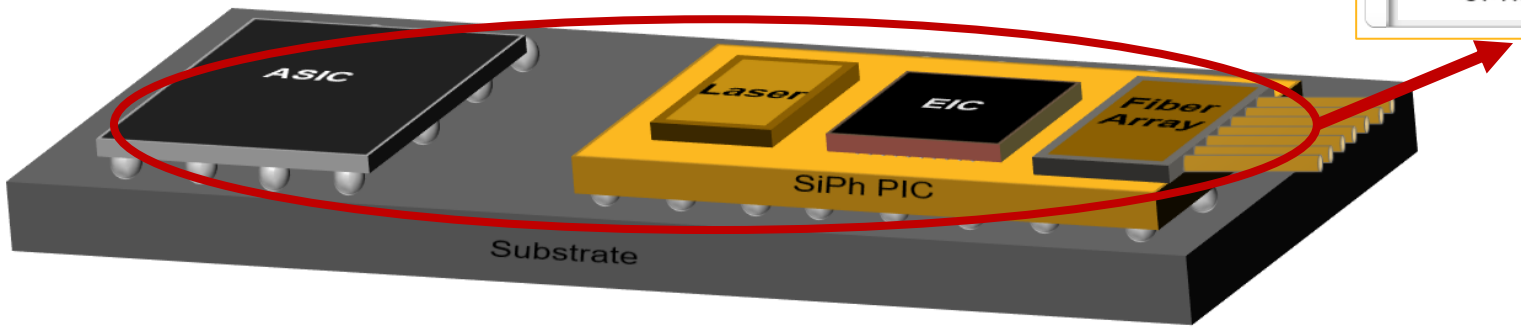


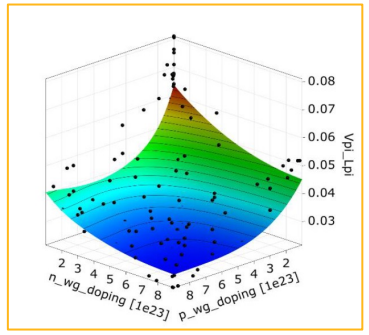
Optimization and Robustness Analysis

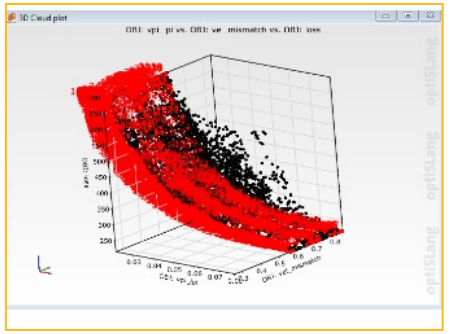
- Ansys **optiSLang** coupled with other Ansys tools, offers workflows to automate your simulation toolchains and connect to state-of-the art optimization algorithms to perform parametric design studies and better understand your designs.

- optiSLang provides a unified workspace to launch Multiphysics optimization workflows.
- Built-in AI/ML driven optimization and robustness analysis algorithms enable robust designs tolerant to manufacturing variations.









Summary

- CPO holds promising solutions for future data center and HPC applications.
- Designers need to solver multiple design challenges to enable CPO.
- Ansys, with its array of Multiphysics simulation tools, is strategically positioned to facilitate comprehensive design solutions.
- Robust package design with fully automated workflows powered by advanced AI/ML algorithms.


Ansys