Heraeus

Electronics

“ELECTRONIC PACKAGING MATERIALS FOR SIC POWER MODULES”

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TODAY'S AGENDA

1 | THE WORLD BECOMES ELECTRIC

2 | REQUIREMENTS FOR POWER MODULE CHANGE

3 | SUBSTRATE TECHNOLOGIES: DCB VS AMB SUBSTRATES

4 | DIE ATTACH AND MODULE ATTACH TECHNOLOGIES: SINTER VS SOLDER

5 | DIE TOP CONNECTIONS: AL VS CU DIE TOP CONNECTIONS

6 | CONCLUSION

THE WORLD BECOMES ELECTRIC

POWER ELECTRONICS HAS **SIGNIFICANT POTENTIAL FOR CO_2 REDUCTION** AND IS **INEVITABLE TECHNOLOGY TOWARDS ZERO EMISSION WORLD**

3 MAIN DRIVERS FOR POWER MARKET GROWTH

CO_2 ↓

Energy generation ↑

electrification

sustainability

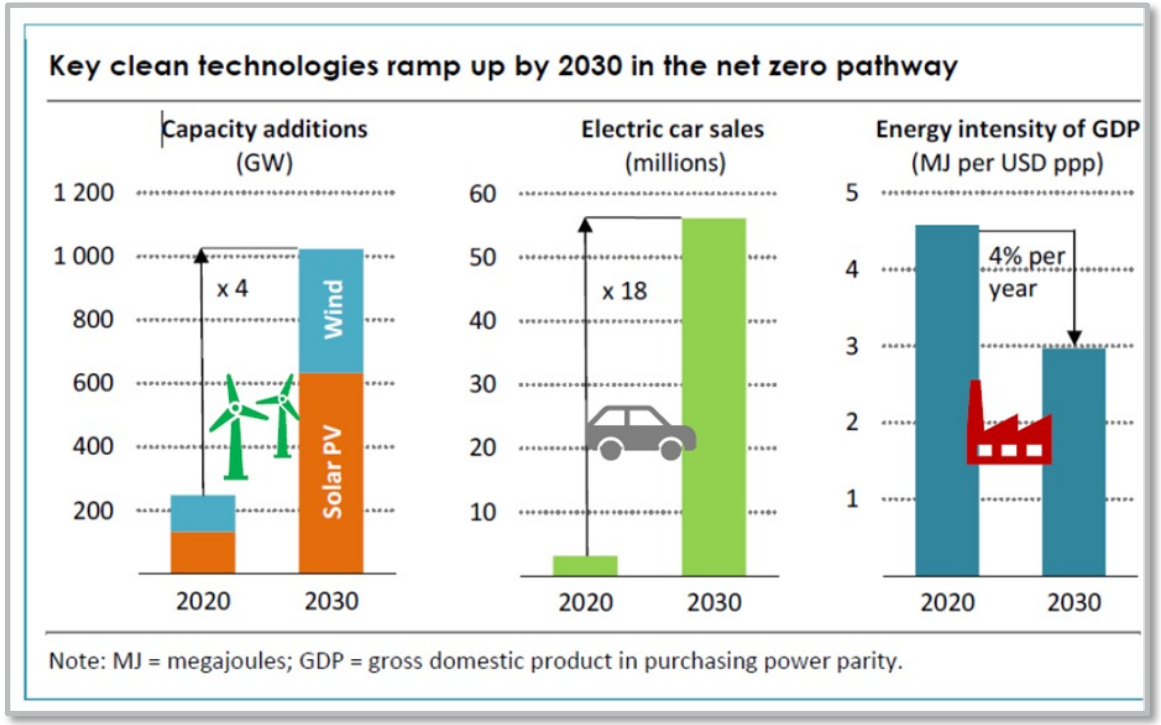
Electricity consumption ↑

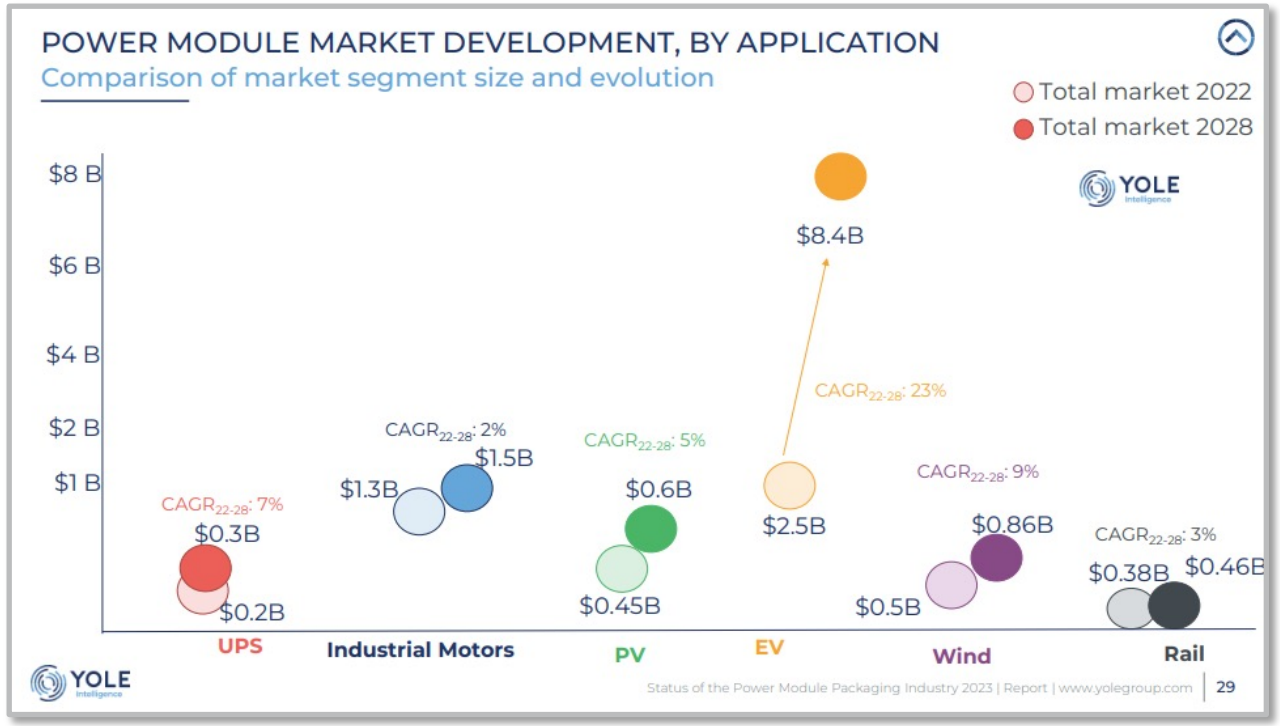
Energy consumption ↓

Source: Yole Report, Status of the Power Module Packaging Industry 2024

“Electronic Packaging Materials for SiC Power Modules” - Dr. Michael Jörger - PE International - April 2024

Power Electronics play a **key role** in today's **increasingly electrified world…**





Source: Yole Report Status of the Power Electronic Industry 2023

….from generation to distribution and consumption in industrial, automotive, renewable energies, appliances …

REQUIREMENTS FOR POWER MODULE CHANGE

TRENDS IN POWER MODULE PACKAGE

Si to WBG

Higher Power Density

Higher Reliability

Lower Total Cost of Ownership

Reduction Weight & Volume

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POWER SEMICONDUCTORS AND
NEED FOR NEW PACKAGING MATERIALs SOLUTIONS

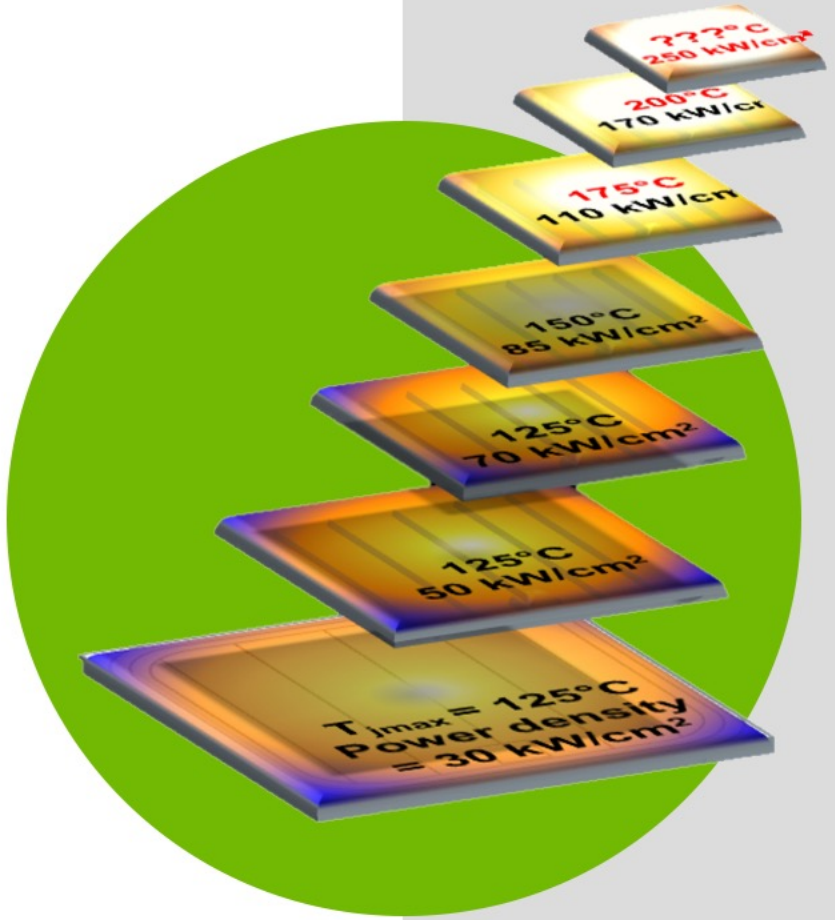
Smaller and Thinner Dies → **Increased Power Density** → **Higher Operating Temperature**

Benefit through smaller dies

- Reduction of chip size / cost
- Lower losses / higher efficiency
- Increase of power & current density per chip

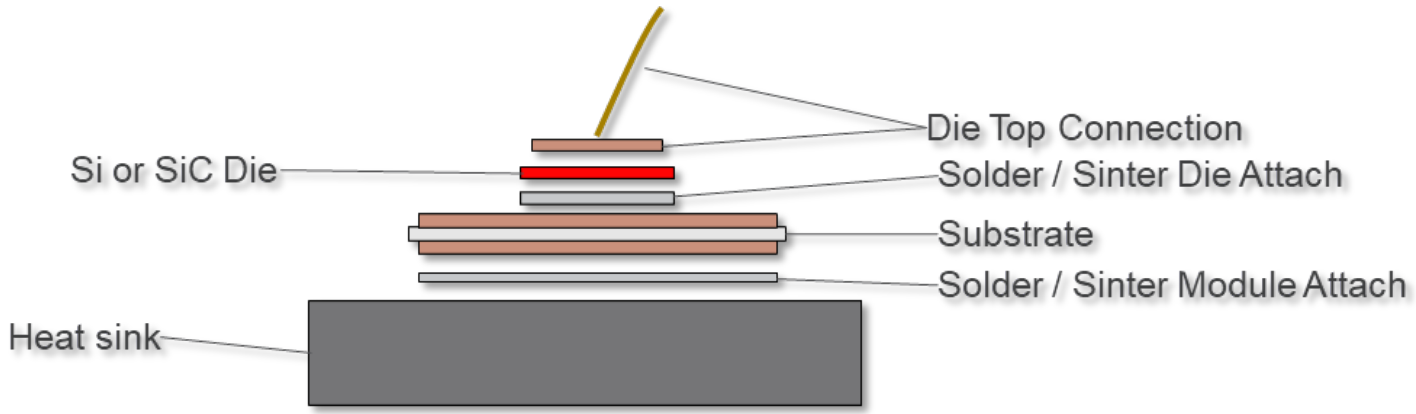
Packaging challenges

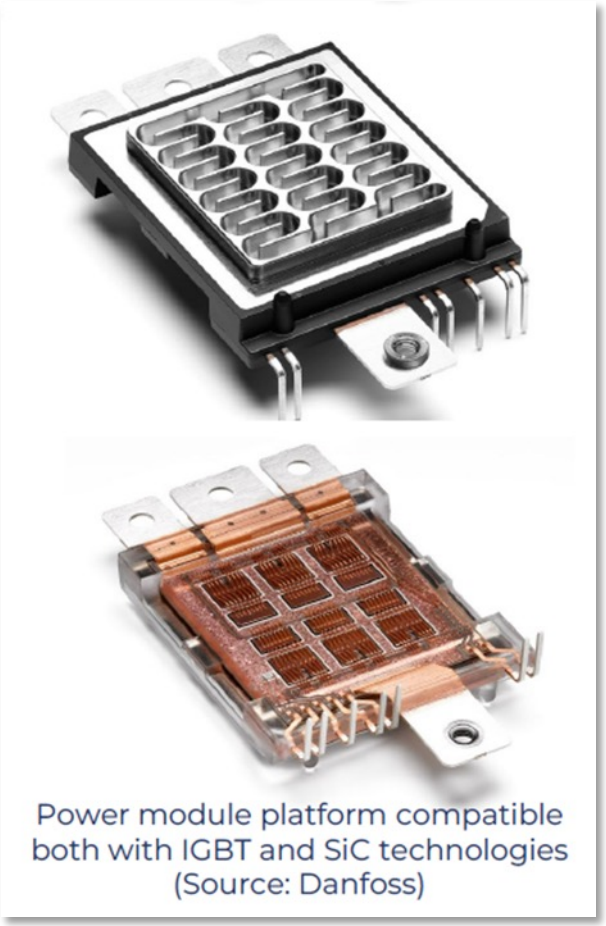
- Increased power loss per chip area requires materials with better heat dissipation
- More power needs better current carrying capability of packaging materials
- Increased operating temperatures and reliability challenges



Source: Challenges of New Packaging Solutions for Power Modules, Prof. R. Eisele - FH Kiel, Anton Miric - Heraeus Electronics GmbH & Co. KG, PCIM Conference May 2021

SIMPLIFIED POWER MODULE PACKAGE




Power module platform compatible both with IGBT and SiC technologies (Source: Danfoss)

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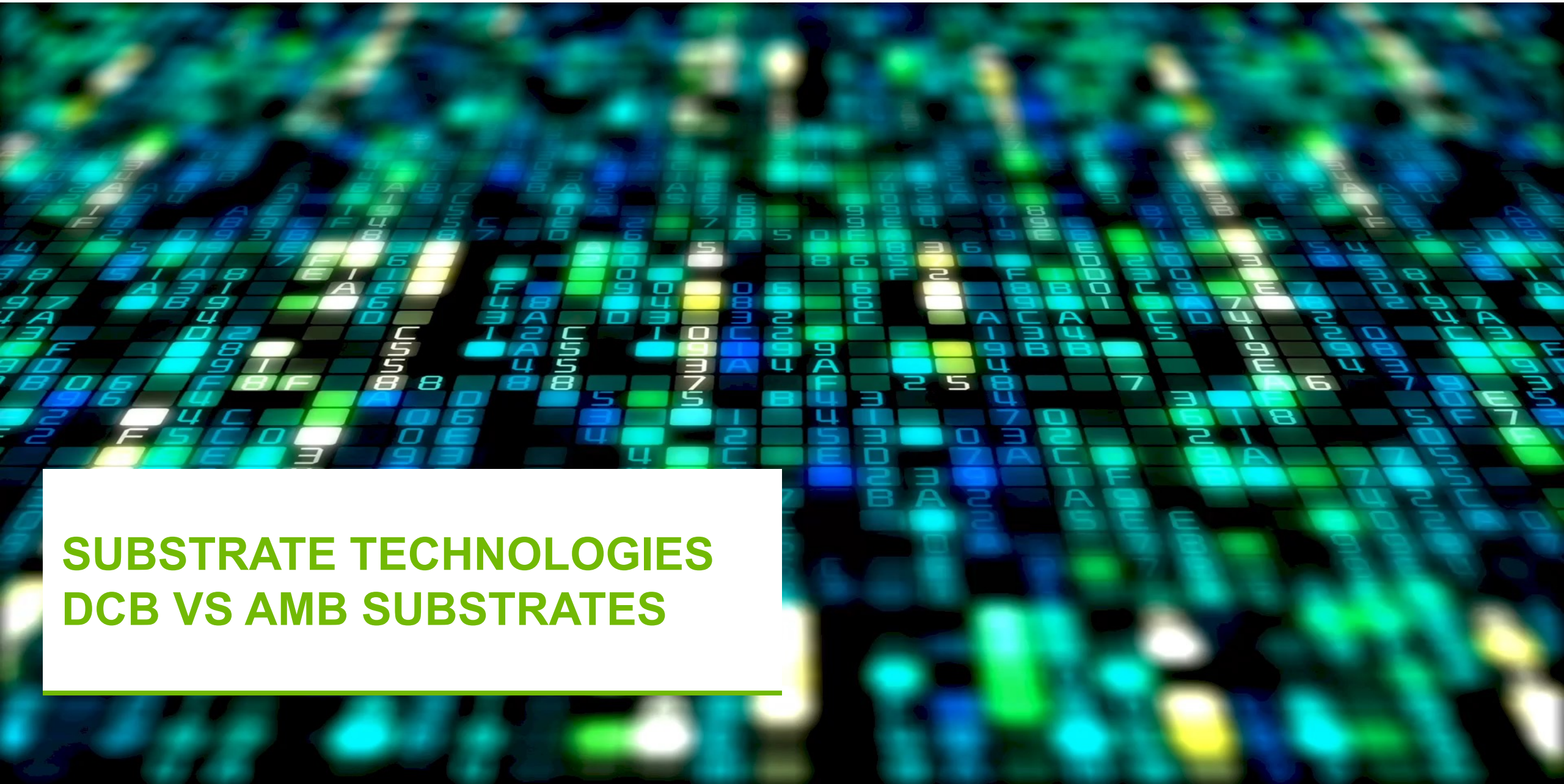
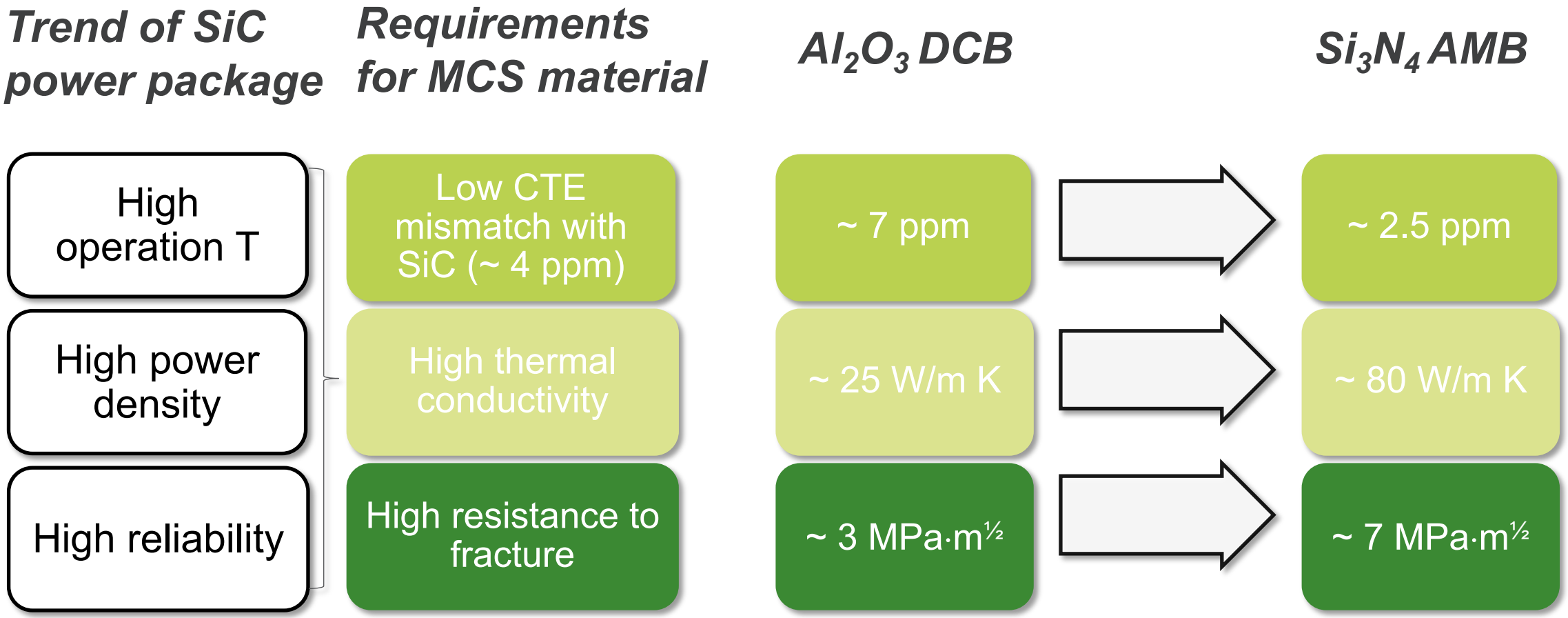


SUBSTRATE TECHNOLOGIES
DCB VS AMB SUBSTRATES

WHY DO WE NEED **NOVEL SOLUTION** FOR SUBSTRATE?



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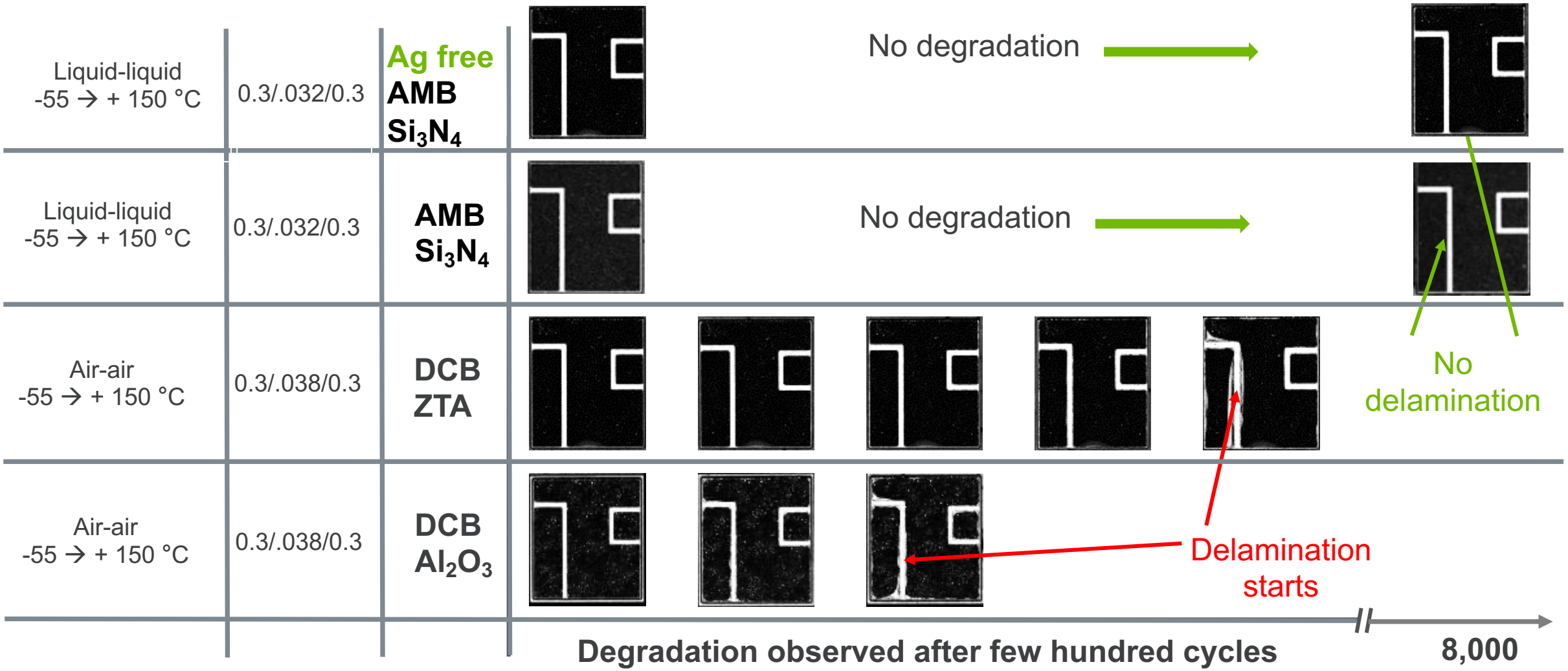
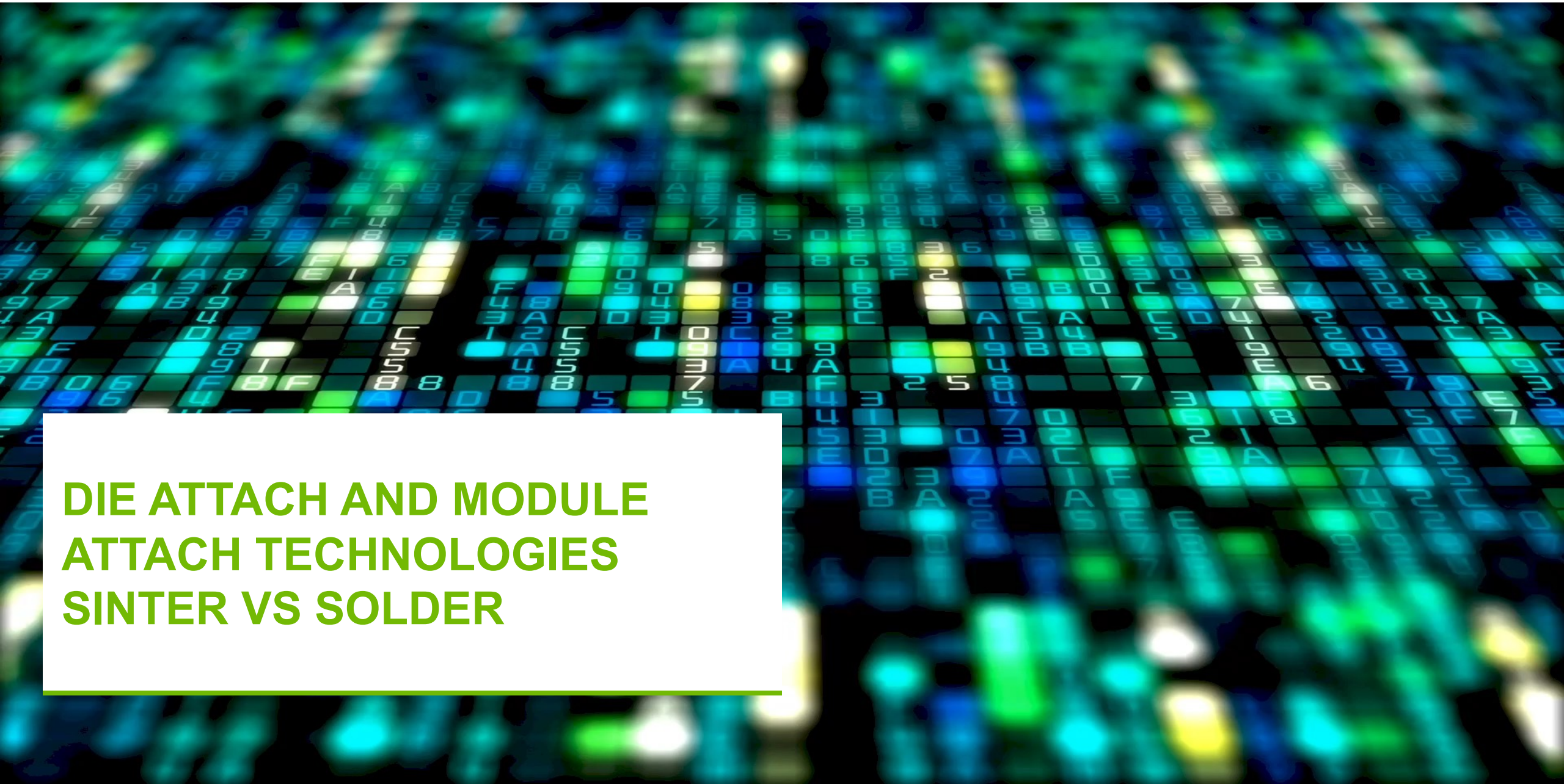
SI_3N_4 SUBSTRATE IS THE **MOST SUITABLE** SOLUTION FOR SIC PACKAGE





DIE ATTACH AND MODULE ATTACH TECHNOLOGIES SINTER VS SOLDER

WHY DO WE NEED **NOVEL SOLUTION** FOR DIE AND MODULE ATTACH?

Trend of SiC power package	*Requirements for DA material*	*Solder*	*Ag Sinter*
High operation T	High melting point	~ 220 °C	~ 960 °C
High power density	High thermal conductivity	~ 50 W/m K	~ 250 W/m K
High reliability	High creep resistance	$T_w/T_m > 0.7$	~ $T_w/T_m < 0.3$

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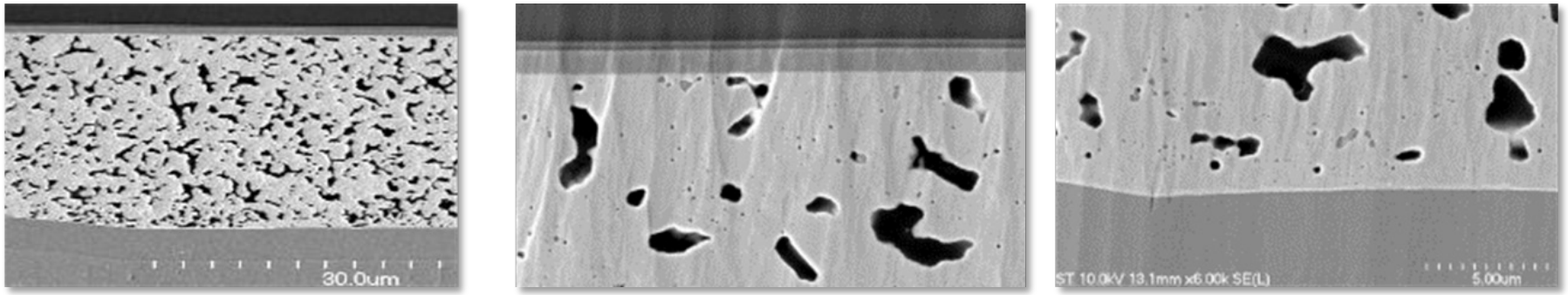
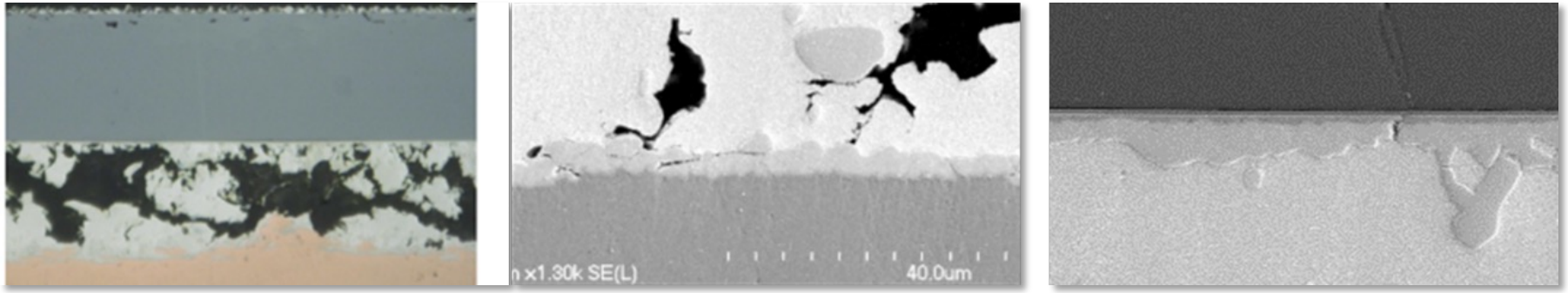
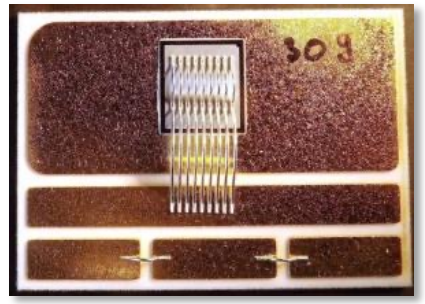
BENEFIT OF DIE-SINTERING - NO DEGRADATION



Sintered Module with AlCu-Wire after 130.000 Power Cycles



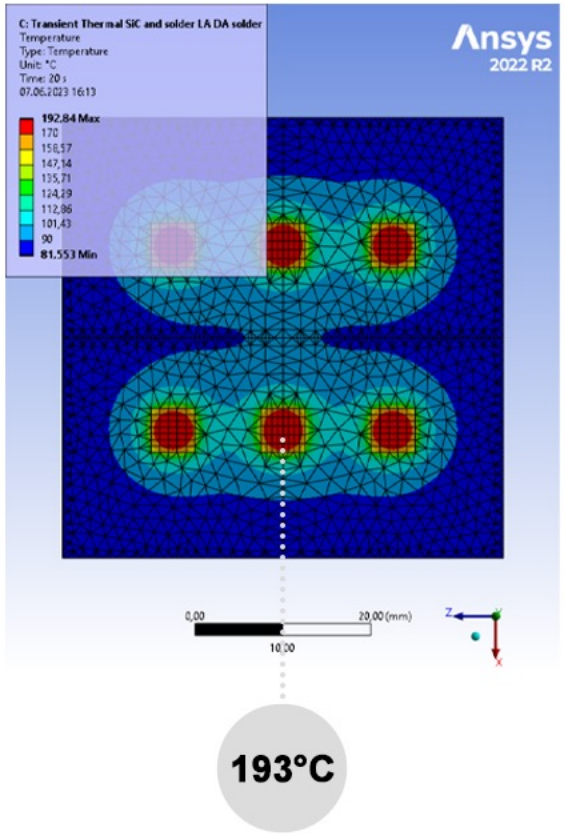
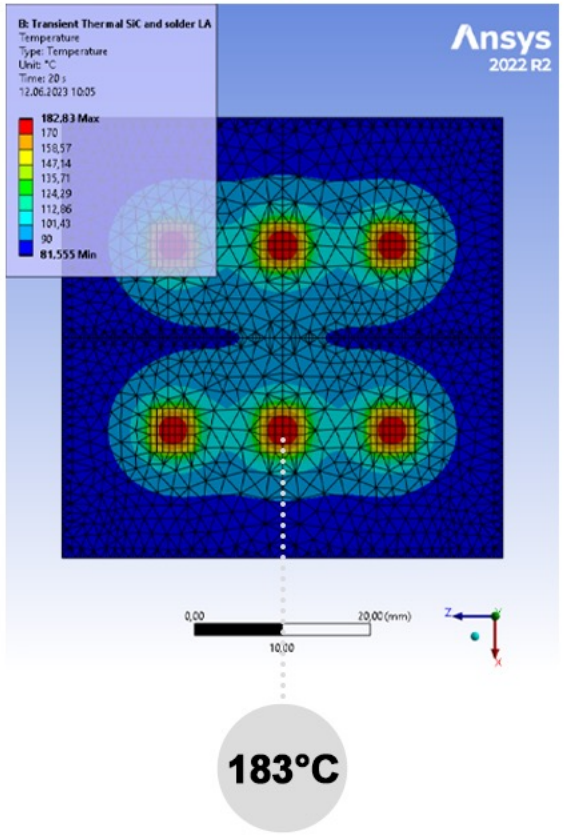
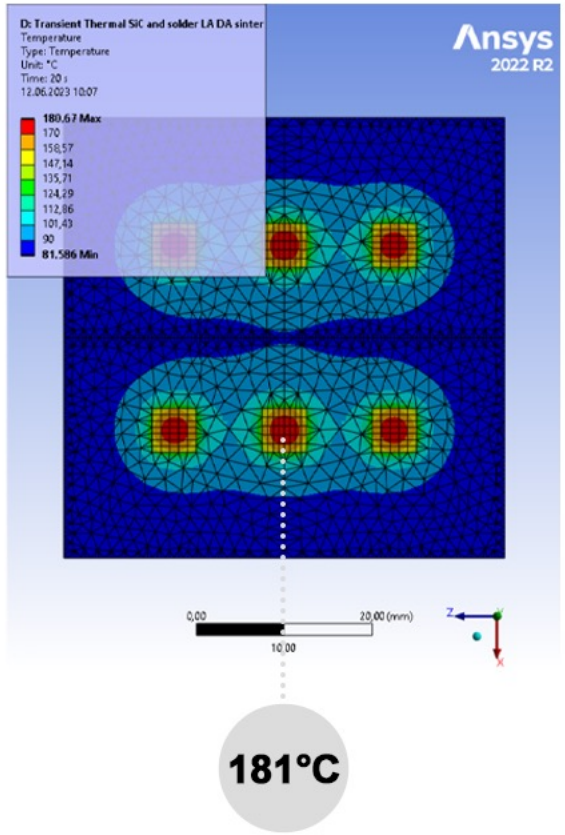
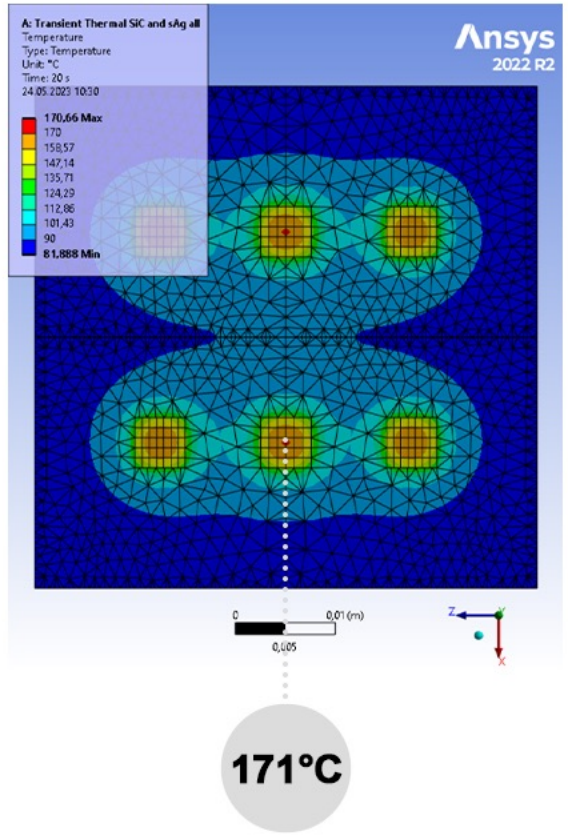
Soldered Module with AlCu-Wire after 56.000 Power Cycles



Test parameters:
T_{on} = T_{off} = 15 sec
T_C = 40°C
dT_{max} = 110 K
T_{max} = 150 °C

Source: T.Krebs et al, 63rd ECTC, 2013

BENEFIT OF MODULE **SINTERING** – HEAT DISSIPATION

Die Attach: soldered Module Attach: soldered	Die Attach: sintered Module Attach: soldered	Die Attach: soldered Module Attach: sintered	Die Attach: sintered Module Attach: sintered
			
193°C	**183°C**	**181°C**	**171°C**

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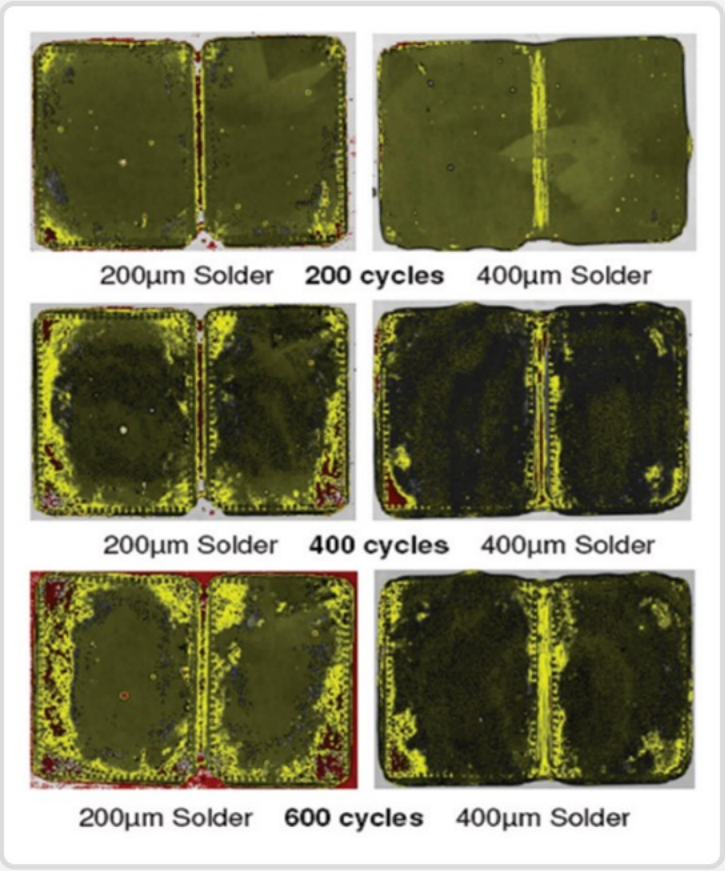
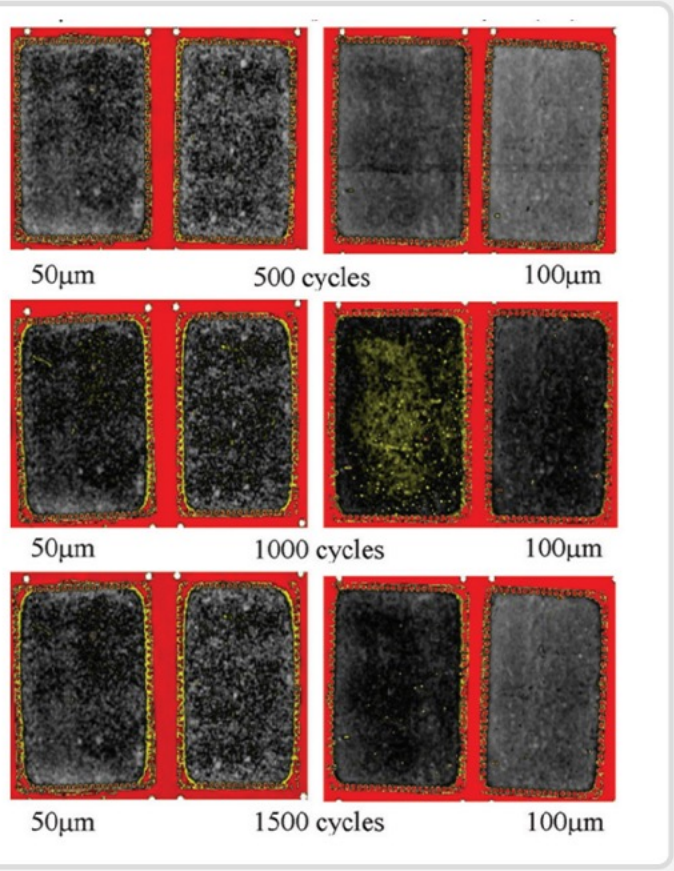
BENEFIT OF MODULE **SINTERING** – RELIABILITY

Module soldered



Module sintered



Source: Pressure Sintering for Power Modules, Mathias Kock, …et. al, Power Electronics Europe, issue7, 2007

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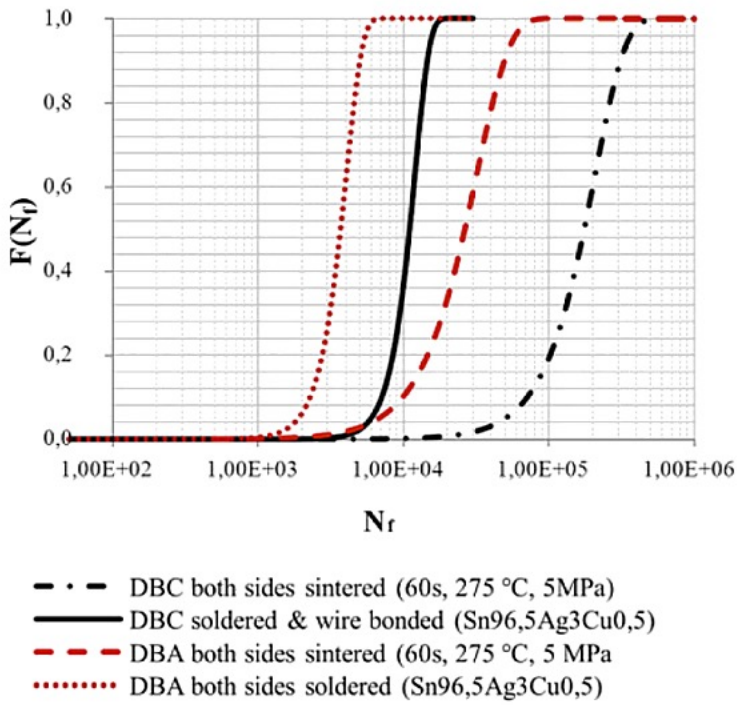
ALL SINTERED MODULE HAS A SIGNIFICANTLY **INCREASED** **LIFETIME**

Materials properties	Solder paste	Sinter paste
Electrical resistivity (mΩ/cm)	0.01-0.03	≤0.008
Thermal conductivity (W/m·K)	20-50	>200
CTE (ppm/K)	25-30	19
Residue free	No	Yes

- Higher reliability at TCT could be achieved by Ag sintering



- A Weibull distribution of active temperature cycling[1]

Source: Innovative Material Packaging Solutions for superior Power Electronics Devices, EDPC Conference Nov. 2016, Nürnberg, A. Miric, Dr. Frank Osterwald, P. Dietrich, A.S. Klein, A. Hinrich

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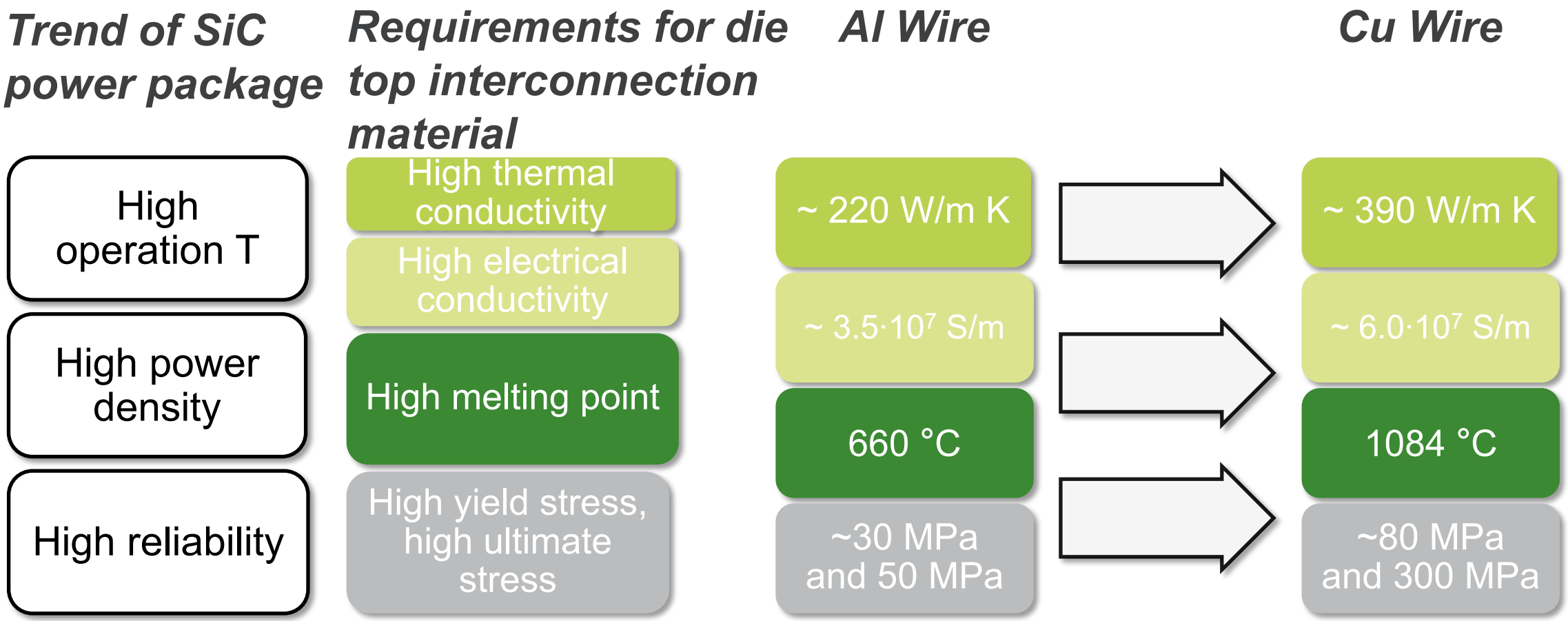
DIE TOP CONNECTIONS
AL VS CU DIE TOP CONNECTIONS

WHY DO WE NEED **NOVEL SOLUTION** FOR DIE TOP CONNECTION?

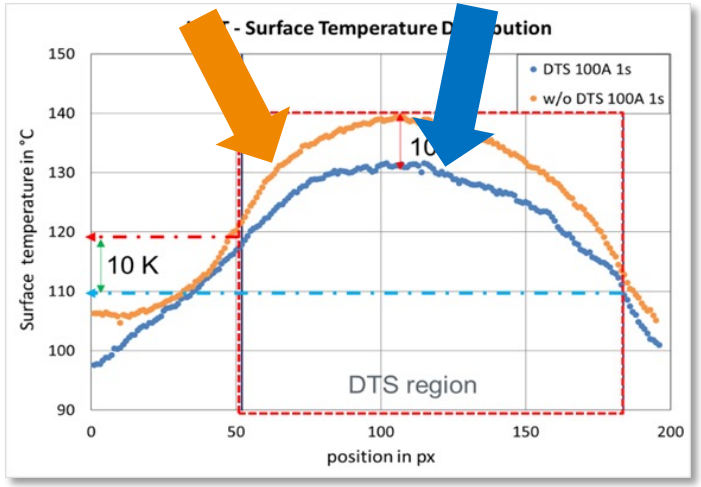


POWER CYCLING SOLDER & AL WIRE VS. SINTER & CU WIRE

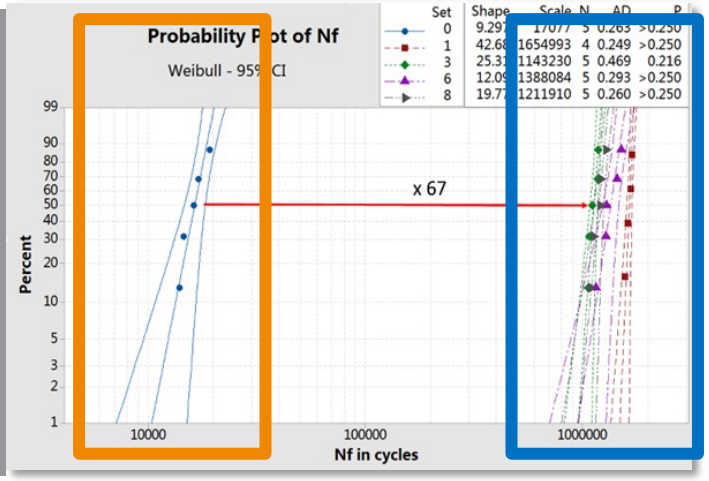
SOLDER / AL WIREBONDING

- **Bond wires:** 400µm Al wire
- **Die attach:** SnAg solder

TEMPERATURE



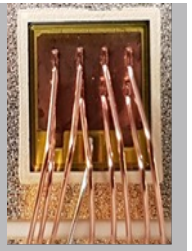
RELIABILITY



Powercycling: I(const.)=136A/ton=1s, toff=2s, DT=130K, Tmax=175°C, failure 5% increase VCE

SINTER / CU WIREBONDING

- **Bond wires:** 400µm Cu wire
- **Die attach:** Ag sinter



- **More homogenous heat distribution**
- **Reduced thermal stress on die topside**

- **Number of cycles increased by a factor > 60**
- **Highest lifetime and performance**

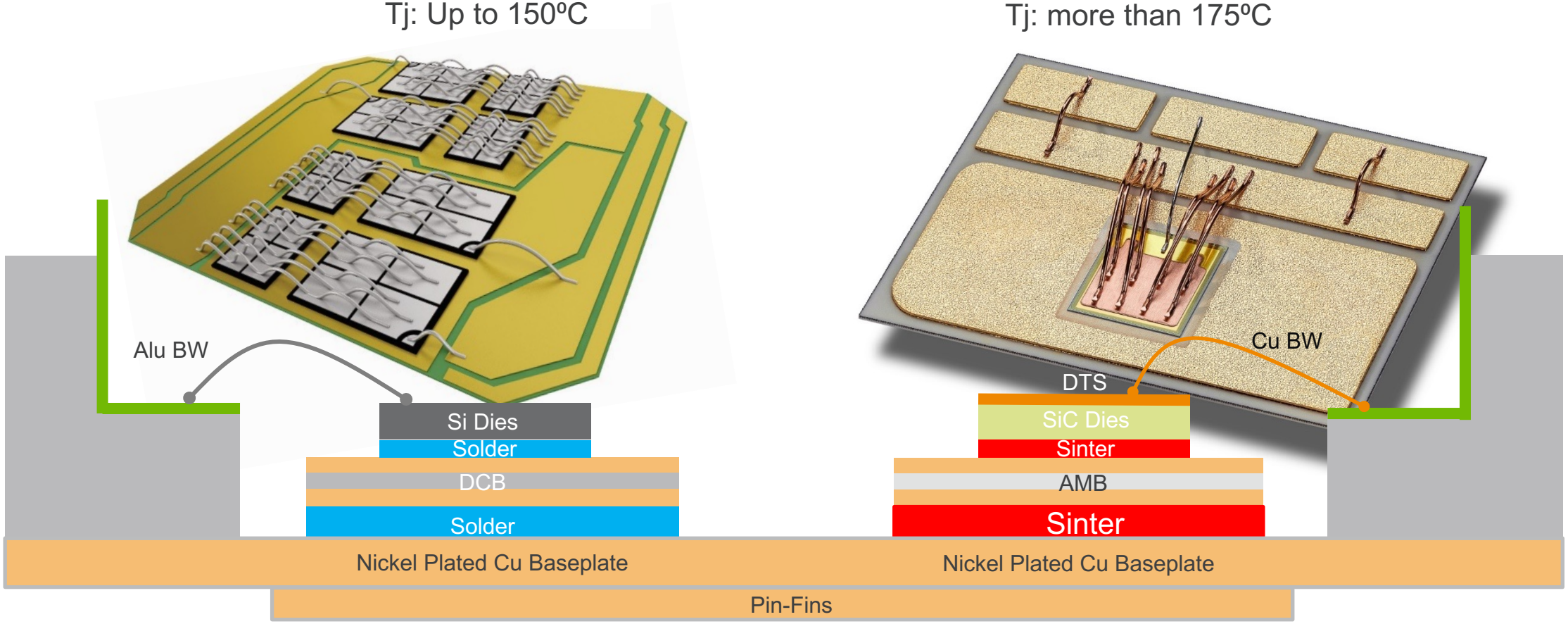
Source: C. Fery, A. Hinrich – Heraeus Electronics GmbH & Co. KG, PCIM Conference May 2021

CONCLUSION

CONCLUSION: TO BENEFIT FROM THE CHANGE OF SI TO SIC BASED POWER MODULES A **CHANGE** IN ELECTRONIC PACKAGING MATERIALS **IS REQUIRED**

IGBT

Tj: Up to 150ºC



Wide Band Gap

Tj: more than 175ºC

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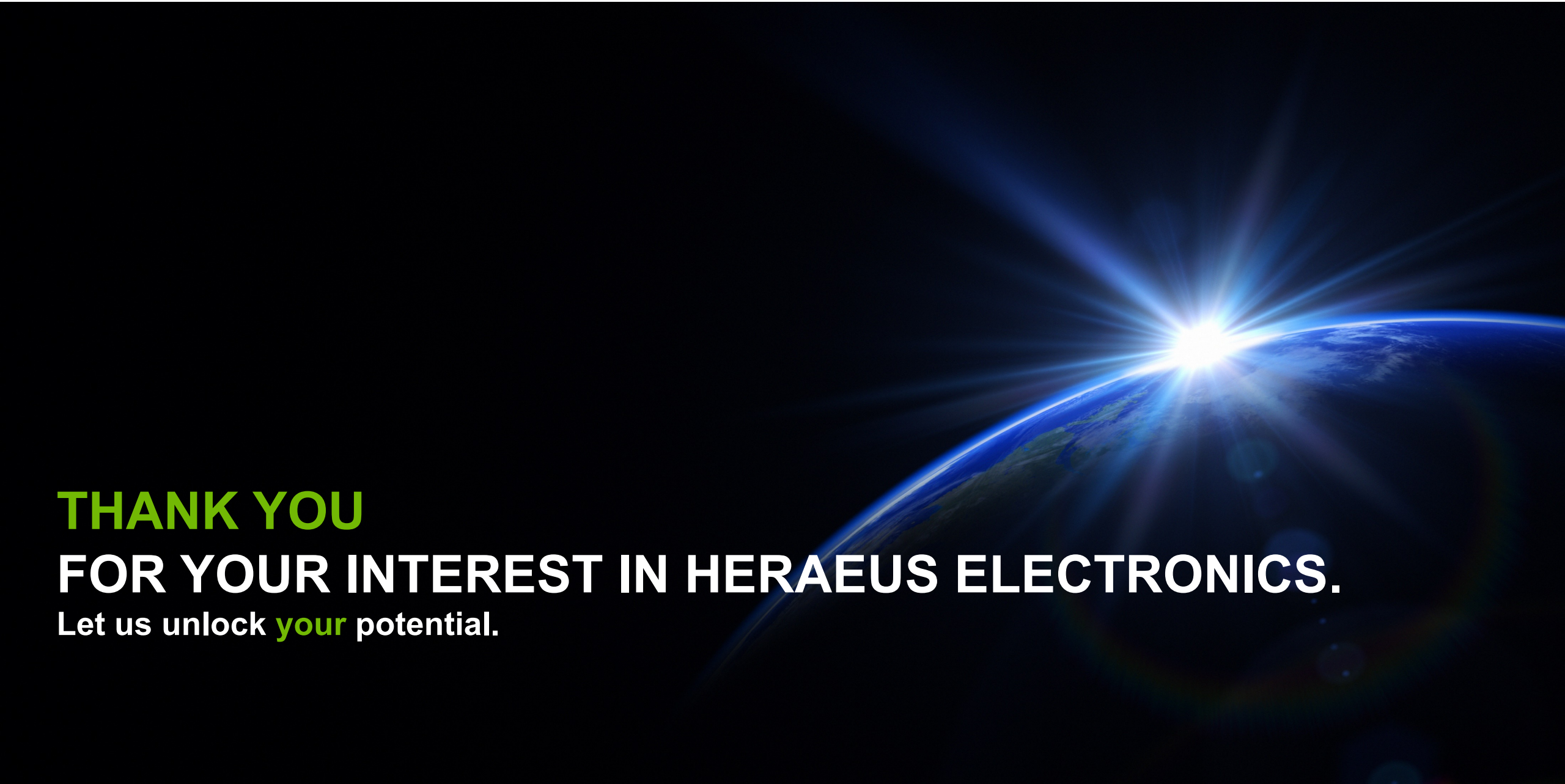

THANK YOU

FOR YOUR INTEREST IN HERAEUS ELECTRONICS.

Let us unlock your potential.