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Cost-effective SiC Substrate Manufacturing for Power Devices Enabled by Oxide-free Wafer Bonding

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EV Group | At A Glance

Leading supplier of wafer processing equipment for the MEMS, nanotechnology and semiconductor markets

Founded in 1980 by DI Erich and Aya Maria Thallner. More than 1300 employees worldwide

Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China and Taiwan

EV Group Headquarters

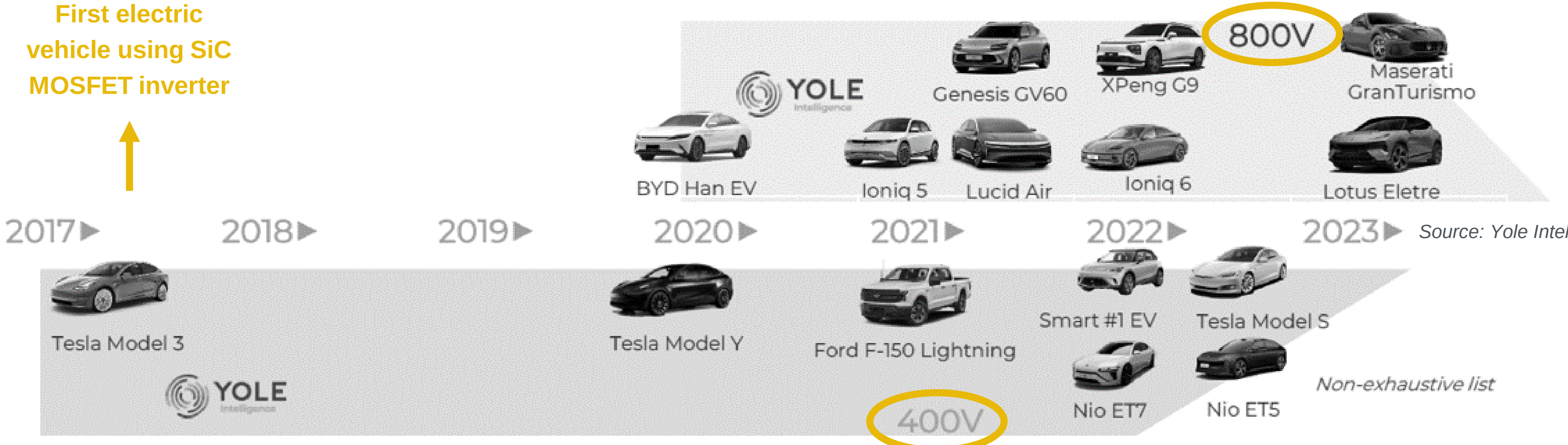
St. Florian am Inn, Austria

SiC Power Devices | Automotive Industry as a Driver

Trend for faster EV charging requires higher charging voltages → **SiC as an enabler**

- High adaption of SiC for inverters as well as high-power DC-chargers
- SiC is forecast to have 90% penetration in 800V by 2028

First electric vehicle using SiC MOSFET inverter



Source: Yole Intelligence

Continuous adaption of SiC in 400V EVs, still main segment requiring SiC devices; competition from Si-IGBT devices

SiC MOSFETs have superior device performance compared to conventional silicon-based devices

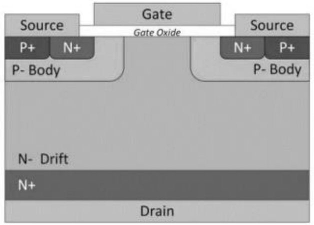
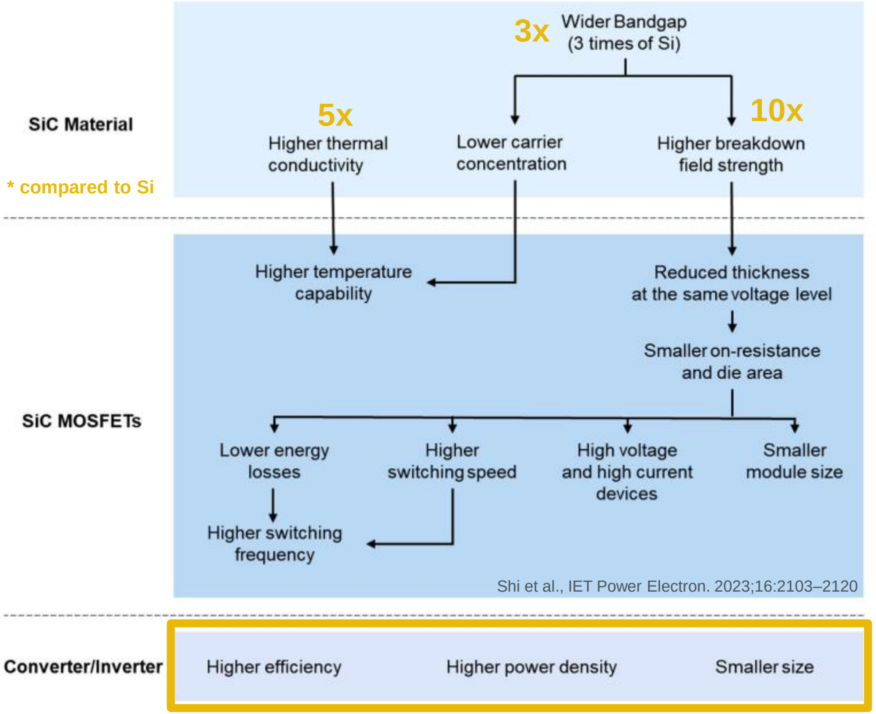


Image Source:
powerelectronicsnews.com

Advantages for EVs

- Lower energy losses
- Improved vehicle performance
- Superior temperature resistance
- Increased efficiency
- Reduced size and weight compared to conventional inverters



Shi et al., IET Power Electron. 2023;16:2103–2120

SiC Power Devices | Manufacturing Challenges

SiC manufacturing processes are not mature yet and face a lot of challenges

Substrate Manufacturing → Epitaxy → Chip Manufacturing → Packaging

Challenges:

- Substrate Cost
- Defects
- Complex Processing
- Reliability
- Yield
- Limited Economies of Scale
- System Cost

Major concerns are related to SiC substrates

- **Cost**, Defects, Supply, etc.

Several routes to reduce cost are considered

→ Novel Wafer Slicing Technologies

→ 8 inch Manufacturing

→ **Engineered Substrates**

→ … and many more

Raw wafer accounts for almost **30 %** of die manufacturing

Vertical SiC Power MOSFET | Engineered Substrates

Conventional vertical SiC MOSFET

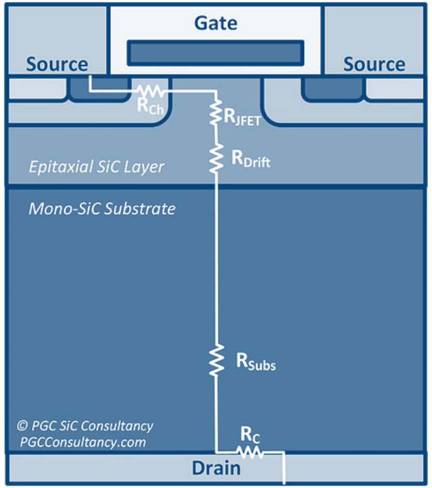


Image Source: PGC Consultancy

High quality mono-crystalline SiC substrates are expensive !

SiC Substrate / Wafer

Cost-effective vertical SiC MOSFET

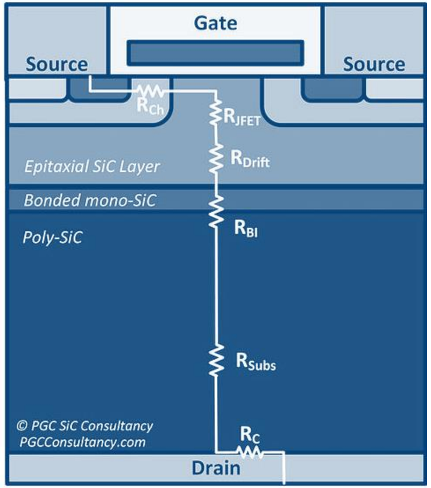


Image Source: PGC Consultancy

Thin mono-crystalline SiC on top of less-expensive substrate

Needs Conductive wafer bonding

Conventional Fusion Bonding vs. ComBond® Technology

EVG Gemini FB

Plasma activated Fusion Bonding

Top Wafer

(Native) Oxide Layers

Bottom Wafer

Top Wafer

Bottom Wafer

→ Oxide interface

EVG ComBond®

Top Wafer

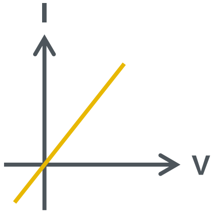
Oxide Removed

Bottom Wafer

Top Wafer

Bottom Wafer

EVG ComBond®



→ Oxide-free interface

→ **Enables conductive interfaces**

Conventional Fusion Bonding vs. ComBond® Technology

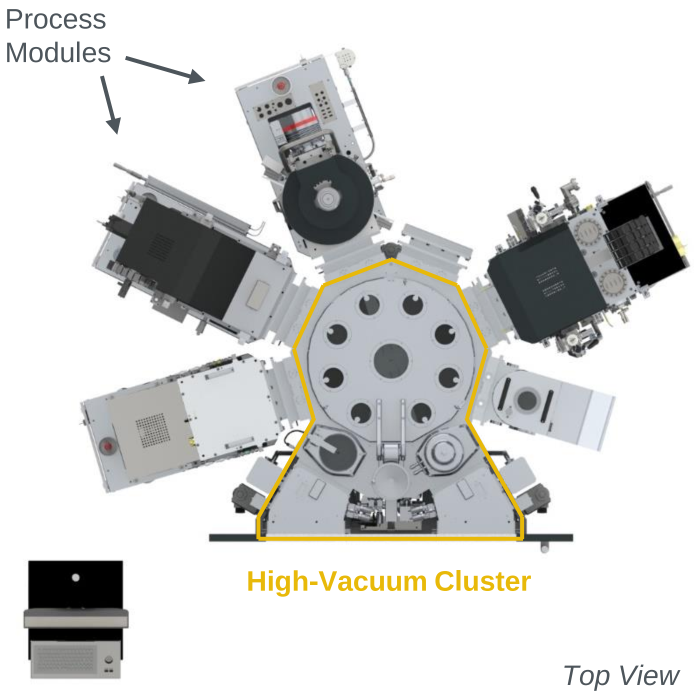
Parameter	Plasma-Activated Fusion Bonding	ComBond® or Covalent Bonding
Pre-Treatment	Plasma (O_2 / N_2)	Sputtering (Accelerated Ar ions)
Treatment Effect	Activation / Oxide growth	Oxide removal
Environment	Ambient air	Ultra-high vacuum (avoids re-oxidation)
Post-bond Annealing	Yes (typ. > 200 °C)	No (room temperature bonding)
Bond Type	Covalent	Covalent
Bonding Interface	Oxide-Oxide (e.g. Si/SiO_2–SiO_2/Si)	Oxide-free (e.g. Si–Si)
Possible side effect	-	Thin amorphous layer (nm range)

↓ Gemini (FB) Wafer Bonding Platform

↓ ComBond® Wafer Bonding Platform

ComBond® High-Vacuum Cluster

Fully automated wafer transport and handling at a base pressure of < 5·10-8 mbar



Top View

High-Vacuum Cluster Features

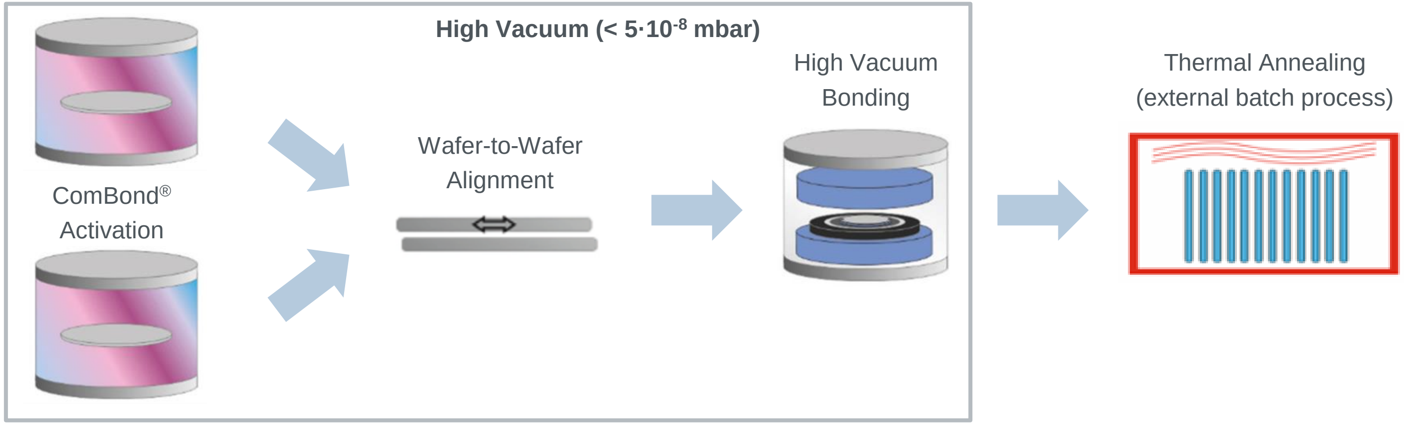
- 6 or 8 inch configuration
- Manual, cassette or EFEM loading with load lock functionality
- Up to 6 free high-vacuum ports for process modules
- Base pressure < $5 \cdot 10^{-8}$ mbar (with bake < 24 h)
- Minimal cleanroom footprint

Front View

SiC – SiC Bonding | Process Flow

Direct bonding of Silicon-Carbide without any interface layer

Process Flow



In-situ oxide removal

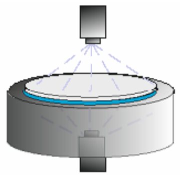
In-situ alignment

Low-force room-temperature bonding

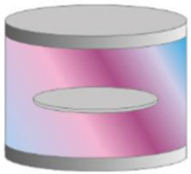
Test Wafer Specification:

- N-type 100 mm research grade 4H-SiC
- 350 µm thickness
- Double-side polished
- Si-face with epi-ready quality
- < 0.5 nm surface roughness

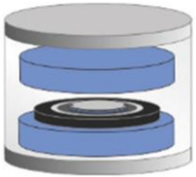
SiC – SiC Bonding | Characterization



Metrology



ComBond® Activation



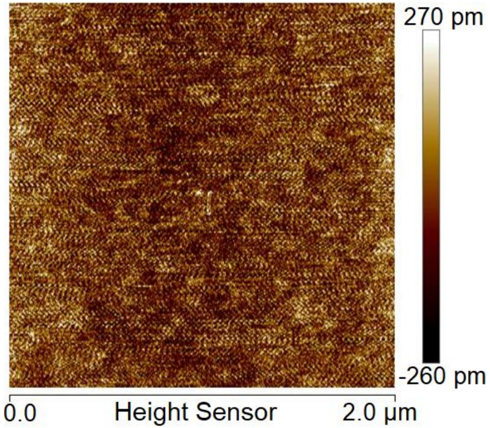
High Vacuum Bonding

Incoming Inspection	Activated single wafer	Bonded Wafer Pair
Surface roughness	Surface roughness	–
Geometry (bow, warp, TTV)	–	Geometry (bow, warp, TTV)
Oxide thickness	–	Amorphous layer and reoxidized layer thickness
Chemical composition of surface	Chemical composition of surface	–
–	–	Bonding Quality
–	–	Bonding Energy
Amorphous layer thickness	Amorphous layer thickness	Amorphous layer thickness
–	–	Elemental composition of bonding interface

Pre-Bonding Characterization | Surface Roughness

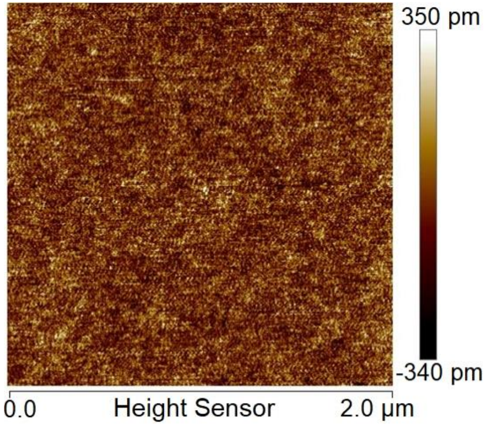
Low surface roughness is preserved during wafer activation process

Before surface Activation



$R_q = 0.76$ Å

After surface Activation



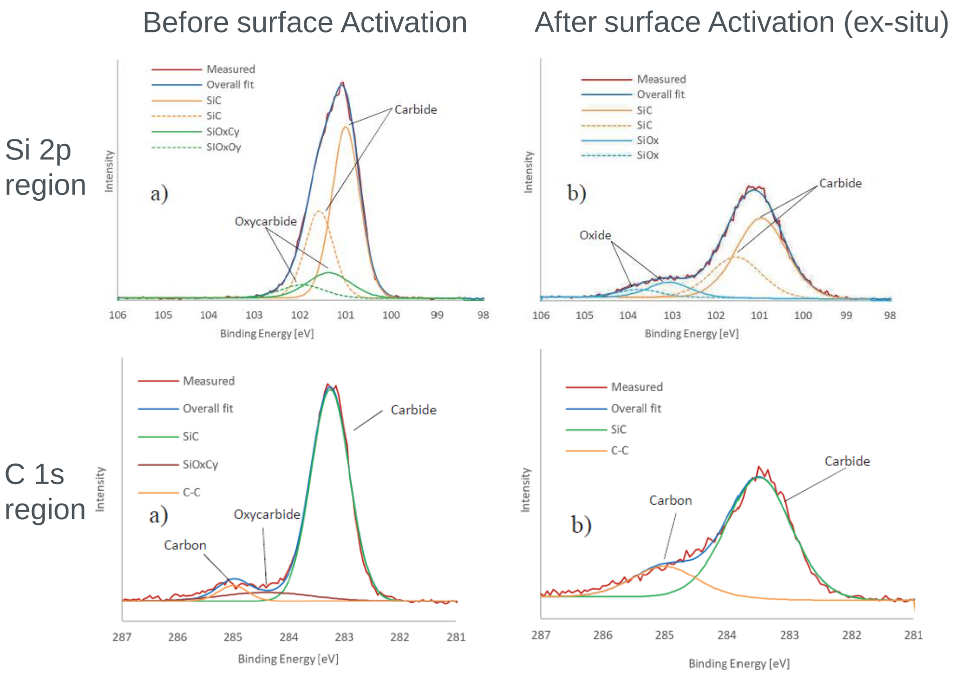
$R_q = 0.98$ Å

Combond Activation Module:
In-situ surface pretreatment based on dry etch process

Surface roughness well below the requirement for fusion bonding (< 5 Å)

Pre-Bonding Characterization | Oxide Removal

Oxide removal after ComBond® activation confirmed with XPS measurements

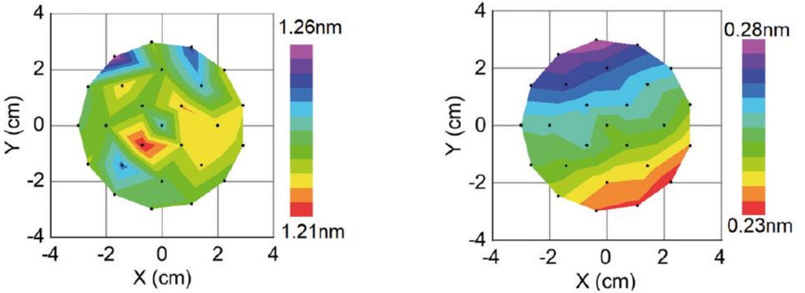


X-ray Photoelectron Spectroscopy (XPS)

- Composition of the re-grown oxide (SiO_2) is different than the native oxide (Silicon Oxycarbide)
- Oxycarbide peak disappeared which indicates successful oxide removal
- Increased Carbon content due to selective sputtering of the SiC surface by Ar atoms

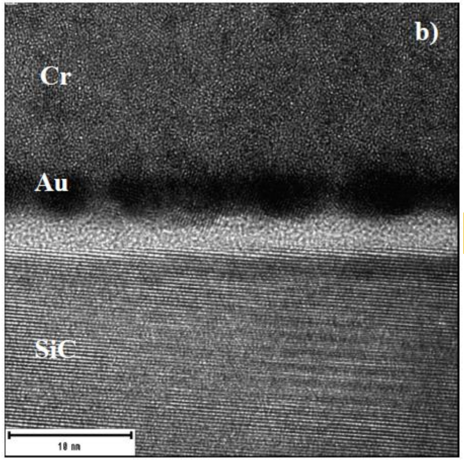
Pre-Bonding Characterization | Amorphous Layer

Amorphous layer is forming during ComBond® activation



Activated Wafer	Activated Wafer
Oxide Thickness	Amorphous layer thickness
1,24 nm	0,26 nm

Variable Angle Spectroscopic Ellipsometry (ex-situ)



Amorphous layer plus the re-grown oxide

1,7 nm

TEM measurement

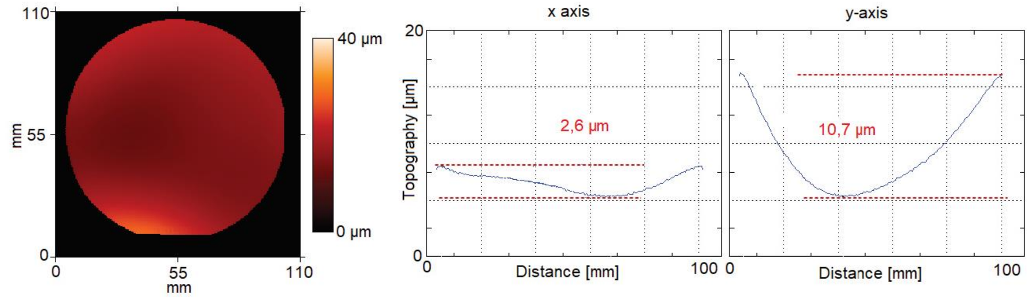
The evaluation model of the ellipsometry was verified by TEM measurements

Bonding Characterization | Geometry

No remaining stress after bonding process

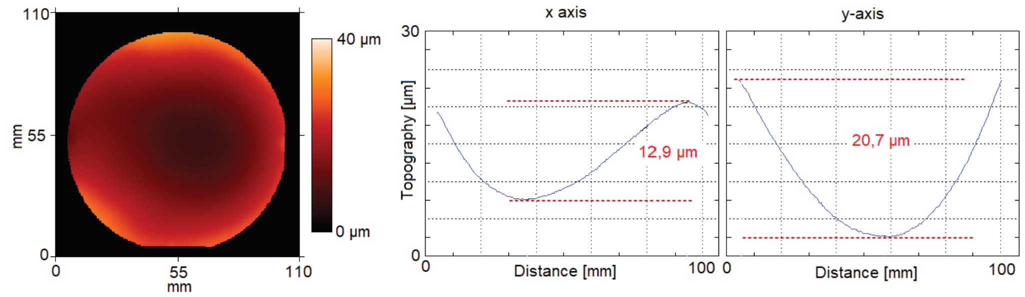
Incoming wafer

< 11 µm bow, < 15 µm TTV



Bonded wafer pair

< 21 µm bow, < 23 µm TTV



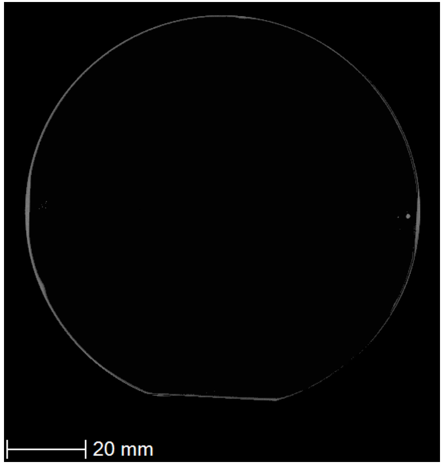
White light interferometer measurements

- Incoming wafer bow of single wafer fulfils requirement for fusion bonding (< 30 µm)
- Wafer bow does not significantly increase after bonding

Bonding Characterization | Bonding Quality / Bond Strength

Uniform high-quality bonding and bulk bond strength after annealing

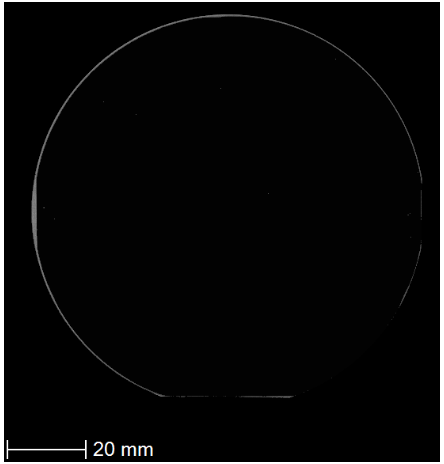
Before annealing



Bonding energy*: 1.4 J/m^2

Scanning Acoustic Microscopy

After annealing @ 1800°C



Bonding energy* same as bulk material

Good bonding quality

- No particle related voids
- No scratches
- No delamination
- No outgassing

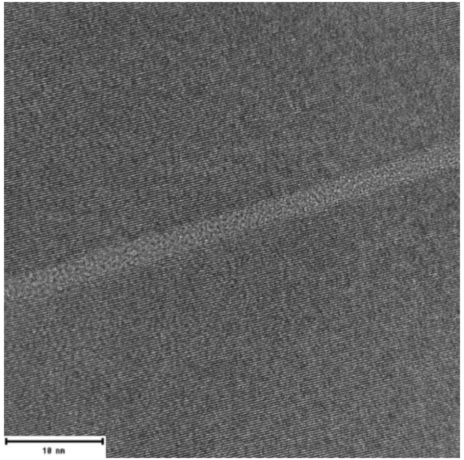
High bonding energy

** Bonding energy measured by Maszara test at 4 locations on the wafer*

Bonding Characterization | Interface

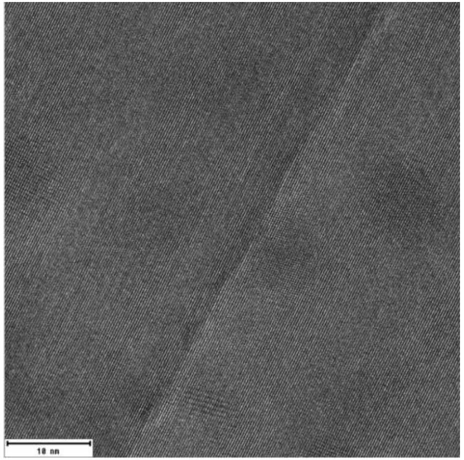
Full recrystallization after thermal annealing

Before annealing



Amorphous layer thickness at the bonding interface ~2,1nm

After annealing @ 1800°C

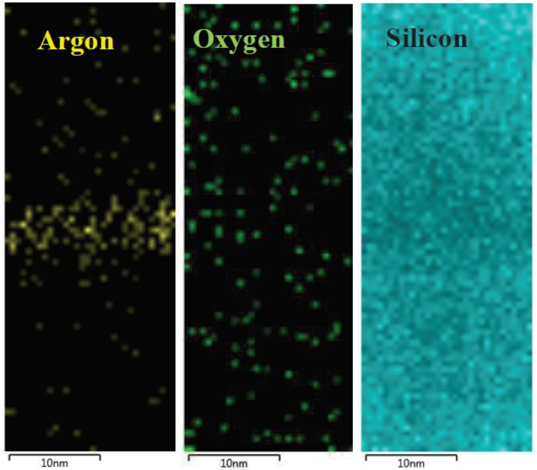


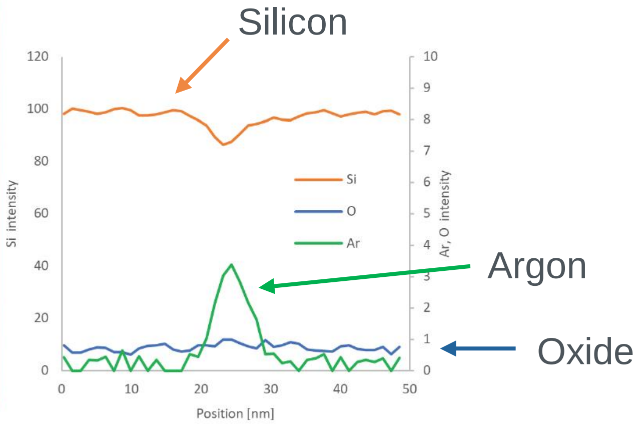
No measurable amorphous layer, full recrystallization

- No amorphous layer and full recrystallization after annealing
- Good electrical performance expected, characterization ongoing

Bonding Characterization | Interface - Elemental Analysis

Oxide-free bonding interface confirmed with EDX analysis





EDX measurement of the bonding interface

- No Oxygen content
- Minor amount of implanted Argon from activation process
- Reduced silicon content at interface (selective sputtering of Si compared to C during activation process)

Summary

- Strong SiC power device market growth driven by Electric Vehicles (EV)
- Still many manufacturing challenges need to be addressed
- Engineered substrates are one option to reduce SiC substrate cost
  - SiC-SiC wafer bonding using ComBond® technology has been successfully demonstrated and characterized
    - High bond energy
    - Defect-free high-quality bond interface
    - Oxide-free interface / full recrystallization

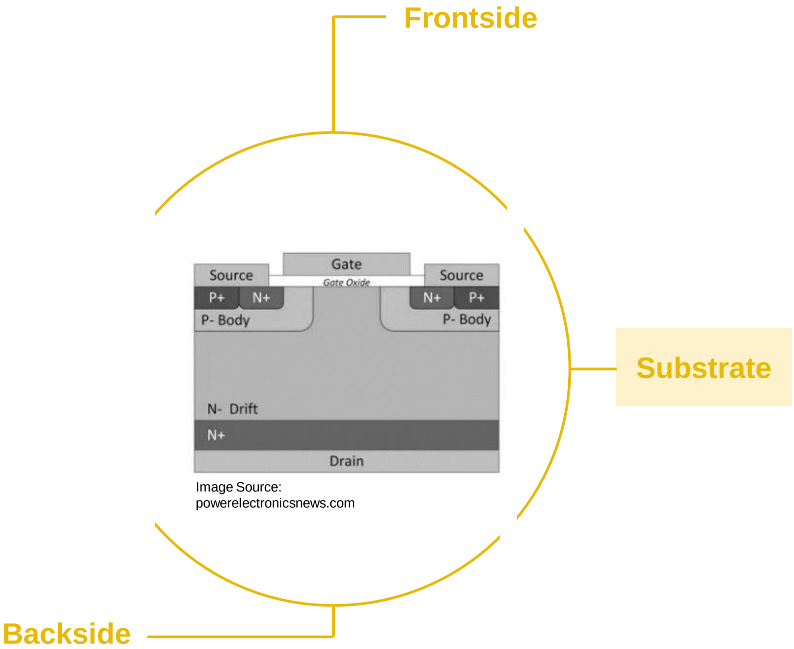


Image Source: powerelectronicsnews.com

Acknowledgement

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Ref.: Péter Kerepesi *et al* 2023 *ECS Trans.* **112** 159

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Thank you!

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